WHAT IS CLAIMED IS:

1. A wafer processing method for processing a wafer having a front side and a back side opposite to said front side, said front side of said wafer having a device area and a peripheral marginal area surrounding said device area, a plurality of crossing division lines being formed on said front side of said wafer to thereby define a plurality of separate regions in each of which a plurality of devices are formed, said wafer processing method comprising:

a back grinding step of grinding said back side of said wafer in a central area corresponding to said device area of said front side to thereby form a recess having a bottom surface in said central area of said back side and also form an annular reinforcing portion surrounding said recess;

a dicing tape attaching step of attaching a dicing tape to said back side of said wafer; and

a dividing step of cutting said wafer along said division lines from said front side of said wafer by using a cutting blade to thereby divide said wafer into a plurality of individual device chips each corresponding to said devices;

said back grinding step including the step of

forming a taper surface between the bottom surface of said recess and said annular reinforcing portion so that said taper surface connects the bottom surface of said recess and said annular reinforcing portion and said taper surface is inclined with respect to a direction perpendicular to the bottom surface of said recess;

said dividing step including the steps of relatively moving said cutting blade and said wafer along a predetermined one of said division lines and lowering said cutting blade toward said wafer to start cutting of said wafer at one end of said predetermined division line radially inside the annular reinforcing portion of said wafer, and raising said cutting blade from said wafer to stop cutting of said wafer at the other end of said predetermined division line radially inside the annular reinforcing portion of said wafer.

2. The wafer processing method according to claim 1, wherein said taper surface to be formed in said back grinding step has a taper angle defined as a supplementary angle of the angle formed between said taper surface and the bottom surface of said recess, said taper angle being set in the range of 30 to 75 degrees.

3. The wafer processing method according to claim 1, wherein a dicing tape attaching step includes

attaching said dicing tape to said bottom surface of said recess, said taper surface and said annular reinforcing portion of said wafer.

4. A wafer processing method for processing a wafer having a front side and a back side opposite to said front side, said front side of said wafer having a device area and a peripheral marginal area surrounding said device area, a plurality of crossing division lines being formed on said front side of said wafer to thereby define a plurality of separate regions in each of which a plurality of devices are formed, said wafer processing method comprising:

a back grinding step of grinding said back side of said wafer in a central area corresponding to said device area of said front side to thereby form a recess having a bottom surface in said central area of said back side and also form an annular reinforcing portion surrounding said recess;

a dicing tape attaching step of attaching a dicing tape to said back side of said wafer; and

a dividing step of cutting said wafer along said division lines from said front side of said wafer by using a cutting blade to thereby divide said wafer into a plurality of individual device chips each corresponding

to said devices;

said back grinding step including the step of forming a taper surface between the bottom surface of said recess and said annular reinforcing portion so that said taper surface connects the bottom surface of said recess and said annular reinforcing portion and said taper surface is inclined with respect to a direction perpendicular to the bottom surface of said recess;

said dividing step including the steps of relatively moving said cutting blade and said wafer along a predetermined one of said division lines and lowering said cutting blade toward said wafer to start cutting of said wafer at one end of said predetermined division line radially inside the outer circumference of said wafer, and raising said cutting blade from said wafer to stop cutting of said wafer at the other end of said predetermined division line radially inside the outer circumference of said wafer,

wherein said dividing step includes lowering said cutting blade toward said wafer to start cutting of said wafer at an outer edge of said recess and raising said cutting blade from said wafer to stop cutting of said wafer at an opposing outer edge of said recess.

5. The wafer processing method according to claim

4, wherein said taper surface to be formed in said back grinding step has a taper angle defined as a supplementary angle of the angle formed between said taper surface and the bottom surface of said recess, said taper angle being set in the range of 30 to 75 degrees.

6. The wafer processing method according to claim 4, wherein a dicing tape attaching step includes attaching said dicing tape to said bottom surface of said recess, said taper surface and said annular reinforcing portion of said wafer.

7. The wafer processing method according to claim 1, wherein said dividing step includes lowering said cutting blade toward said wafer to start cutting of said wafer at one end of said predetermined division line at a first point where said taper surface meets said bottom surface of said recess, and raising said cutting blade from said wafer to stop cutting of said wafer at the other end of said predetermined division line at a second point where said taper surface meets said bottom surface of said recess.

8. A wafer processing method for processing a wafer having a front side and a back side opposite to said front side, said front side of said wafer having a device area and a peripheral marginal area surrounding

said device area, a plurality of crossing division lines being formed on said front side of said wafer to thereby define a plurality of separate regions in each of which a plurality of devices are formed, said wafer processing method comprising:

a back grinding step of grinding said back side of said wafer in a central area corresponding to said device area of said front side to thereby form a recess having a bottom surface in said central area of said back side and also form an annular reinforcing portion surrounding said recess;

a dividing step of cutting said wafer along said division lines from said front side of said wafer by using a cutting blade to thereby divide said wafer into a plurality of individual device chips each corresponding to said devices;

said dividing step including the steps of relatively moving said cutting blade and said wafer along a predetermined one of said division lines and lowering said cutting blade toward said wafer to start cutting of said wafer at one end of said predetermined division line radially inside the outer circumference of said wafer, and raising said cutting blade from said wafer to stop cutting of said wafer at the other end of said

predetermined division line radially inside the outer circumference of said wafer,

wherein said dividing step includes lowering said cutting blade toward said wafer to start cutting of said wafer at an outer edge of said recess and raising said cutting blade from said wafer to stop cutting of said wafer at an opposing outer edge of said recess.

9. The wafer processing method according to claim 1, wherein an annular area along an outer circumference of said wafer is not cut by said cutting blade in said dividing step.