

Description

The invention relates to a transistor circuit comprising:

- an emitter-coupled transistor pair comprising a first and a second transistor,
- a third transistor to compensate for the base-current of the first transistor, which third transistor has its collector-emitter path arranged in series with the collector-emitter path of the second transistor, the base of the third transistor being coupled to the base of the first transistor.

Such a transistor circuit is known from IBM Technical Disclosure Bulletin, Vol. 16, No. 5, October 1973, pages 1657-1658 and is shown in Fig. 1a.

In gyrator-capacitor filters, which are described *inter alia* in "Integration of Analog Filters in a Bipolar Process", IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 4, August 1982, pp. 713-722, the emitter-coupled transistor pair is an important element, which is often referred to as a transconductance circuit or transconductor, the voltage difference between the bases of the transistors of one pair being converted into two balanced output currents. By coupling two emittercoupled transistor pairs a gyrator can be formed. The quality and precision of the gyrator-capacitor filters depends *inter alia* on the manner in which a gyrator loads the other filter components, such as capacitors, resistors and other gyrators. In the ideal case a gyrator comprises two transconductors each having an infinitely high input impedance, which transconductors neither load one another nor the filter components coupled to the gyrator. A high input impedance can be obtained by base-current compensation as used in the prior art transistor circuit as shown in said IBM Technical Disclosure.

In this known circuit the a.c. components in the base currents of the first and the second transistor of the transistor pair are equal but in phase opposition. The d.c. components are also equal but in phase. By arranging the collector-emitter path of the third transistor in series with the collector-emitter path of the second transistor a current is obtained which is in phase with the base-current of the second transistor. By coupling this current to the base of the first transistor the a.c. component in the base-current of the first transistor is compensated for, while the d.c. component, which is of no further influence for the signal gain, is doubled. Thus, the a.c. impedance at the base of the first transistor is high at the expense of a doubled d.c. component. However, in gyrator-capacitor filters this doubled base direct current of a compensated transistor can be allowed for simply in designing the gyrator-bias circuits.

If required, the base-current of both the first and the second transistor of the emitter-coupled transistor pair can be compensated for by the known method as shown in Fig. 1b. In gyrator-capacitor filters the gyrators and the filter components coupled thereto are generally not floating but have one end coupled to a reference voltage. In that case it is not necessary to provide base-current compensation for those bases of the emitter-coupled transistor pairs which are coupled to the reference potential. This is because their alternating currents do not load other gyrators or filter components and therefore do not affect the quality and accuracy of the gyrator-capacitor filter.

A gyrator with the known base-current compensation for gyrator-capacitor filters may be obtained by adding to the known transistor circuit

- an emitter-coupled transistor pair comprising a fourth and a fifth transistor,
- a sixth transistor, whose collector-emitter path is arranged in series with the collector-emitter path of the fifth transistor and which has its base coupled to the base of the fourth transistor,

the base of the second transistor being coupled to the collector of the fourth transistor, the base of the first transistor being coupled to the collector of the sixth transistor, the base of the fourth transistor being coupled to the collector of the first transistor, and the base of the fifth transistor being coupled to the collector of the third transistor. A gyrator of this type is shown in Fig. 2a.

In this gyrator compensation is provided only for the base-currents of the first and the fourth transistor in the two emitter-coupled transistor pairs. The two other bases of the transistor pairs can be coupled to a reference voltage and therefore require no compensation. A gyrator-capacitor filter is obtained by arranging a suitable impedance between the bases of the first and the second transistor and between the bases of the fourth and fifth transistor. For example, if a capacitor is selected for these impedances an LC resonator is obtained whose selectivity is very high on account of the compensation of the base-currents of the first and the fourth transistor.

As known from said IBM Technical Disclosure and shown in Fig. 2b, signal points whose operating potentials are too far apart, should be coupled via a level-shifting circuit, such as for example LS3 between the collector of the sixth transistor T3B and the base of the first transistor T1A. It is an object of the invention to provide a transistor circuit having two emitter-coupled transistor pairs to form a gyrator which simply combines base-current compensation and level-shifting.

According to the invention a transistor circuit of the type defined in the opening paragraph is char-

acterized in that the transistor circuit further comprises

- a fourth transistor having its collector-emitter path arranged in series with the collector-emitter path of the third transistor,
- an emitter-coupled transistor pair comprising a fifth and a sixth transistor,
- a diode-connected seventh transistor and a diode-connected eighth transistor, whose collector-emitter paths are arranged in series with the collector-emitter path of the sixth transistor,
- the bases of the third and the seventh transistor being coupled to each other and the bases of the fourth and the eighth transistor being coupled to each other,
- the base of the first transistor being coupled to the collector of the sixth transistor and the base of the fifth transistor being coupled to the collector of the first transistor, and
- the bases of the second and the sixth transistor and the collectors of the fourth and the fifth transistor being coupled to a reference-voltage terminal.

By coupling the bases of the second and the sixth transistor to a suitable reference voltage base-current compensation must be provided only for the first and the fifth transistor. The base-emitter junction of the seventh transistor functions as a level shifter for the base-current of the third transistor. The collector-emitter path of a fourth transistor is arranged in series with the third transistor and its base-current is transferred to the base of the first transistor via the base-emitter junction of the eighth transistor, which serves as a level shifter, and via the seventh transistor. In this way the base-current of the first transistor is compensated for twice. However, the base-current of the fifth transistor is not compensated for. When this gyrator is employed in a gyrator-capacitor filter a first and a second impedance are coupled to the base of the first and that of the fifth transistor respectively. The surplus of compensation current for the base-current of the first transistor flows to the first impedance, the deficient compensation current for the base-current of the fifth transistor being taken from the second impedance. The surplus and the deficiency thus compensate for one another wholly or at least partly. This gyrator does not load the filter components or at least to a smaller extent than a gyrator comprising similar transistor pairs without base-current compensation.

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings, in which

Fig. 1 shows four transistor circuits with known base-current compensation,

Fig. 2 shows two circuit diagrams to explain the operation of a transistor circuit in accordance with the invention, and

Figs. 3 and 4 show circuit diagrams of embodiments of a transistor circuit in accordance with the invention.

Fig. 1a shows an emitter-coupled transistor pair T1, T2 with known base-current compensation. The emitters of T1 and T2 are coupled to a bias-current source, whose current is equally divided between the transistors T1 and T2, so that a quiescent current I_c flows in the collectors of both transistors T1 and T2. The base of the transistor T1 is coupled to a terminal 1 and the base of the transistor T2 is coupled to a terminal 2. A voltage difference is applied across the terminals 1 and 2, causing base-currents to flow in the transistors T1 and T2. As a result of the symmetry of the transistor pair T1, T2 the a.c. components i_b in these currents are in phase opposition. Conversely, the d.c. components I_b are in phase. A current $I_b + i_b$ flows in the base of the transistor T1 and a current $I_b - i_b$ flows in the base of the transistor T2. In the transistors T1 and T2 the a.c. components i_b and $-i_b$ are amplified by a specific current-gain factor, resulting in balanced collector currents i_c and $-i_c$ respectively. The collector current i_c is available on the terminal 3, which is coupled to the collector of the transistor T1. The collector-emitter path of the transistor T3 is arranged in series with the collector-emitter path of the transistor T2. The emitter of the transistor T3 is coupled to the collector of the transistor T2 and the collector of the transistor T3 is coupled to a terminal 4. The collector current $-i_c$ of T2 flows through the transistor T3 and is available on the terminal 4. The a.c. component in the base of the transistor T3 is substantially equal to that in the base of the transistor T2. The same applies to the d.c. component of the base-current of the transistor T3. Consequently, the total current in the base of the transistor T3 is substantially equal to $I_b - i_b$. The base of the transistor T3 is coupled to the base of the transistor T1. As a result of this coupling the a.c. component $+i_b$ in the base current of the transistor T1 is compensated for by the a.c. component $-i_b$ in the base-current of the transistor T3. Thus, only a d.c. component $2I_b$ will flow in terminal 1. As a result of the compensation for the a.c. component the a.c. impedance, seen at the terminal 1, is high. If required, the a.c. component in the base-current of the transistor T2 can be compensated for in the same way as shown in Fig. 1b, by arranging a transistor in the collector line of the transistor T1. This method of compensation results in an emitter-coupled transistor pair with a high a.c. impedance at both the terminals 1 and 2.

Figs. 1c and 1d show modifications of emitter-coupled transistor pairs with base-current compensation. In these Figures corresponding reference numerals have the same meaning as in Fig. 1a. In the transistor pair shown in Fig. 1c the emitters are coupled to a resistor. In Fig. 1d the collectors and the bases of two emitter-coupled transistor pairs are interconnected. The relative emitter area of each of the transistors is given in brackets. Such a configuration provides a more linear voltage-to-current conversion than the transistor pair of Fig. 1a and is used in the circuit of Fig. 4.

A gyrator comprises two mutually coupled voltage-to-current converters, also referred to as transconductors. The voltage-to-current converter is then constituted by an emitter-coupled transistor pair to convert the voltage difference on the bases of the transistors of the pair into balanced collector currents. Such voltage-to-current converters require a high input impedance in order to obtain a loss-free gyrator. A gyrator which is not loss-free may also be used to realize a specific gyrator filter but presents a load to the filter components connected to the gyrator. Generally, the gyrator filter will then operate less accurately than anticipated. In particular, if very selective gyrator filters are needed it is essential that the gyrator does not load the filter components. The emitter-coupled transistor pairs shown in Fig. 1 are therefore very suitable as voltage-to-current converters in gyrator filter circuits because of their high input impedance.

Fig. 2a shows the a.c. diagram of a gyrator comprising two identical emitter-coupled transistor pairs A and B with base-current compensation, which each by way of example are constructed as the modification in Fig. 1a. The reference numerals have the same meaning as in Fig. 1a, but to distinguish between the two pairs A and B the corresponding parts of the pairs A and B have reference numerals suffixed with A and B. The terminals 3A and 1B, 1A and 4B, 2A and 3B and 4A and 2B are coupled to each other, so that the transistor pairs A and B together act as a gyrator. An impedance Z1 is connected across the terminals 1A and 2A and an impedance Z2 is connected across the terminals 3A and 4A. If Z1 and Z2 are capacitors the gyrator-filter circuit will behave as an LC parallel resonant circuit between the terminals 1A and 2A. Fig. 2a further shows that the impedances Z1 and Z2 may have one of their ends connected to a suitable reference voltage, for example earth. For this situation the circuit of Fig. 2a is shown in Fig. 2b in such a way that it is easier to see which terminals of the gyrator circuit are coupled to the reference voltage. It will be seen that the transistors T1A and T1B load the filter components Z1 and Z2, so that base-current compensation must be provided for these transistors T1A and

T1B only. Coupling the bases of the transistors T3A and T3B to the bases of the transistors T1A and T1B respectively and terminal 4B to terminal 1A requires the use of level shifters, for example diode-connected transistors, which are referenced LS1, LS2 and LS3. This is because the signal points to be coupled are at different operating potentials.

Fig. 3 shows the a.c. diagram of a transistor circuit in accordance with the invention, which combines the base-current compensation and the level shifters shown in Fig. 2b. The gyrator comprises two emitter-coupled transistor pairs DP1, comprising the transistors T1, T2, and DP2, comprising the transistors T5 and T6. The transistor T1 has its base coupled to the collector of the transistor T6 and the transistor T5 has its base coupled to the collector of the transistor T1. The bases of the transistors T1 and T5 are coupled to a suitable reference voltage via the impedances Z1 and Z2 respectively. The bases of the transistors T2 and T6 and the collectors of the transistors T2 and T5 are also coupled to the reference voltage. This again results in a gyrator-filter circuit whose operation is basically identical to that of the circuit shown in Fig. 2. The collector-emitter paths of the transistors T3 and T4 are arranged in the collector line of the transistor T2. Two diode-connected transistors T7 and T8 are arranged in the collector line of the transistor T6 and have their bases coupled to the bases of the transistors T3 and T4. In accordance with the principle as set forth in the explanation of the base-current compensation used in the circuit shown in Fig. 1a the base of the transistor T3 is coupled to the base of the transistor T1, level shifting being provided by the transistor T7. By means of the transistor T4, however, another compensation current is generated which is also applied to the base of the transistor T1 via a transistor T8, which again functions as a level shifter, and the transistor T7. An alternating current $+ibA$ in the base-current of the transistor T1 results in an alternating current $2ibA$ in the emitter line of the transistor T7, which current divides into the base-current ibA to the transistor T1 and a current ibA which flows into the impedance Z1. In fact, this provides over compensation for the base-current of the transistor T1. However, the base-current ibB of the transistor T5 is not compensated for by a transistor, corresponding to the transistor T3, in the collector line of the transistor T6. Consequently, a current ibB is sunk from the impedance Z2. Sourcing the current ibA to the impedance Z1 and sinking the current ibB from the impedance Z2 results on the average in the filter components Z1 and Z2 being hardly loaded by the gyrator if the currents ibA and ibB are substantially equal. But even in the case of unequal currents ibA and ibB a

load reduction is achieved as compared with a similar of the gyrator filter without base-current compensation.

In the compensation loop T1, T2, T3, T4, T8 and T7 instabilities may occur, for example owing to phase shifting in the impedance Z1. This causes the signal voltage on the base of the transistor T1 to increase. This signal voltage appears in amplified form but in phase opposition on the collector of the transistor T1. This amplified signal voltage is again amplified by the transistor pair T5, T6 but without any further phase shift. Thus, an inverted and amplified signal voltage will appear on the collector of the transistor T6, which counteracts the increasing signal voltage on the base of the transistor T1. The inverting loop gain from the base of the transistor T1 to the collector of the transistor T6 is several times higher than the non-inverting loop gain in the compensation loop. In this way any oscillation tendencies are suppressed effectively.

Fig. 4 shows the circuit diagram of an embodiment of the gyrator filter circuit as shown in Fig. 3, which also shows the bias means. In this Figure corresponding reference numerals denote the same elements as in Fig. 3. The transistors T1 to T8 are coupled similarly to those in the circuit shown in Fig. 3 and, by way of example, a capacitor C1 and a capacitor C2 have been selected for the impedances Z1 and Z2 respectively in the circuit shown in Fig. 3. The base-collector junctions of the transistors T12, T11, T15 and T16 are arranged in parallel with the base-collector junctions of the transistors T2, T1, T5 and T6 respectively. The emitters of the transistor pairs T1-T2, T11-T12, T5-T6 and T15-T16 are connected to a negative power supply terminal 1 by means of NPN current-source transistors T20, T21, T22 and T23 respectively and a resistor arranged in the emitter lines of each of these current-source transistors. The emitter areas of the transistors T12, T2, T1, T11 and of the transistors T15, T5, T6, T16 are in a ratio of 4 : 1 : 4 : 1 to one another. This provides a more linear voltage-to-current conversion in the emitter-coupled transistor pairs DP1 and DP2. The bases of the transistors T12, T2, T6 and T16 are coupled to a reference-voltage terminal 3, to which a suitable reference voltage VR is applied. The capacitors C1 and C2 also have one end connected to this reference-voltage terminal. The collectors of the transistors T4, T1 and T8 are connected to a positive power-supply terminal 5 via PNP current-source transistors T30, T32 and T33 respectively and a resistor arranged in the emitter line of each of said current-source transistors. The signal voltage on the base of the transistors T1 and T5 is available in buffered form on the emitters of the transistors T27 and T28 respectively, whose bases are connected to the bases of the transistors T1

and T5 respectively, whose collectors are connected to the reference-voltage terminal 3 and whose emitters are connected to the negative power-supply terminal 1 via NPN current-source transistors T24 and T25 respectively and a resistor arranged in the emitter line of each of said current source transistors. The collectors of the transistors T5, T15, T27 and T28 are connected to the reference-voltage terminal 3. The bias current for the transistors T15 and T5 is supplied to the reference-voltage terminal by a PNP current-source transistor T31, which has its emitter connected to the positive power-supply terminal via a resistor. The collector of the transistor T31 is connected to the collector of the transistor T4 and, via two diode-connected transistors T13 and T14, to the reference voltage terminal 3. The bases of the PNP and NPN current-source transistors are connected to the terminals 4 and 2 respectively, to which suitable bias voltages V_{PNP} and V_{NPN} respectively are applied. The a.c. component in the transistors T2 and T12 flows to the reference-voltage terminal 3 via the transistors T3, T4, T14 and T13. The a.c. component in the transistors T1 and T11 flows to the reference-voltage terminal 3 via the capacitor C1. As their two a.c. components are in phase opposition the voltage source connected to the reference-voltage terminal 3 is not loaded by these alternating currents. In the circuit diagram the circuit for these currents is indicated in broken lines. The a.c. component in the transistors T6, T16 flows to the reference-voltage terminal 3 via the capacitor C2. However, again the opposite a.c. component in the transistors T15, T5 presents an opposite load to the reference-voltage terminal 3. The circuit for this a.c. component is also indicated in broken lines. On account of the capacitors C1 and C2 the gyrator filter behaves as an LC parallel resonator and can be employed as a band-pass filter. For this purpose the base of the transistor T6 is connected to an input terminal 6 via resistor R11 and to the reference-voltage terminal 3 via a resistor R10. The signal VIN to be filtered is then applied to the input terminal 6. The output signal VOUT is available on an output terminal 7 connected to the emitter of the buffer transistor T27. Since the input impedances at the bases of the buffer transistors T27 and T28 are inherently very high, it is not necessary to compensate for the base-currents of the transistors T27, T28. In principle, the collector currents of the transistors T27 and T28 are not balanced. Nevertheless the resulting load presented by these currents to the reference voltage terminal 3 is small. Therefore, the entire circuit presents a very small a.c. load to the reference voltage terminal 3. Thus, it is simpler to keep the reference voltage VR free from interference.

Claims

1. A transistor circuit comprising:

- an emitter-coupled transistor pair (DP1) comprising a first (T1) and a second (T2) transistor, 5
- a third transistor (T3) to compensate for the base-current of the first transistor (T1), which third transistor (T3) has its collector-emitter path arranged in series with the collector-emitter path of the second transistor (T2), the base of the third transistor (T3) being coupled to the base of the first transistor (T1), characterized in that the transistor circuit further comprises: 10
- a fourth transistor (T4) having its collector-emitter path arranged in series with the collector-emitter path of the third transistor (T3), 20
- an emitter-coupled transistor pair (DP2) comprising a fifth (T5) and a sixth (T6) transistor, 25
- a diode-connected seventh transistor (T7) and a diode-connected eighth transistor (T8), whose collector-emitter paths are arranged in series with the collector-emitter path of the sixth transistor (T6), 30
- the bases of the third (T3) and the seventh (T7) transistor being coupled to each other and the bases of the fourth (T4) and the eighth (T8) being coupled to each other, 35
- the base of the first transistor (T1) being coupled to the collector of the sixth transistor (T6) and the base of the fifth transistor (T5) being coupled to the collector of the first transistor (T1), and 40
- the bases of the second (T2) and the sixth (T6) transistor and the collectors of the fourth (T4) and the fifth (T5) transistor being coupled to a reference terminal. 45

Patentansprüche

1. Transistorschaltung, die

- ein emittergekoppeltes Transistorpaar (DP1) mit einem ersten (T1) und einem zweiten (T2) Transistor umfaßt
- sowie einen dritten Transistor (T3) zur Kompensation des Basisstroms des ersten Transistors (T1), wobei die Kollektor-Emitter-Strecke des dritten Transistors (T3) in Reihe mit der Kollektor-Emitter-Strecke des zweiten Transistors (T2) geschaltet ist, und wobei die Basis des dritten Transistors (T3) mit der Basis des ersten Transistors (T1) gekoppelt ist, 50
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dadurch gekennzeichnet, daß die Transistorschaltung außerdem folgendes umfaßt:

- einen vierten Transistor (T4), dessen Kollektor-Emitter-Strecke in Reihe mit der Kollektor-Emitter-Strecke eines dritten Transistors (T3) geschaltet ist,
- ein emittergekoppeltes Transistorpaar (DP2) mit einem fünften (T5) und einem sechsten (T6) Transistor, sowie
- einen als Diode geschalteten siebten Transistor (T7) und einen als Diode geschalteten achten Transistor (T8), deren Kollektor-Emitter-Strecken mit der Kollektor-Emitter-Strecke des sechsten Transistors (T6) in Reihe geschaltet sind,
- wobei die Basen des dritten (T3) und des siebten (T7) Transistors miteinander gekoppelt sind und die Basen des vierten (T4) und des achten (T8) Transistors miteinander gekoppelt sind,
- die Basis des ersten Transistors (T1) mit dem Kollektor des sechsten Transistors (T6) und die Basis des fünften Transistors (T5) mit dem Kollektor des ersten Transistors (T1) gekoppelt ist und
- die Basen des zweiten (T2) und des sechsten (T6) Transistors und die Kollektoren des vierten (T4) und des fünften (T5) Transistors mit einer Bezugsspannungsklemme gekoppelt sind.

Revendications

1. Circuit à transistors comportant:

- une paire de transistors à émetteurs couplés (DP1) comportant un premier (T1) et un deuxième (T2) transistor,
- un troisième transistor (T3) pour compenser le courant de base du premier transistor (T1), troisième transistor (T3) qui a son trajet de collecteur-émetteur monté en série avec le trajet de collecteur-émetteur du deuxième transistor (T2), la base du troisième transistor (T3) étant couplée à la base du premier transistor (T1), caractérisé en qu'il comporte en outre:
- un quatrième transistor (T4) ayant son trajet de collecteur-émetteur disposé en série avec le trajet de collecteur-émetteur du troisième transistor (T3),
- une paire de transistors à émetteurs couplés (DP2) comportant un cinquième (T5) et un sixième (T6) transistor,
- un septième transistor monté en diode (T7) et un huitième transistor monté en diode (T8) dont les trajets de collecteur-



émetteur sont connectés en série avec le trajet de collecteur-émetteur du sixième transistor (T6),

- les bases du troisième (T3) et du septième (T7) transistor étant couplées entre elles et les bases du quatrième (T4) et du huitième (T8) transistor étant couplées entre elles, 5
- la base du premier transistor (T1) étant couplée au collecteur du sixième transistor (T6) et la base du cinquième transistor (T5) étant couplée au collecteur du premier transistor (T1) et 10
- les bases du deuxième (T2) et du sixième (T6) transistor et les collecteurs du quatrième (T4) et du cinquième (T5) transistor étant couplées à une borne de référence. 15

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