"A NONVOLATILE MEMORY".

The present invention relates to a non-volatile memory which has a high density of integration and uses a low operating voltage.

In general, nonvolatile memories used as EEPROMs (Electrically Erasable and Programable ROMs) or EAROMs (Electrically Alterable ROMs) are constructed of MISFETs (Metal-Insulator-Semiconductor Field Effect Transistors) which are broadly classified into two types; the FLOTOX (Floating Tunnel Oxide) type belonging to the floating gate type, and the MNOS (Metal-Nitride-Oxide-Semiconductor) type. The former has a control gate electrode for control, and a floating gate electrode for storing charges. The charges to be stored in the floating gate are injected thereinto by passing them through a thin oxide film on a drain region owing to the modified Fowler-Nordheim tunneling (MFN tunneling) or the direct tunneling (hereinafter, simply referred to as "tunneling"). On the other hand, the latter has its gate insulator

film formed of a double-layer structure consisting of a silicon dioxide film (SiO_2 film) and a silicon nitride film (Si_3N_4 film) deposited thereon. Charges are tunneled through the SiO_2 film, in order to be injected and stored in those traps within the Si_3N_4 film which are formed near the boundary of the two insulator films.

However, the respective semiconductor devices present certain problems which hamper enhanced densities of integration and lower operating voltages for the memories.

The former is advantageous in data retention. In order to ensure the retention of the charges, however, a thick inter-layer insulator film of about 1000Å as used in conventional EPROM (Erasable and Programable ROM) needs to be interposed between the floating gate and the control gate. The thickness is required for preventing the stored charges of the floating gate from leaking to the control gate. It is therefore impossible to simply apply scaling-down for the purpose of enhancing the density of integration. Besides, in the former, in constructing memory cells, the registration between the drain regions previously formed and the floating gates

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becomes a serious problem. Since an allowance for the alignment is required, the fine processing of a pattern attendant upon an enhanced density of integration becomes very difficult.

With the latter, the alignment between gates and drain regions is not a problem. In addition, the latter is advantageous in endurance. However, the scaling-down to the end of enhancing the density of integration cannot be simply performed, either. When the Si_3N_4 film constituting the gate insulator film becomes thinner than a certain value or about 200 Å by reason of the scaling-down, there arises the phenomenon that the charges are emitted to a gate electrode. Therefore, the retention becomes a serious problem. In this manner, the reduction of the thickness of the Si_3N_4 film, namely, the scaling-down is limited, which forms obstacles to enhancing the density of integration and the lowering of the operating voltage.

It is an object of the present invention to provide a nonvolatile memory which can attain a higher density of integration and lower writing and erasing voltages while holding the retention of charges favourable.

According to the present invention there is provided a nonvolatile memory having a field effect transistor for use as a memory element, said field effect transistor including:

(a) a semiconductor body which includes a semiconductor region of a first conductivity type;

(b) a gate insulator film which is formed on said semiconductor region, and which consists of a first gate insulator film and a second gate insulator film formed thereon, said second gate insulator film having a dielectric constant different from that of said first gate insulator film:

(c) a floating gate electrode for storing charges, which is formed on said gate insulator film;

(d) a control gate electrode which is formed over said floating gate electrode;

(e) an inter-layer insulator film which is arranged between said floating and control gate electrodes; and

(f) semiconductor regions of a second conductivity type which are formed within the first-mentioned semiconductor region, and which are located on both sides of said floating and control gate electrodes.

The charges for storing data are retained in such a way that the floating gate is charged. Since the

centroid of the charges lies within the floating gate electrode, the upper-layer insulator film can be thinned.

The lower layer of insulator film may be a SiO_2 film, while the upper layer of insulator film may be a Si_3N_4 film. The thickness of the upper-layer insulator film is set to be at least 40 Å and at most 100 Å. Polycrystalline silicon is used as the material of the floating gate as well as the control gate.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figures 1A and 1B are diagrams for explaining a charge centroid in an MNOS type FET, in which Figure 1A is a graph of the characteristic, and Figure 1B is a model-like sectional view of the NMOS type FET.

Figure 2 is a sectional view showing the structure of a first preferred form of FET;

Figure 3 is a graph illustrating the relationship between the gate voltage V_G and drain-source current I_{DS} of the FET shown in Figure 2;

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Figure 4 is a sectional view showing the structure of the essential portions of the second form of FET,

Figure 5 is a sectional view showing the strucutre of the essential portions of a third form of FET;

Figure 6 is a plan view of an embodiment of a preferred form of nonvolatile memory;

Figure 7 is a sectional view taken along line VII - VII of the nonvolatile memory shown in Figure 6; and

Figure 8 is a memory circuit diagram of the nonvolatile memory shown in Figure 6.

Figura 1A illustrates the relationship between the charge centroid and the quantity of charges Q injected into traps within an Si_3N_4 film 5 in a FET of an MNOS structure shown in Figure 1B, the result having been obtained by experiment carried out by us. Referring to Figure 1B, a gate insulator film 3 underlying a gate electrode 2 consists of a silicon dioxide film (SiO_2 film) 4 being 23 Å thick and the silicon nitride film (Si_3N_4 film) 5 being 520 Å thick.

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The charge centroid is found in the following way. It is assumed that all the injection charges Q exist in a plane which is parallel to the boundary between the SiO_2 film 4 and the Si_3N_4 film 5 and which is spaced a certain distance $\underline{d}$ from the boundary. Meanwhile, the capacitance C of a MIS capacitor is evaluated from the injection charges Q and a potential V generated in the MIS capacitor of the gate electrode portion by the charges ($C = Q/V$). The distance $\underline{d}$ is evaluated from the capacitance C, the area S of the gate electrode portion, and the dielectric constance ε which is substantially stipulated by the two insulator film ($d = \varepsilon.S/C$). This distance $\underline{d}$ is the charge centroid.

In Figure 1A, the abscissa represents the distance $\underline{d}$ (in Å) which is taken towards the gate 2 (upwards) from the boundary between the SiO_2 film 4 being the lower-layer insulator film and the Si_3N_4 film 5 being the upper-layer insulator film, while the axis of ordinates represents the value of the injection charge quantity Q which is converted into the voltage V. This voltage value may be considered as being a value at which the charge injection quantity Q can vary the threshold voltage

of the FET having the MNOS structure shown in Figure 1B. The experiment conducted by us has revealed the following. As illustrated in Figure 1A, the charge centroids formed by the trapped charges are distributed in a region of about 40 Å to about 110 Å from the boundary of the SiO_2 film 4 and the Si_3N_4 film 5. In particular, the charge centroids often exist in the part of the Si_3N_4 film distance about 100 Å from the boundary, and more injection charges are trapped here. The charge centroids scarcely exist in a region within 40 Å or a region distant more than 110 Å, from the boundary.

Figure 2 shows a first preferred form of the FET constructed on the basis of the above experiment so that a charge centroid may exist within a floating gate arranged anew, not in the Si_3N_4 film. The FET includes a P-type semiconductor region 10 which is constructed of a P-type silicon semiconductor substrate as a semiconductor body. The P-type substrate 10 is formed with a field oxide film 11 by the thermal oxidation of the surface thereof, to define regions for forming elements. In each region N^+-type regions 12 and 13 form the source and drain regions.

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A SiO_2 film 14 which is about 20 Å thick is formed on the surface of the element forming region by the thermal oxidation of the substrate. The SiO_2 film 14 may have a thickness through which charges can be tunneled, and which can assume a value of 15 Å - 50 Å. In order to raise the efficiency of injection, a thinner film is better. In order to form a film of good quality at high available percentage, a value of about 20 Å is preferable. A Si_3N_4 film 15 which is about 60 Å thick is formed in the lower part of a gate electrode portion by the CVD (Chemical Vapour Deposition) technique The Si_3N_4 film 15 may be so thick that the charge centroid can exist within a floating gate. While a value of 40 Å - 110 Å can be taken, a value of approximately 50 Å - 100 Å is more reliable. A thinner film is more preferable for thinning a gate insulator film. The floating gate 16 being a first electrode which is made of polycrystalline silicon about 20 Å - 100 Å thick is formed on the Si_3N_4 film 15, to form a structure similar to the so-called MNOS structure. The floating gate 16 should preferably be thin. With the thin floating gate, the charges are difficult to move within this gate. In the case where the gate insulator film has pinholes, this measure can reduce charges to leak therethrough,

resulting in improved data retention. On the floating gate 16, a SiO_2 film 17 as an inter-layer insulator film is formed to a comparatively great thickness of about 1000 Å. A control gate 18 being a second electrode which is made of polycrystalline silicon is formed on the SiO_2 film 17. The FET also includes a PSG (phosphosilicate glass) film 19, and aluminium wiring 20 which is electrically connected to the N^+-type regions 12 and 13 through contact holes 21a and 21b. The N^+-type regions 12, 13 are formed in self-alignment with the gate electrode by ion implantation after the parts up to the control gate 18 have been completed. A final passivation film 22 is formed over the top, the film being a SiO_2 film formed by the CVD technique.

The FET is formed such that the gate insulator film or tunnel region 23 located wholly underneath the floating gate 16 is put into the double structure consisting of the SiO_2 film 14 of the lower-layer insulator film and the Si_3N_4 film 15 of the upper-layer insulator film whose dielectric constants differ from each other. The thickness of the Si_3N_4 film of the upper layer is 60 Å, which is smaller than the distance of the charge centroid. The injection charge quantity is set in relation to the

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Si_3N_4 film 15 in order that the charge centroid may lie within the floating gate. In addition, the thickness of the complete gate insulator film 23 comprising the upper and lower layers is as thin as 80 Å.

When, in the FET shown in Figure 2, a positive voltage is applied to the control gate 18 and the P-type substrate 10 is connected to earth potential GND, electrons tunnel through the SiO_2 film 14 from the P-type substrate side, and the floating gate is charged. At this time, either one of the N^+-type regions 12, 13 is connected to earth potential GND, and the other is held in the floating state. The injection of the electrons is based on the same action as that of the above referred to MNOS structure. The above described embodiment is advantageous because the gate insulator film degrades less than in the conventional floating gate type EEPROM. Since, in the present example, the Si_3N_4 film 15 is rendered 60 Å thick, the centre of the traps of the charges (that part corresponding to the charge centroid which traps the most charges) lies within the thickness of the floating gate 16, so that the charges are stored in the floating gate 16. The charged region is the same as in the prior-art

floating gate type. Accordingly, the leakage of the charges from the Si_3N_4 film to the gate electrode is slight, and the retention is favourable, as in the conventional MNOS type EEPROM. Even when the thickness of the gate insulator film 23 decreases with scaling-down, no problem arises with regard to the retention.

Trapping the charges can be done in the same manner as in the MNOS structure. Owing to the decreases of the thicknesses of the SiO_2 film 14 and the Si_3N_4 film 15, the voltage which is applied to the control gate 18 at the injection can be lowered without affecting the injection efficiency. According to our experiments, the tunneling of charges sufficient for storing data was possible at about 10 V. In forming the N^+-type regions 12, 13, the floating gate 16, the problem of the alignment between the N^+-type regions and the floating gate does not arise. This facilitates fining the pattern, namely, enhancing the density of integration, in cooperation with the scaling-down referred to above.

In order to write data into the floating gate 16, in other words, to inject charges thereinto, a positive voltage may be applied to the control gate 18, with the P-type substrate 10

connected to earth potential GND. Conversely, in order to erase data written in the floating gate 16, in other words, to emit trapped charges, the control gate 18 may be connected to earth potential GND, with a positive voltage applied to the P-type substrate 10. Thus, the charges are emitted to the P-type substrate 10. At this time, the potential of the N^+-type regions 12, 13 may be any, and it is rendered equal to that of the P-type substrate 10 by way of example.

Written data is read out as follows. The current - voltage characteristics of the FET shown in Figure 2 are set as indicated by "1" and "0" in Figure 3 when the charges are not trapped in the floating gate 16 and when they are trapped therein, respectively. The FET shown in Figure 2 is set at the depletion mode having a threshold voltage of, e.g. -3 V or so beforehand, whereupon it is put into the enhancement mode when the threshold voltage is raised to, e.g., +3 V or so by the writing of the data, namely, the trapping of the charges. In Figure 3, the abscissa V_G represents the voltage which is applied to the control gate 18, while the ordinate I_{DS} represents the current which flows between the source region and the drain region, that is, between the N^+-type regions 12 and 13.

By utilizing such difference of the threshold voltages, the potential of the control gate 18 is made, e.g. O V, whereby the data can be read out. Thus, the number of readable times is increased. It is possible to know the two states in which the FET having the potential of the control gate set at O V is conductive (state of "1") and is non-conductive (state of "O"). The FET can accordingly be exploited as a nonvolatile memory element having the data of one bit.

Figure 4 shows a second embodiment of a FET, and only illustrates the structure of the gate portion. The other parts which are not shown are the same as in Figure 2. In the second embodiment, the gate insulator film 23 is held between the floating gate 16 and the semiconductor substrate 10 as in the previous embodiment and is formed into the double structure out of the SiO_2 film 14 being the lower-layer insulator film and the Si_3N_4 film 15 being the upper-layer insulator film. In this construction it should be noted that an inter-layer insulator film 24 lies between the floating gate 16 and the control gate 18 and is formed as a double structure. The inter-layer insulator film 24 is composed of a lower-layer Si_3N_4 film 25, and an upper-layer SiO_2 film 26

formed by the thermal oxidation of the surface of the former. The respective films are 60 Å and 20 Å thick. These films should preferably be thin. The Si_3N_4 film 25 can assume a value of 40 Å - 110 Å, and the SiO_2 film 26 a value of 15 Å - 50 Å. However, for reasons to be stated below, the thicknesses of the films 25 and 26 should desirably be respectively equal to the Si_3N_4 film 15 and the SiO_2 film 14 which constitute the gate insulator film.

When the inter-layer insulator film 24 is thus constructed, the whole thickness thereof can be reduced to a size smaller than the thickness of the inter-layer insulator film constructed of the SiO_2 film 17 alone as shown in Figure 2. Further, in spite of the thin inter-layer insulator film, the emission of charges from the floating gate 16 to the side of the control gate 18 can be effectively prevented. Thus, the data retention is substantially improved. This is based on the fact that charges having leaked from the floating gate 16 are captured by the Si_3N_4 film 25 which is prone to form the trap centre, and that the leakage of charges from the Si_3N_4 film to the control gate 18 is prevented by the SiO_2 film 26.

Although the SiO_2 film 26 is as thin as 20 Å, it does have sufficient thickness in order to prevent the charge leakage from the Si_3N_4 film 25. This structure is effective for thinning the gate portion, and becomes more advantageous in the fine processing.

Since, in this structure, the two insulator films 23 and 24 underlying and overlying the floating gate 16 have approximately equal thicknesses, an electric field intensity in the floating gate 16 becomes about one half of the voltage applied to the control gate 18. Therefore, the efficiency of the tunneling of charges can be enhanced. Thus, when the FET is used as a memory element, the writing voltage can be reduced. For example, when a voltage of 5 V is applied to the control gate 18, a potential which appears on the floating gate 16 becomes 2.5 V. In this case, charges sufficient for raising the threshold voltage of the order of several V can be injected, so that the FET can be satisfactorily used as the memory element. Of course, the emission of charges can be similarly effected with a low voltage. The way in which the voltages are applied to the respective regions of the FET in the writing and erasing modes

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are the same as in the example of the first embodiment of the FET.

Figure 5 shows a third embodiment of the FET. This example is such that, between the Si_3N_4 film 25 of the inter-layer insulator film 24 and the floating gate 16 in the FET of Figure 4, an SiO_2 film 27 exists which is formed at a thickness of 20 Å by thermal oxidation of the floating gate 16. In all other respects the third embodiment of the FET is the same as in the second embodiment of the FET. As a result, the inter-layer insulator film 24 has a triple structure composed of upper, middle and lower layers 26, 25 and 27 which are the SiO_2 film, the Si_3N_4 film and the SiO_2 film, respectively. Owing to the presence of the new SiO_2 film 27, it is possible to enhance the effect of preventing the leakage of charges from the floating gate 16 to the Si_3N_4 film 15.

With the second or third embodiment of the FET, writing and erasure at 5 V are permitted by optimizing the thicknesses of the Si_3N_4 films 15 and 25.

In the second and third embodiments described above, the Si_3N_4 films 15, 25 may well be replaced with Al_2O_3 films or hydroxynitride films. For the control gate 18 and the floating gate 16, films made of molybdenum Mo, tungsten W, or platinum Pt, may well be used instead of the polycrystalline silicon films. A film made of W or Pt is particularly advantageous for the floating gate 16. An Al film may be used for the control gate 18.

Figures 6 to 8 show a preferred embodiment of a nonvolatile memory constructed by employing the FETs of one of the above three embodiments of FETs as memory elements. Figures 6 and 7 are respectively plan and sectional views of the memory and Figure 8 is a circuit diagram of the memory. As shown in Figures 6 and 7, a P-type well 31 indicated by a dot-and-dash line, as a semiconductor region for forming memory cells, is formed in an N-type silicon semiconductor substrate 30 as a semiconductor body. A plurality of elongate regions 33 for forming the elements, the regions being isolated from one another by a field oxide film 32, are formed in the major surface of the silicon substrate. In each element forming region 33, N^+-type regions 34, 35 and 36 are formed at predetermined intervals in the lengthwise direction

of the element forming region 33, in self-alignment with word lines W_{S1}, ..., W_{M1},.... The adjacent N^+-type regions 34 and 35 with the word lines W_{S1}..... sandwiched therebetween serve as the source or drain regions of MOSFETs Q_{S1}, Q_{S2},..... which are switching elements. The adjacent N^+-type regions 35 and 36 with the word lines W_{M1}, ... sandwiched therebetween serve as the source or drain regions of FETs Q_{M1}, Q_{M2}, ... which are memory elements. The MOSFETs Q_{S1}, Q_{S2}, ... as the switching elements have the ordinary MOSFET structure consisting of a gate oxide film (SiO_2 film) 37 and a gate 38 of polycrystalline silicon formed thereon. The gate electrodes of the MOSFETs Q_{S1}, Q_{S2}, ... construct the word lines W_{S1}, W_{S2}, ... The FETs Q_{M1}, Q_{M2}, ... as the memory elements have the non-volatile memory device structure shown in Figure 4. In the gate electrodes of the FETs Q_{M1}, Q_{M2}, ..., the control gates construct the word lines W_{M1}, W_{M2}, ... The two sorts of FETs Q_{S1}, Q_{S2}, ... and Q_{M1}, Q_{M2}..... use the N^+-type regions 35 existing therebetween, as the common source or drain regions. Each memory cell is constructed in such a way that one pair of FETs Q_{S1} and Q_{M1}, Q_{S2} and Q_{M2}, ... are connected in series. The adjacent switching elements are adjacent memory elements constituting the different memory cells share the

N^+-type regions 34 and 36, respectively. An Al wiring lead 47 is connected to the shared N^+-type regions 34 and 36 through contact holes. As illustrated in Figure 6, the Al wiring lead 47 alternately connects the N^+-type regions 34 between the switching elements and the N^+-type regions 36 between the memory elements.

The devices formed as described above are connected as shown in Figure 8. Data lines $\overline{D_1}$, $\overline{D_2}$, ... are connected to the drains of the memory elements Q_{M1}, Q_{M2}, ... are connected to a writing circuit 50. Data lines D_1, D_2, ... which are connected to the sources of the switching elements Q_{S1}, Q_{S2}, ... are connected to a Y decoder 51 as well as a reading circuit 52. The word lines W_{S1}, W_{S2}, ... connected to the gates of the switching elements, and the word lines W_{M1}, W_{M2}, ... connected to the gates of the memory elements are respectively connected to an X decoder 53. In addition, the P-type well 31 which is the semiconductor region for forming the memory cells therein is connected to a well voltage circuit 54, the whole structure thus forming a memory circuit.

In injecting or emitting charges, a high voltage of, e.g. 20 V as in the prior art is not required.

In writing data, namely, in injecting charges, any desired one, e.g., $\overline{D_1}$ among the data lines $\overline{D_1}$, $\overline{D_2}$, ... is connected to 0 V by the writing circuit 50. The other data lines $\overline{D_2}$, ... are connected to 5 V. Any desired one, e.g. W_{M1} among the word lines W_{M1}, W_{M2}, ... is connected to a writing voltage of 5V by the X decoder. The other word lines W_{M2}, ... are connected to 0 V. All the word lines W_{S1}, W_{S2}, ... are held at 0 V. The data lines D_1, D_2, ... are held at any desired value, e.g. 0 V by the Y decoder. On the other hand, the P-type well 31 under the channel of the FET Q_{M1} has the voltage of 0 V applied thereto by the well voltage circuit 54. As a result, charges are injected into the floating gate of the FET Q_{M1} as described before.

In erasing data, namely, in emitting charges, all the word lines are rendered to earth potential (zero volts), whereas the potential of the P-type well 31 is set at an erasing voltage of, e.g. 5 V. Thus, charges in all the memory elements are emitted.

At this time, the word lines W_{S1}, W_{S2}, ... are held at O V, and all the data lines at any desired potential. When one word line, e.g., W_{M1} among the word lines W_{M1}, W_{M2}, ... is set at O V and the other word lines W_{M2}, ... are connected to 5 V, only data in the memory cells connected to W_{M1} can be erased.

In reading data, the data lines $\overline{D_1}$, $\overline{D_2}$, ... and the word lines W_{M1}, W_{M2}, ... are set at O V. Among the word lines W_{S1}, W_{S2}, ... , any desired one, e.g. W_{S1} is set at 5 V. Since the charges are trapped in the FET Q_{M1} connected to the selected FET Q_{S1}, the threshold voltage of the FET Q_{M1} is higher than 0V, so that this FET does not turn "on". Therefore, the potential of the data line D_1 precharged to a certain voltage, e.g. 5 V connected to the FET Q_{S1} does not change. When no charges are trapped in the FET Q_{M1}, this FET Q_{M1} turns "on", so that the potential of the data line D_1 becomes approximately 0 V. This potential of the data line D_1 is sensed by the reading circuit 52 through the Y decoder 51.

Since the writing voltage and erasing voltage in the memory element MOSFET may be 5 V, the supply voltage, 5 V of the memory circuit can be utilized as it is, and there is accordingly no need for a booster circuit. Moreover, since the reading current is high, no amplifier circuit is necessary. In addition, since the whole device is flattened and is enhanced in the density of integration, a memory device of large capacity can be constructed.

The memory device and memory circuit described above are only one example of the application of the present invention. Other various applications including, for example, a nonvolatile random access memory (NVRAM) are possible.

In the above described nonvolatile memory, a gate insulator film under a floating gate is put into a double structure by the use of insulator films having dielectric constants different from each other, and the thickness of the upper-layer insulator film is set at or below a predetermined thickness so as to situate a charge centroid within the floating gate. Thus, enhancing the density of integration of a device and lowering the writing voltage and the erasing voltage can be simultaneously

achieved and the retention of data is excellent. Another effect is that, with an increase in the capacity of the device, a simplification of the arrangement of the memory circuit can be achieved.

The advantages of the present invention can be achieved on other types of FETs by using the gate insulator film or a tunnel region. It may be favourable to use the tunnel region of a double layer structure which consists of the silicon dioxide film and the silicon nitride film formed thereon. The tunnel region is used, for example, instead of a tunnel dioxide film in a floating gate type nonvolatile memory shown in Electronics, February 28th, 1980, PP113-117, or in a floating gate type cell similar to a one transistor cell shown in Electronics, July 31st 1980, PP89-92. These examples do not enjoy the advantage in which no allowance of the alignment is required. The invention may also apply to other types of floating gate nonvolatile memory cells which use tunneling.

CLAIMS.

1. A nonvolatile memory having a field effect transistor for use as a memory element, said field effect transistor including:

(a) a semiconductor body which includes a semiconductor region of a first conductivity type;

(b) a gate insulator film which is formed on said semiconductor region, and which consists of a first gate insulator film and a second gate insulator film formed thereon, said second gate insulator film having a dielectric constant different from that of said first gate insulator film;

(c) a floating gate electrode for storing charges, which is formed on said gate insulator film;

(d) a control gate electrode which is formed over said floating gate electrode;

(e) an inter-layer insulator film which is arranged between said floating and control gate electrodes; and

(f) semiconductor regions of a second conductivity type which are formed within the first-mentioned semiconductor region, and which are located on both sides of said floating and control gate electrodes.

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2. A nonvolatile memory acording to Claim 1, wherein said first gate insulator film is a silicon dioxide film.

3. A nonvolatile memory according to Claim 2, wherein said second gate insulator film is a silicon nitride film.

4. A nonvolatile memory according to Claim 3, wherein said silicon dioxide film is 15 - 50 Å thick, and said silicon nitride film is 40 - 110 Å thick.

5. A nonvolatile memory according to Claim 4, wherein said silicon dioxide film is 20 Å thick, and said silicon nitride film is 60 Å thick.

6. A nonvolatile memory acocrding to Claim 4, wherein said inter-layer insulator film is a silicon dioxide film.

7. A nonvolatile memory according to Claim 4, wherein said inter-alyer insulator film consists of a silicon nitride film which is a first inter-layer insulator film, and a silicon dioxide film which is a second inter-layer insulator film formed on said first inter-layer insulator film.

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8. A nonvolatile memory according to Claim 7, wherein said silicon dioxide film of said first gate insulator film and said silicon dioxide film of said second inter-layer insulator film have substantially equal thicknesses, while said silicon nitride film of said second gate insulator film and said silicon nitride film of said first inter-layer insulator film have substantially equal thicknesses.

9. A nonvolatile memory according to Claim 4, wherein said inter-layer insulator film consists of a silicon nitride film which is a first inter-layer insulator film, a silicon dioxide film which is a second inter-layer insulator film formed on said first inter-layer insulator film, and a silicon dioxide film which is a third inter-layer insulator film formed between said first gate electrode and said silicon nitride film of said first inter-layer insulator film.

10. A nonvolatile memory according to Claim 9, wherein said silicon dioxide film of said first gate insulator film and said silicon dioxide film of said second inter-layer insulator film have substantially equal thicknesses, while said silicon

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nitride film of said second gate insulator film and said silicon nitride film of said first inter-layer insulator film have substantially equal thicknesses.

11. A nonvolatile memory according to Claim 4, wherein said floating gate electrode is 20 - 100 Å thick.

12. A nonvolatile memory according to Claim 11, wherein said floating gate electrode is made of a polycrystalline silicon layer.

13. A nonvolatile memory according to Claim 4, wherein said floating gate electrode is made of a polycrystalline silicon layer having a thickness of 20 - 100 Å, and said control gate electrode is made of a polycrystalline silicon layer.

14. A nonvolatile memory according to Claim 13, wherein said first conductivity type is the P-type, while said second conductivity type is the N-type.

15. A nonvolatile memory according to Claim 14, wherein said semiconductor body is an N-type silicon substrate.

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16. A nonvolatile memory including:

(a) a semiconductor body;

(b) a selecting circuit which is located on said semiconductor body;

(c) a memory array which consists of a plurality of memory cells arranged in the shape of a matrix, said memory cells being arranged within semiconductor regions of a first conductivity type formed in said semiconductor body, said memory cells having first and second selecting terminals and first and second reading terminals;

(d) a plurality of pairs of word lines which are extended from said selecting circuit into said memory array, and which receive signals for selection from said selecting circuit, one and the other of said each pair of word lines being respectively connected to the first and second terminals of the corresponding memory cells; and

(e) a plurality of pairs of data lines which are extended from said selecting circuit into said memory array in a manner to orthogonally intersect said word lines, and which receive signals for reading from said selecting circuit, one and the other of said each pair of data lines being respectively connected to the first and second reading terminals of the corresponding memory cells;

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(f) said each memory cell including a first field effect transistor for use as a memory element and a second field effect transistor as a switching element, said first and second field effect transistors being connected in series between the first and second reading terminals, control electrodes of said first and second field effect transistors being respectively connected to the first and second selecting terminals;

(g) said first field effect transistor including a silicon dioxide film which is formed on said semiconductor regions of said first conductivity type, a silicon nitride film which is formed on said silicon dioxide film, a floating gate electrode of polycrystalline silicon which is formed on said silicon nitride film, a control gate electrode which is formed over said floating gate electrode, an inter-layer insulator film which is located between said floating and control gate electrodes, and semiconductor regions of a second conductivity type which are arranged on both sides of said floating and control gate electrodes within each of the first-mentioned semiconductor regions, wherein said control gate electrode forms a part of the word line connected to the first selecting terminal.

* C L M S *

17. A nonvolatile memory constructed substantially as herein described with reference to and as illustrated in Figures 2 to 8 of the accompanying drawings.

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