CLAIMS

1. A component in plasma processing apparatus for manufacturing semiconductor comprising a deposition layer covering an interlayer boundary, the component comprising:

a first deposition layer;

a second deposition layer formed on the first deposition layer; and

a third deposition layer formed on the second deposition layer to cover at least a portion of a boundary between the first deposition layer and the second deposition layer;

wherein a grain size of each of the first deposition layer and the second deposition layer is greater than a grain size of the third deposition layer.

2. The component in plasma processing apparatus for manufacturing semiconductor of claim 1, wherein the first deposition layer, the second deposition layer, or both the first deposition layer and the second deposition layer is formed of a plurality of layers, and

the third deposition layer is formed to cover at least a portion of a boundary between the plurality of layers of the first deposition layer, the second deposition layer, or both the first deposition layer and the second deposition layer.

3. The component in plasma processing apparatus for manufacturing semiconductor of claim 1, wherein a ratio of a sum of respective diffraction peak intensities of a face 200 and a face 220 to a diffraction peak intensity of a face 111 of an X-ray diffraction spectrum of each of the first deposition layer and the second deposition layer is 0.9 to 3.5.

4. The component in plasma processing apparatus for manufacturing semiconductor of claim 1, wherein a ratio of a sum of respective diffraction peak intensities of a face 200 and a face 220 to a diffraction peak intensity of a face 111 of an X-ray diffraction spectrum of the third deposition layer is 0.05 to 0.9.

5. The component in plasma processing apparatus for manufacturing semiconductor of claim 1, wherein a ratio of a diffraction peak intensity of a face 311 to

a diffraction peak intensity of a face 111 of an X-ray diffraction spectrum of the third deposition layer is 0.05 to 0.3.

6. The component in plasma processing apparatus for manufacturing semiconductor of claim 1, wherein each of the first deposition layer, the second deposition layer, and the third deposition layer includes at least one of silicon carbide (SiC) or tantalum carbide (TaC).

7. The component in plasma processing apparatus for manufacturing semiconductor of claim 1, wherein the first deposition layer, the second deposition layer, and the third deposition layer have a same composition.

8. The component in plasma processing apparatus for manufacturing semiconductor of claim 1, wherein a thickness of the third deposition layer is 0.7 millimeters (mm) to 2.5mm.

9. The component in plasma processing apparatus for manufacturing semiconductor of claim 2, wherein the plurality of layers of the first deposition layer, the second deposition layer, or both the first deposition layer and the second deposition layer have different transmittance values.

10. The component in plasma processing apparatus for manufacturing semiconductor of claim 1, being a component of a plasma processing device including at least one selected from a group consisting of a ring, an electrode portion, and a conductor.

11. A method of manufacturing a component in plasma processing apparatus for manufacturing semiconductor comprising a deposition layer covering an interlayer boundary of claim 1, the method comprising:

preparing a base material;

forming a first deposition layer on the base material through chemical vapor deposition;

forming a second deposition layer on the first deposition layer through the

chemical vapor deposition;

performing first processing;

forming a third deposition layer; and

performing second processing.

12. The method of claim 11, wherein a flow rate and a composition of deposition gas in the forming of the first deposition layer are the same as a flow rate and a composition of deposition gas in the forming of the second deposition layer.

13. The method of claim 11, wherein a supply flow rate of deposition gas in the forming of the third deposition layer is 30% to 80% of a supply flow rate of the deposition gas in the forming of the first deposition layer and the forming of the second deposition layer.

14. The method of claim 11, wherein a deposition layer forming speed in the forming of the first deposition layer and the forming of the second deposition layer is 30 micrometers per hour (μm/hr) to 65 μm/hr.

15. The method of claim 11, wherein a deposition layer forming speed in the forming of the third deposition layer is 30% to 80% of a deposition layer forming speed in the forming of the first deposition layer and the forming of the second deposition layer.

16. The method of claim 11, further comprising:

cleaning between the performing of the first processing and the forming of the third deposition layer, after the performing of the second processing, or between the performing of the first processing and the forming of the third deposition layer and after the performing of the second processing.

17. The method of claim 11, wherein the performing of the first processing is to process a face including at least a portion of a boundary between the first deposition layer and the second deposition layer.

18. The method of claim 11, wherein the performing of the first processing comprises:

removing the base material.

19. The method of claim 11, wherein the performing of the second processing comprises:

removing the base material.

20. The method of claim 11, wherein the base material includes at least one selected from a group consisting of graphite, carbon black, silicon carbide (SiC), tantalum carbide (TaC), and zirconium carbide (ZrC).