PATENT SPECIFICATION (11) 1290092

1290092

DRAWINGS ATTACHED

(21) Application No. 9874/70 (22) Filed 2 March 1970

(31) Convention Application No. 803728 (32) Filed 3 March 1969 in

(33) United States of America (US)

(45) Complete Specification published 20 Sept. 1972

(51) International Classification H03G 3/30

(52) Index at acceptance

H3T 1A5 1R 2J 2P 2T2X 2T2Z 2T3J 2T4 2W2 3J 3X 5E 5S

(54) AUTOMATIC GAIN CONTROL CIRCUIT

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to automatic gain control (AGC) systems for superheterodyne receiving apparatus, and, particularly, to AGC systems applicable to use in association with superheterodyne receivers incorporating intermediate frequency (IF) amplifiers fabricated with integrated circuit (IC) techniques.

Disclosed in our United States Patent, No. 3628166, entitled "Wide-Band Amplifier", is a gain-controllable IF amplifier arrangement suitable for fabrication in integrated form on a monolithic integrated circuit chip. In the arrangement disclosed in that application, input signals are applied to a voltage amplifier stage via a dynamic attenuator network. A delay transistor biased into saturation, holds off a transistor serving as the active device of the attenuator network over a first range of received signal levels below a given threshold level, resulting in a constant, small degree of introduced attenuaton. AGC bias variations applied to the input electrode of the amplifier stage serve to vary the gain of the amplifier stage without changing the network attenuation in the first range of operation.

The forward bias on the base of the delay transistor is made responsive to the AGC bias. At a chosen AGC bias level, reflecting a given received signal level, the delay transistor comes out of saturation, permitting the delay transistor collector potential to vary (inversely) with AGC bias. At a still greater signal level, the delay transistor collector potential variation from its saturation potential is sufficient to bias the attenuator transistor into conduction. For signal strengths increasing above this threshold, the attenuator provides increasing degrees of attenuation, thus limiting the voltage swing at the amplifier input electrode. Attenuator transistor conduction closes a D.C. negative feedback loop which holds the bias at the amplifier input electrode relatively constant in the face of input AGC variations reflecting signal levels above the threshold. Thus, in the second, above-threshold, range of operation, control is essentially confined to attenuator action, with the gain of the amplifier stage remaining relatively constant.

The above-described arrangement facilitates handling of a wide range of input signals by the IF amplifier, with distortion at the strong-signal end of the range avoided without introducing impairment of signal-to-noise ratio at the weak-signal end of the range. Moreover, as disclosed in said United States patent, the attenuator network and associated delay transistor circuit may conveniently be realized in integrated form on the same monolithic integrated circuit chip as the associated amplifier stage.

The present invention is directed to a modification of the above-described arrangement enabling accurately controlled association of a delayed RF AGC action with the aforementioned IF gain control and IF attenuator actions. Pursuant to the present modification, derivation of an AGC potential for control of RF amplification of received signals prior to conversion of intermediate frequencies is associated with the delay apparatus controlling IF attenuator action. Use of common delay apparatus enables accurate relating of the respective thresholds of RF AGC and IF attenuator actions.

In a preferred application of the principles of the present invention, directed toward optimizing the signal handling range of the superheterodyne receiver, signal amplitude control in response to an AGC potential source follows a sequence including at least three distinct phases: (a) a weak-signal phase, wherein AGC action is confined to IF amplifier gain variations; (b) a medium-

signal phase, wherein IF amplifier gain variations are accompanied by RF amplifier gain variations; and (c) a strong-signal phase, wherein AGC action is confined essentially to IF attenuator action.

In accordance with a specific embodiment of the present invention, a delay transistor functioning as previously described is coupled to control both an IF attenuator transistor and an RF drive transistor. Conduction of the latter is initiated at a signal threshold level (indicated by IF amplifier bias level) below that causing initation of attenuator transistor conduction, and a full range of RF AGC action is traversed before reaching the latter level. When attenuator action begins, the previously mentioned negative feedback loop closing serves to stabilize IF amplifier gain at a relatively constant value. The same monolithic integrated circuit chip which incorporates the controlled IF amplifier, delay transistor circuit and attenuator network may conveniently accommodate the RF AGC drive transistor circuit.

A feature of the present invention provides a superheterodyne receiver with a delayed RF AGC system associated in a such manner with IF signal control as to enhance the signal handling range of the receiver.

In the accompanying drawing a portion of a superheterodyne receiver embodying the present invention is illustrated, partly in schematic detail and partly by block diagram representation.

In the drawing, a tuner 18 is illustrated in block form; the tuner 18 incorporates apparatus for performing the conventional functions of selectively amplifying a desired one of various received RF signals, and converting the selected RF signal to intermediate frequencies. A selectivity network 20, providing a bandpass characteristic appropriate to the particular receiver's IF operating frequencies, couples the output of tuner 18 to the IF input terminal T5 of a monolithic integrated circuit chip indicated by the dotted outline 30. Chip 30 includes circuitry performing an IF amplifier function (as will be described in more detail subsequently) and provides an IF amplifier output signal at chip terminal T8.

A second selectivity network 40, further defining the IF passband, couples the IF signals at chip terminal T8 to an output terminal 0. While the subsequent receiver circuits (not illustrated) may differ depending on the particular signals for which the receiver is provided, typically additional IF amplifier stages will be interposed between terminal 0 and the receiver's IF signal detecting apparatus.

An IF AGC potential source 50 supplies a variable bias to the IF input terminal T5 of chip 30. The IF AGC potential source 50 is shown in block form only in the drawing. A variety of ways of developing a suitable IF AGC potential from detected IF signals are known to the art, and the present invention is not concerned with the details thereof. For the particular circuit embodiment of the drawing, it may be assumed that source 50 supplies a positive bias potential to terminal T5 which becomes less positive with increases in received signal level. To explain the resulting changes of the receiver operation, which changes reduce the effects of received signal level variations on the output signal level at terminal 0, the schematic details of the drawing will now be described.

In the illustrated circuitry for chip 30, the intermediate frequency signals supplied by selectivity network 20 to chip terminal T5 are directly applied to the base of a transistor Q101, arranged as an emitter follower. In place of an emitter resistor, the collector-emitter path of a transistor Q119 provides a return to the ground terminal T4 of chip 30 from the emitter of Q101 (for reasons to be subsequently described).

The signals appearing at the emitter of transistor Q101 are applied to an attenuator formed by a resistor R101 and the emitter-collector path of a transistor Q103. An attenuated version of the emitter-follower output will appear at the resistor-transistor junction, the degree of attenuation depending upon the impedance presented by the emitter-collector path of transistor Q103. The functioning of this attenuator network will be described in greater detail subsequently.

The attenuator network output is supplied via a pair of emitter-follows (Q105 and Q107) in cascade to the base of a transistor Q109, the output of the cascaded emitter-followers appearing across emitter resistor R107. Transistor Q109 is disposed in a cascode pair arrangement with transistor Q111 to form a high gain amplifying stage supplying an output to the chip's IF output terminal T8. In the cascode pair arrangement, Q109 is a base-input, grounded emitter stage, the collector of which is directly connected to the emitter-input, grounded base stage constituted by transistor Q111. Operating potential for the cascode amplifying stage is supplied from the B+ chip terminal T12 via an external resistor 56 and a coil of the selectivity network 40.

As previously explained, in addition to IF input signals, an AGC control potential is supplied to input terminal T5. By virtue of the direct coupling via emitter follower Q101, resistor R101 and emitter-followers Q105 and Q107, such AGC input directly affects the bias at the base of transistor Q109 of the cascode pair. The supplied AGC potential variations are poled to provide reverse AGC action; that is, as signal strength increases, the bias voltage at the base of Q109 is made less positive to introduce a desired reduction in the gain of the cascode amplifying stage.

As discussed in the aforementioned United States Patent No. 3628166, it is desirable to provide in addition to the gain variations of the cascode amplifying stage further aid in gain reduction, and, in particular, further aid of a character to provide, under strong signal conditions, a limitation on the voltage swing supplied to the base of transistor Q109, whereby distortion in that stage may be avoided. It is for such purpose that the previously mentioned R101/Q103 attenuator is provided.

Control of the attenuator is provided in the following manner. A transistor Q113 is provided, deriving its collector potential from an external receiver power supply via an external resistor 52, and with its base responding to the voltage at the base of transistor Q109 by virtue of the connection of resistor R113 between the respective bases. Under no-signal or weak-signal conditions, the base of transistor Q113 is sufficiently forward biased that the transistor is in saturation.

Under such saturation conditions, an emitter-follower transistor Q115, having its base directly connected to the collector of transistor Q113 and its emitter returned to ground via resistors R115 and R116 in series, is held in nonconducting condition. Transistor Q103, in the previously mentioned attenuator network, has its base directly connected to the emitter of the emitter-follower transistor Q115.

Thus, under weak-signal conditions, transistor Q103 is likewise nonconducting, and, as a consequence, a constant, relatively small degree of attenuation is introduced by the R101/Q103 network. The interposition of the cascaded emitter-follower transistors Q105, Q107 in the signal path to the cascode amplifier input establishes a dynamic input impedance sufficiently high relative to the impedance of the attenuator resistor R101 as to ensure that the degree of attenuation of weak signals (when transistor Q103 is nonconducting) is indeed small.

Under strong signal conditions, however, the AGC potential derived from the source 50 will lower the voltage at the base of transistor Q109 and will reach a point at which transistor Q113 will come out of saturation allowing its collector to rise to a level sufficient to forward bias the emitter-follower transistor Q115. The emitter of transistor Q115 thereafter follows the rising base voltage; transistor Q103 will begin to conduct when the emitter of transistor Q115 rises to a positive voltage sufficient to overcome the reverse bias at the emitter of transistor Q103.

For signal strengths above the conditions just described, the current drawn by transistor Q103 will increase and the impedance presented by the emitter-collector path of Q103 will decreasee as the signal strength increases to introduce greater and greater degrees of attenuation of the IF signal to be delivered to the base of transistor Q109.

An additional transistor Q117 is provided for driving the delayed RF AGC output terminal T6. The base of transistor Q117 is directly connected to the junction of the resistors R115 and R116 in the emitter circuit of emitter-follower Q115. The emitter of transistor Q117 is returned to ground via an emitter resistor R117, while the collector of transistor Q117 is linked via chip terminal T6 and external resistor 58 to the power supply (+30V) regulated by the chip 80 as will be subsequently described. Under the no-signal and weak-signal conditions which hold transistor Q115 off, transistor Q117 is likewise off.

When, however, signal strength is sufficiently high that emitter follower Q115 conducts sufficiently, the base of transistor Q117 becomes forward biased, and transistor Q117 starts conducting. Setting of the threshold of RF AGC delivery may be controlled externally, as by the selection of the value of resistor 52 to determine the saturation current of the delay transistor Q113.

For signal levels above the selected threshold level, i.e., for AGC levels beyond that sufficient to remove transistor Q113 for saturation, and in turn render transistors Q115 and Q117 conducting, the voltage at terminal T6 will vary in accordance with the AGC potential at the base of Q107. Shifted to a lower voltage range by the shifting network formed by resistors 54 and 55 (in association with a negative potential supply), the varying voltage at the junction of resistors 54 and 55 constitutes a suitably delayed AGC potential for RF amplifier control in tuner 18. Filtering of the RF AGC potential is facilitated by the coupling of capacitor 57 between the resistor junction and the bypassed chip terminal T7.

It may be noted that, desirably, the delay threshold associated with the RF AGC drive transistor Q117 is less than the delay threshold associated with the attenuator transistor Q103. That is, RF AGC action is initated at a lower level of signal strength (as indicated by the AGC potential) than the signal strength level at which attenuator action begins. Indeed, preferably, the full range of RF gain control is traversed before the start of attenuator action. Thus, for example, in the illustrated circuit, the RF AGC drive transistor Q117 reaches saturation for a level of voltage at the emitter of transistor Q115 that associated with the initiation of conduction of attenuator transistor Q103.

It should also be observed that, once attenuator action is commenced by the conduction of transistor Q103, a negative D.C. feedback loop of relatitvely high gain is completed, the loop including resistor R113 and transistors Q113, Q115, Q103, Q105 and Q107.

A consequence of such feedback is that the bias at the base of transistor Q109 is held relatively constant in the face of further increases in the AGC potential supplied at terminal T5.

Accordingly, the control sequence includes at least three distinct phases. In a first, relatively weak-signal level phase, AGC action is confined to gain variations for the cascode amplifier stage Q109, Q111; for a second medium-signal level phase, gain variations for the cascode amplifier stage are accompanied by RF gain variations; in a third, strong signal level phase, AGC action is confined essentially to the operation of the attenuator network R101, Q103. A fourth phase, involving a reversion to IF amplifier gain variations alone, may optionally be associated with the transition between the above-mentioned second and third phases, as governed by the degree of separation of levels for transistor Q117 saturation and transistor Q103 conduction initiation.

As previously noted, the collector-emitter path of transistor Q119 provides a return to ground from the emitter of the input emitter follower transistor Q101. Transistor Q119 is used in place of an emitter resistor to provide a relatively constant current supply for the emitters of transistors Q101 and Q103, with the current being of sufficient magnitude as to prevent the current "robbing" (from transistor Q101) by transistor Q103 from limiting the AGC range.

That is, in the strong signal mode of operation, when transistor Q103 comes into conduction and draws greater and greater amounts of current, there will be a corresponding reduction of current through transistor Q101. To avoid cutoff of transistor Q101 under such circumstances, the emitters must see an adequate current source. Transistor Q119 serves as such a source, with its base suitably biased to establish a relatively constant current of the desired magnitude.

The required bias current for supply transistor Q119 is derived from the emitter of the emitter-follower transistor Q105 by a biasing network comprising the series combination of resistor R104, resistor R105 and a forward biased stabilizing diode D101, with the base of transistor Q119 connected to the junction of resistors R104 and R105. The total resistance value of the series combination is chosen to give a bias current appropriate to set the constant current supply in the desired range. The resistance value of resistor R104 is chosen to be sufficiently large relative to that of resistor R105 to prevent transistor Q119 from introducing any significant degeneration of the AGC potential (in the weak-signal mode).

The circuitry of chip 30 additionally includes a decoupling network for supplying operating potentials to a number of transistor devices previously discussed. A regulated B+ voltage (illustratively, 11 volts) is developed by a regulator circuit 80 from a power supply (not illustrated) provided elsewhere in the receiver and is supplied to chip terminal T12. The B+ voltage is applied to a simple decoupling network comprising the series combination of resistor R119 and zener diode Z101.

While this simple network provides adequate decoupling, the zener diode operation may introduce an undesired level of noise in the voltage appearing thereacross. Accordingly, the voltage across zener diode Z101 is applied via an emitter-follower Q121 to a dynamic noise filter network comprising transistor Q123, resistor R121 and capacitor C101. The collector of transistor Q123 is directly connected to the emitter of transistor Q121. Resistor R121 links the base of transistor Q123 to the emitter of transistor Q121, while capacitor C101 is coupled between the base of transistor Q123 and the T4 ground lead. There is thus available at an emitter electrode of the filter transistor Q123 a relatively noise free B+ potential, adequately decoupled from additional circuits linked to terminal T12.

It has been found to be additionally advisable to decouple the collectors of transistors Q101 and Q103 from the collector of subsequent stages in the chip circuitry. To this end, transistor Q123 is constructed in double-emitter form, with a first emitter supplying B+ potential to the collectors of transistors Q101 and Q103, and with a second emitter providing an isolated B+ potential source for the collectors of transistors Q105, Q107, Q109 and Q115. The base of the emitter-input transistor Q111 of the cascade amplifier is also returned to the latter B+ potential source.

Illustratively, one type of superheterodyne receiver in which the principles of the present invention have been successfully employed is a color television receiver. In our United States patent 3564125, details of such a color television receiver embodiment are presented. In that example of use, the circuitry shown herein for chip 30 was included on the same monolithic integrated circuit chip with additional circuitry performing such functions as final IF amplification, video detection, video amplification, AGC control potential development, intercarrier sound detector drive, intercarrier sound detection, intercarrier sound IF amplification, automatic fine tuning (AFT) drive and regulator reference control. The AGC control potential development circuits used therein embody the invention disclosed in our Application 9873/70 (Serial No. 1290091).

By way of example only, a set of values for the circuitry of chip 30 and off-chip components associated therewith in the drawing,

which values provided satisfactory operation in the aforementioned color television receiver embodiment, are set forth in the tables below:

TABLE A:
ON-CHIP COMPONENT VALUES

Resistor	R101	1,000 ohms
Resistor	R104	2,000 ohms
Resistor	R105	360 ohms
Resistor	R107	700 ohms
Resistor	R113	1,000 ohms
Resistor	R115	1,600 ohms
Resistor	R116	3,200 ohms
Resistor	R117	800 ohms
Resistor	R121	3,000 ohms
Capacitor	C101	20 picofarads

TABLE B:
OFF-CHIP COMPONENT VALUES

Resistor	52	100,000 ohms
Resistor	54	2,400 ohms
Resistor	55	62,000 ohms
Resistor	56	1,200 ohms
Resistor	58	6,800 ohms
Capacitor	53	.001 microfarad
Capacitor	57	.100 microfarad
Capacitor	59	.001 miicrofarad

WHAT WE CLAIM IS:—

1. An automatic gain control (AGC) circuit adapted to be used in a superheterodyne receiver having an AGC source providing a DC potential varying in response to received signal level variations, the AGC circuit including an IF amplifier having an input circuit, means including a dynamic attenuator network, adapted to receive intermediate frequency signals and apply said signals and said varying DC potential from said AGC source to said IF amplifier input circuit, an attenuator transistor included in said dynamic attenuator, the degree of conduction of said attenuator transistor controlling the degree of attenuation introduced by said attenuator network, an RF AGC drive transistor, and common delay means controlled by said varying D.C. potential for preventing conduction of both of said attenuator and RF AGC drive transistors when received signal levels fall in a first, weak-signal range, for preventing conduction of said attenuator transistor and permitting conduction of said RF AGC drive transistor when received signal levels fall in a second, medium-signal range, and for permitting conduction of both of said attenuator and RF AGC drive transistors when received signal levels fall in a third, strong-signal range.

2. A circuit as claimed in claim 1 in which said delay means includes a delay transistor biased into saturation in the absence of received signals.

3. A circuit as claimed in Claim 1 or 2 wherein conduction by said attenuator transistor when received signal levels fall in said strong-signal range closes a D.C. negative feedback loop opposing variations in the D.C. potential at said IF amplifier input circuit.

4. A circuit as claimed in Claims 1, 2, or 3 arranged so that said RF AGC drive transistor operates in saturation when received signal levels fall in said strong-signal range.

5. A circuit as claimed in any one of the preceding claims in which said circuit is disposed in a monolithic integrated circuit.

6. A circuit as claimed in Claim 4 wherein the RF AGC drive transistor is arranged to saturate for received signal levels falling in a fourth range below said strong-signal range, as well as in the latter range.

7. A superheterodyne receiver with circuitry substantially as described in conjunction with the accompanying drawing.

T. I. M. SMITH,
Chartered Patent Agent,
50 Curzon Street,
London W1Y 8EU.
Agent for the Applicant.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1972.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

which values provided satisfactory operation in the aforementioned color television receiver embodiment, are set forth in the tables below:

TABLE A:
ON-CHIP COMPONENT VALUES

Resistor	R101 —	1,000 ohms
Resistor	R104 —	2,000 ohms
Resistor	R105 —	360 ohms
Resistor	R107 —	700 ohms
Resistor	R113 —	1,000 ohms
Resistor	R115 —	1,600 ohms
Resistor	R116 —	3,200 ohms
Resistor	R117 —	800 ohms
Resistor	R121 —	3,000 ohms
Capacitor	C101 —	20 picofarads

TABLE B:
OFF-CHIP COMPONENT VALUES

Resistor	52 —	100,000 ohms
Resistor	54 —	2,400 ohms
Resistor	55 —	62,000 ohms
Resistor	56 —	1,200 ohms
Resistor	58 —	6,800 ohms
Capacitor	53 —	.001 microfarad
Capacitor	57 —	.100 microfarad
Capacitor	59 —	.001 miicrofarad

WHAT WE CLAIM IS:—

1. An automatic gain control (AGC) circuit adapted to be used in a superheterodyne receiver having an AGC source providing a DC potential varying in response to received signal level variations, the AGC circuit including an IF amplifier having an input circuit, means including a dynamic attenuator network, adapted to receive intermediate frequency signals and apply said signals and said varying DC potential from said AGC source to said IF amplifier input circuit, an attenuator transistor included in said dynamic attenuator, the degree of conduction of said attenuator transistor controlling the degree of attenuation introduced by said attenuator network, an RF AGC drive transistor, and common delay means controlled by said varying D.C. potential for preventing conduction of both of said attenuator and RF AGC drive transistors when received signal levels fall in a first, weak-signal range, for preventing conduction of said attenuator transistor and permitting conduction of said RF AGC drive transistor when received signal levels fall in a second, medium-signal range, and for permitting conduction of both of said attenuator and RF AGC drive transistors when received signal levels fall in a third, strong-signal range.

2. A circuit as claimed in claim 1 in which said delay means includes a delay transistor biased into saturation in the absence of received signals.

3. A circuit as claimed in Claim 1 or 2 wherein conduction by said attenuator transistor when received signal levels fall in said strong-signal range closes a D.C. negative feedback loop opposing variations in the D.C. potential at said IF amplifier input circuit.

4. A circuit as claimed in Claims 1, 2, or 3 arranged so that said RF AGC drive transistor operates in saturation when received signal levels fall in said strong-signal range.

5. A circuit as claimed in any one of the preceding claims in which said circuit is disposed in a monolithic integrated circuit.

6. A circuit as claimed in Claim 4 wherein the RF AGC drive transistor is arranged to saturate for received signal levels falling in a fourth range below said strong-signal range, as well as in the latter range.

7. A superheterodyne receiver with circuitry substantially as described in conjunction with the accompanying drawing.

T. I. M. SMITH,
Chartered Patent Agent,
50 Curzon Street,
London W1Y 8EU.
Agent for the Applicant.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1972.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.