

CLAIMS

1. A method for performing low-density parity-check (LDPC) decoding, the method comprising:
 - receiving soft bits associated to an LDPC codeword; and
 - performing LDPC decoding of the soft bits using a parity check matrix, wherein:
 - each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code,
 - at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and
 - the parity check matrix has row orthogonality between each pair of consecutive rows that are below a row to which the at least two punctured variable nodes are both connected.
2. The method of claim 1, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.
3. The method of claim 1, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have row orthogonality.
4. The method of claim 3, wherein the 1/2 of all pairs of consecutive rows comprises the last 1/2 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.
5. The method of claim 1, wherein the parity check matrix comprises:
 - a core portion of a first N rows; and
 - hybrid automatic repeat request (HARQ) rows after the first N rows.
6. The method of claim 5, wherein:
 - for each row below the row to which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows.

7. An apparatus for wireless communications, comprising:
a processor configured to:
 cause the apparatus to receive soft bits associated to a low-density parity-check (LDPC) codeword; and
 perform LDPC decoding of the soft bits using a parity check matrix,
wherein:
 each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code,
 at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and
 the parity check matrix has row orthogonality between each pair of consecutive rows that are below a row to which the at least two punctured variable nodes are both connected; and
a memory coupled with the processor.
8. The apparatus of claim 7, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.
9. The apparatus of claim 7, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have row orthogonality.
10. The apparatus of claim 9, wherein the 1/2 of all pairs of consecutive rows comprises the last 1/2 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.
11. The apparatus of claim 7, wherein the parity check matrix comprises:
a core portion of a first N rows; and
hybrid automatic repeat request (HARQ) rows after the first N rows.
12. The apparatus of claim 11, wherein:
for each row below the row in which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows.

13. An apparatus for performing low-density parity-check (LDPC) decoding, the apparatus comprising:

means for receiving soft bits associated to an LDPC codeword; and

means for performing LDPC decoding of the soft bits using a parity check matrix,

wherein:

each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code,

at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and

the parity check matrix has row orthogonality between each pair of consecutive rows that are below a row to which the at least two punctured variable nodes are both connected.

14. The apparatus of claim 13, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.

15. The apparatus of claim 13, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have rows orthogonality.

16. The apparatus of claim 15, wherein the 1/2 of all pairs of consecutive rows comprises the last 2/3 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.

17. The apparatus of claim 13, wherein the parity check matrix comprises:
a core portion of a first N rows; and
hybrid automatic repeat request (HARQ) rows after the first N rows.

18. The apparatus of claim 17, wherein:
for each row below the row in which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows.

19. A computer-readable medium for performing low-density parity-check (LDPC) decoding, comprising instructions that, when executed by at least one processor, cause the at least one processor to perform operations comprising:

receiving soft bits associated to an LDPC codeword; and

performing LDPC decoding of the soft bits using a parity check matrix, wherein:

each row of the parity check matrix corresponds to a lifted parity check of the lifted LDPC code,

at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and

the parity check matrix has row orthogonality between each pair of consecutive rows that are below a row to which the at least two punctured variable nodes are both connected.

20. The computer-readable medium of claim 19, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.

21. The computer-readable medium of claim 19, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have rows orthogonality.

22. The computer-readable medium of claim 21, wherein the 1/2 of all pairs of consecutive rows comprises the last 1/2 of all layers of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.

23. The computer-readable medium of claim 19, wherein the parity check matrix comprises:

a core portion of a first N rows; and

hybrid automatic repeat request (HARQ) rows after the first N rows.

24. The computer-readable medium of claim 23, wherein:

for each row below the row in which the at least two punctured variable nodes are connected to the same row, no column has a non-empty entry in two consecutive rows.

25. A method for performing low-density parity-check (LDPC) encoding, the method comprising:
- obtaining information bits of a codeword; and
 - performing encoding of the information bits to compute parity bits of an LDPC codeword according to a parity check matrix, wherein:
 - each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code,
 - at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and
 - the parity check matrix has row orthogonality between each pair of consecutive rows that are below a row to which the at least two punctured variable nodes are both connected.
26. The method of claim 25, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.
27. The method of claim 25, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have row orthogonality.
28. The method of claim 27, wherein the 1/2 of all pairs of consecutive rows comprises the last 1/2 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.
29. The method of claim 25, wherein the parity check matrix comprises:
- a core portion of a first N rows; and
 - hybrid automatic repeat request (HARQ) rows after the first N rows.
30. The method of claim 29, wherein:
- for each row below the row to which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows.
31. An apparatus for wireless communications, comprising:
- a processor configured to:

obtain information bits of a codeword; and
perform encoding of the information bits to compute parity bits of an LDPC codeword according to a parity check matrix, wherein:
each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code,
at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and
the parity check matrix has row orthogonality between each pair of consecutive rows that are below a row to which the at least two punctured variable nodes are both connected; and
a memory coupled with the processor.

32. The apparatus of claim 31, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.

33. The apparatus of claim 31, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have row orthogonality.

34. The apparatus of claim 33, wherein the 1/2 of all pairs of consecutive rows comprises the last 1/2 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.

35. The apparatus of claim 31, wherein the parity check matrix comprises:
a core portion of a first N rows; and
hybrid automatic repeat request (HARQ) rows after the first N rows.

36. The apparatus of claim 35, wherein:
for each row below the row in which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows.

37. An apparatus for performing low-density parity-check (LDPC) encoding, the apparatus comprising:
means for obtaining information bits of a codeword; and

means for performing encoding of the information bits to compute parity bits of an LDPC codeword according to a parity check matrix, wherein:

each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code,

at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and

the parity check matrix has row orthogonality between each pair of consecutive rows that are below a row to which the at least two punctured variable nodes are both connected.

38. The apparatus of claim 37, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.

39. The apparatus of claim 37, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have rows orthogonality.

40. The apparatus of claim 39, wherein the 1/2 of all pairs of consecutive rows comprises the last 2/3 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.

41. The apparatus of claim 37, wherein the parity check matrix comprises:
a core portion of a first N rows; and
hybrid automatic repeat request (HARQ) rows after the first N rows.

42. The apparatus of claim 41, wherein:
for each row below the row in which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows.

43. A computer-readable medium for performing low-density parity-check (LDPC) encoding, comprising instructions that, when executed by at least one processor, cause the at least one processor to perform operations comprising:
obtaining information bits of a codeword; and

performing encoding of the information bits to compute parity bits of an LDPC codeword according to a parity check matrix, wherein:

each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code,

at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and

the parity check matrix has row orthogonality between each pair of consecutive rows that are below a row to which the at least two punctured variable nodes are both connected.

44. The computer-readable medium of claim 43, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.

45. The computer-readable medium of claim 43, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have rows orthogonality.

46. The computer-readable medium of claim 45, wherein the 1/2 of all pairs of consecutive rows comprises the last 1/2 of all layers of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.

47. The computer-readable medium of claim 43, wherein the parity check matrix comprises:

a core portion of a first N rows; and

hybrid automatic repeat request (HARQ) rows after the first N rows.

48. The computer-readable medium of claim 47, wherein:

for each row below the row in which the at least two punctured variable nodes are connected to the same row, no column has a non-empty entry in two consecutive rows.