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ABSTRACT

An object of this array substrate for a flat display device is to eliminate display unevenness caused by the inequality of parasitic capacitances of switches of signal line switch circuits. Electrode patterns
5 (P) which connects the gate electrodes of the switches (ASW) to any one of a plurality of switch control signal lines (ASWL1 and ASWL2) are formed so as to each two-dimensionally overlap all of the switch control signal lines ASWL and to have substantially identical shapes, thus equalizing the areas of the electrode patterns (P).



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