

SPECIFICATION

Apparatus for displaying a group of characters

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The present invention relates to an apparatus for displaying a group of characters, and is particularly but not exclusively useful in a television game.

- 10 Television game machines incorporating recent developments of microelectronics and microcomputers and capable of providing various types of games using a television receiver have become popular. In an example of a
- 15 game played with such a television game machine, a plurality of characters are first displayed in an initial condition and a moving symbol such as a ball is displayed to move on the screen, while a position controllable symbol such as a racket is displayed on the screen
- 20 such that a player hits and repulses the moving symbol with the position-controllable symbol through manual operation of a control knob for the position-controllable symbol in order to make the moving symbol collide with one of the characters. When the moving symbol collides with any one of the characters, the display of the said one character is extinguished. The number of the characters thus
- 25 extinguished is counted to keep the score. The score is also displayed.

- In order to display characters on the screen of a cathode ray tube using such a television game machine, a so-called video random-access memory may be used. It has been a
- 35 conventional common practice that a video random-access memory is structured to comprise a plurality of storing regions corresponding to the picture elements of a picture frame of a cathode ray tube. As well known, when
- 40 using a cathode ray tube, each line of a picture frame is scanned in the horizontal direction and successive lines are scanned in the vertical direction with an electron beam.
- 45 (The terms "horizontal" and "vertical" are used herein in a broad sense to refer to the two transverse directions in which a scanning type of display such as a cathode ray tube is scanned). According to the Japanese television standard, one picture frame comprises
- 50 262 lines and the horizontal scanning is performed by way of the interlaced scanning method. Let it be assumed that the horizontal line is divided into say 114 to consider one
- 55 picture frame as comprising a plurality of picture elements arranged in rows and columns. Therefore, it was required that a conventional video random-access memory comprised a number of bits commensurate with
- 60 the product ($114 \times 262 = 29868$) obtained by multiplication of the number of elements in the horizontal direction (114) by the number of elements in the vertical direction (262). The stored information is read out bit by bit during
- 65 the horizontal scanning and the vertical scanning

and each time the logic one representing that display is to be made at the position corresponding to a given bit is read, display is made on the corresponding region on the

70 screen of the cathode ray tube. Thus, the logic one is written in a plurality of bits or storing regions in the random-access memory corresponding to a corresponding plurality of picture elements constituting the configuration of a character to be displayed. As a result, it was required that the conventional video random-access memory have a large storage capacity. As a result, such a video random-access memory was expensive and accordingly a game machine utilizing such a conventional random-access memory was considerably expensive.

- In playing such a game, the arrangement of the characters being displayed needs to be
- 85 returned to an initial condition to be ready for the following game, after one game is ended, so that the characters as extinguished in the previous game are again displayed. To that end, a conventional game machine comprises
- 90 a read-only memory for fixedly storing a predetermined pattern of characters to be displayed in the initial condition. The read-only memory also comprises a plurality of bits corresponding to a corresponding plurality of picture elements constituting the configurations of the characters being displayed, which necessitates a large storage capacity. Accordingly, a read-only memory for storing such a pattern of characters also was expensive. Further, if it is desired that the pattern of characters be changeable, a read-only memory of a larger storage capacity was required.

- In some type of conventional television game machines, a microcomputer has been
- 105 utilized and generation of signals for displaying a moving symbol such as a ball, a position controllable symbol such as a racket, and the like, detection of collision of the moving symbol with one of characters, and the like have been achieved by software processing by means of a microcomputer. However, a conventional video random-access memory and a read-only memory of a large storage capacity as described above have increased the number of steps of control operations performed by a microcomputer and thus required a microcomputer of a higher speed and larger scale. Accordingly, a conventional game machine using a microcomputer became much
- 120 more expensive.

- In some cases, it is desired that the configuration of the characters themselves be changeable depending on the kind of game or in order to increase the interest of the game.
- 125 However, in order to change the configuration of a character per se being displayed using a conventional video random-access memory, it was necessary to load information associated with the character configuration in a plurality of bits in the video random-access memory
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corresponding to the changed character configuration. Typically, such a change of a character configuration is performed by way of software processing by a microcomputer. Accordingly, a game machine capable of changing a character configuration became much more complicated and expensive.

According to the present invention there is provided an apparatus for displaying a group of characters on a display by repetitive horizontal and vertical scanning of the display, the apparatus comprising:

display storage means having storing regions each of which corresponds to a respective one of a number of individual areas of the display and stores information representing whether or not a character is to be displayed in the respective area, the total area occupied by said individual areas corresponding to all said storing regions being less than the total display area,

addressing means for sequentially addressing, in association with said horizontal and vertical scanning, said storing regions of said storage means to enable said information to be read out therefrom, said addressing means generating addresses only when said individual areas are being scanned, and

converting means responsive to the read-out information for converting information representing that a character is to be displayed into an electrical display signal for displaying said character in the respective area on the display.

Thus, the storage means needs only to have a number of storing regions corresponding to the number of displayable characters, and does not need to have a number of storing regions corresponding to all the picture elements of the display, as required in a conventional apparatus. Accordingly, the apparatus of the present invention may be inexpensive, and of an extremely simple structure. By employing the apparatus of the invention in a television game machine, the latter can be provided at an extremely inexpensive cost.

In a preferred embodiment, the storage means is addressed using row addresses each corresponding to a respective vertical position on the display and column addresses each corresponding to a respective horizontal position on the display. During scanning, the address of a storing region is provided when the horizontal and vertical scans reach the position of the character whose display condition is stored in this storing region.

In a preferred embodiment of the present invention, a column address for the storage means is provided while counting a number of pulses corresponding to the width of the character to be displayed and similarly a vertical address is provided while counting a number of pulses corresponding to the vertical width of the character.

Preferably, the characters are displayed in a

pattern which is stored in a separate storage means, such as a read-only memory. The read-only memory for storing such a pattern may have a number of storing regions commensurate with the product obtained by multiplying the maximum number of characters in the horizontal direction by the maximum number in the vertical direction, a signal representing whether or not a respective character is to be displayed being stored in each storing region. The read-only memory for storing the pattern of the characters is also addressed in association with the horizontal scanning and vertical scanning.

If desired, more than one such read-only memory may be provided, each storing a respective pattern of characters. Any one of the patterns can be selected, whereby if the apparatus is employed in a television game machine, a variety of games can be provided and thereby the players interest increased.

The term "character" as used herein refers to any selectively displayable symbol. In one embodiment, the character is in the shape of a rectangle. However, more detailed configurations are possible. According to a preferred embodiment of the invention, a character configuration memory, e.g. a read-only memory, is provided for storing the configuration of the characters. The character configuration memory has sufficient storing regions for storing a desired configuration of one character. The memory may be arranged to be addressed by horizontal and vertical addressing signals. The contents of the storing regions of the memory are all read out while a storing region of the display storage means is being addressed, whereby the character corresponding to this storing region of the display storage means can be displayed in the desired configuration. If desired, several different configurations can be stored.

Thus, no particularly complicated software processing is required in order to change the configuration of the characters and therefore a microcomputer of a simple structure can be employed. Therefore, if such an apparatus is employed in a television game machine, a machine providing a variety of games can be provided at a relatively inexpensive cost and with a simple structure.

Arrangements embodying the invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a view showing a television game machine of one embodiment of the present invention;

Figure 2 is a block diagram of a main body of the television game machine shown in Fig. 1;

Figure 3 is a block diagram showing in more detail a character vertical timing generating circuit;

Figure 4 is a block diagram showing in

more detail a ball symbol signal generating circuit;

Figure 5A is a block diagram showing in more detail a racket symbol signal generating circuit;

Figure 5B is a graph showing waveforms for explaining the operation of the Fig. 5A diagram;

Figure 6 is a block diagram showing in more detail a collision detecting circuit and a game control circuit;

Figure 7 is a view diagrammatically showing one example of a random-access memory included in the character signal generating circuit;

Figure 8A is a timing chart showing one example of the timing signals obtained from the horizontal timing decoder;

Figure 8B is a timing chart showing one example of the timing signals obtained from the vertical position decoder;

Figure 9 is a block diagram showing another embodiment of the character signal generating circuit;

Figure 10A is a diagram showing one example of a pattern of characters that can be displayed in accordance with the Fig. 9 embodiment;

Figure 10B is a view diagrammatically showing the read-only memory for storing the pattern shown in Fig. 10A;

Figure 11A is a view showing another example of a character pattern;

Figure 11B is a view diagrammatically showing the information stored in the read-only memory for the pattern shown in Fig. 11A;

Figure 12 is a block diagram of another embodiment of the character signal generating circuit, wherein a group of characters can be displayed in different patterns;

Figure 13 is a block diagram showing a further embodiment of the character signal generating circuit, wherein a character pattern is written in the random-access memory in an initial condition;

Figure 14 is a block diagram showing a still further embodiment of the character signal generating circuit adapted for displaying characters each having a given configuration;

Figure 15A shows one example of a character configuration;

Figure 15B is a view diagrammatically showing the read-only memory for storing the character configuration shown in Fig. 15A;

Figures 16A and 16B are timing charts showing the horizontal timing signal TH and the vertical timing signal TV, respectively;

Figure 17 is a block diagram showing an embodiment wherein two kinds of character configurations can be selected;

Figures 18A to 18E each show another example of a character configuration;

Figure 19 is a block diagram of an embodiment wherein three kinds of character confi-

gurations can be selected; and

Figure 20 is a block diagram showing a still further embodiment of the character signal generating circuit, wherein a group of characters each of a desired configuration, can be displayed in a desired pattern.

First referring to Fig. 1, one example of a television game machine embodying the present invention will be described. A high frequency input, such as an antenna terminal, of a television receiver 1 is connected to receive a high frequency signal obtained through a connection lead 21 from a game machine main body 2. The television game of the embodiment shown is referred to as "block game". A video signal obtained from the game machine main body 2 is displayed as various symbols and numerals on a screen 10 of the television receiver 1. Fig. 1 shows a display in the initial condition of such a game. In such initial condition, a group of characters such as block symbols 11 arranged in six rows and fourteen columns arranged from the left end to the right end is displayed on the screen 10. A position controllable symbol such as a racket symbol 13 is displayed beneath the block symbol group 11 in the vicinity of the bottom of the screen 10. A moving symbol such as a ball symbol 12 is displayed so as to be movable throughout the screen 11. The upper end portion of the screen 10 above the block symbol group 11 is used as a first score display portion 14 for displaying the score of a game now in progress, a second score display portion 15 for displaying the score of the previous game, and a ball number display portion 16 for displaying the number of remaining balls which can be used in the game being played.

On the other hand, the game machine main body 2 comprises a serve switch 22 for causing the ball symbol 12, after it has disappeared from the screen 10, to again appear on the screen until the allowed number of balls has been used up. The main body 2 further comprises a power switch 23, a reset switch 24 to be depressed upon completion of one game for returning the display of various symbols and the like on the screen 10 to an initial condition, a game selection switch 25 for selecting among the kinds of games that can be played with the game machine main body 2 shown, and a ball number selection switch 26 for selectively setting the number of ball symbols that can be used by a player in one game. The game machine main body 2 further comprises a racket operation switch knob 27 for controlling the position of the racket symbol 13 in the horizontal direction on the television screen 10.

In playing a television game with such television game machine, first of all the power switch 23 is turned on, whereby the whole circuit of the game machine main body 2 is placed in an enabled state, whereupon the

reset switch 24 is depressed, so that various displays on the television screen 10 are brought to an initial condition. Such a state is shown in Fig. 1. More specifically, in the

5 initial condition, the block symbol group 11 is shown as a group of 84 block symbols. At the same time, the first score display portion 14 is reset to zero and the second score display portion 15 is enabled to display the score of the player who played the game immediately before the reset switch 24 was depressed, i.e. the score of the previous game. The ball number display portion 16 is enabled to display the number of balls that can be used by one player as set by the ball number selection switch 26, say, "5". Thereafter, the serve switch 22 is depressed. Then, the ball symbol 12 appears on the screen 10. The ball symbol 12 is caused to move freely throughout the television screen 10 under the control of a corresponding circuit portion included in the game machine main body 2. The movement of the ball symbol 12 is controlled such that if and when the ball symbol 12 collides with the racket symbol 13 or the block symbol 11 or a wall symbol, not shown, fixedly set around the television screen 10 the ball symbol 12 is repulsed as if the same is reflected so that the moving direction (and the speed) is altered. In this type of television game, the movement of the ball symbol 12 is controlled such that if and when the ball symbol 12 goes over the bottom end of the television screen 10 the same disappears from the screen 10 without being repulsed. The player can manipulate the operation knob 27 so that the racket symbol 13 is displaced in the horizontal direction on the screen, thereby to hit the ball symbol so that the latter is repulsed and prevented from disappearing. If and when the ball symbol 12 as repulsed by the racket symbol 13 or the wall symbol, not shown, collides with one of the block symbols in the block symbol group 11, the said block symbol is extinguished from the screen 10. Different scores are accorded in advance to the various block symbols, the scores being weighted in a predetermined manner. Each time a block symbol is extinguished, the score associated with the extinguished block is added to the total score, which is displayed on the score display portion 14. Accordingly, a player must control the operation knob 27 to quickly displace the racket symbol 13, thereby to prevent the ball symbol 12 from disappearing from the screen 10 and to make the ball symbol 12 collide with any one of the block symbols 11. This is an example of a block game.

The present invention is directed to an apparatus for displaying a group of characters, such as block symbols, which can be advantageously utilized in such a television game machine. More specifically, the present invention is directed to an apparatus for displaying various symbols, particularly the grouped

block symbols 11 as shown in Fig. 1.

Fig. 2 is a block diagram showing the circuitry included in the game machine main body 2 shown in Fig. 1. The circuitry comprises a clock generator 201, which may comprise a crystal oscillator, adapted to provide a reference clock CL1 of the frequency commensurate with the horizontal scanning frequency of a television receiver. The reference clock CL1 from the clock generator 201 is applied to a main horizontal counter 202. The horizontal counter 202 comprises a 114-nary counter connected to receive the reference clock CL1. The count value in the main horizontal counter 202 is applied in a bit parallel fashion to a horizontal timing decoder 203. The horizontal timing decoder 203 may comprise a read-only memory structured to decode the count value in the main horizontal counter 202 to provide the decoded output. The output of the horizontal timing decoder 203 is applied to a memory, not shown in Fig. 2 and described subsequently, included in a character signal generating circuit 3 as addressing signals CH1 to CH14 representing the addresses in the horizontal direction or in terms of the columns of the memory. The horizontal timing decoder 203 also provides a horizontal timing signal TH for each horizontal timing to the character signal generating circuit 3. The horizontal timing decoder 203 decodes the count value in the main horizontal counter 202 to provide a horizontal synchronizing signal HSYNC of a television receiver and to provide one pulse for each horizontal scanning line, i.e. one circulation of the main horizontal counter 202. The above described pulse is applied to a main vertical counter 204 as a reference clock CL2 for use in a vertical synchronization circuit. The main vertical counter 204 is structured as a 262-nary counter, for example. The count value in the main vertical counter 204 is applied in a bit parallel fashion to a vertical timing decoder 205. The vertical timing decoder 205 may comprise a read-only memory and decodes the count value in the main vertical counter 204 to provide a vertical synchronizing signal VSYNC of a television receiver. At the same time, both the horizontal timing decoder 203 and the vertical timing decoder 205 provide a score displaying horizontal position signal PH and a score displaying vertical position signal PV, respectively, for use in the score display portions 14 and 15 (and the ball number display portion 16) shown in Fig. 1, for example. At the same time, the decoders 203 and 205 provide the time, the decoders 203 and 205 provides the horizontal and vertical position signals WH and WV for the wall symbol, not shown in Fig. 1. The score display horizontal and vertical position signals PH and PV are both applied to a score symbol signal generating circuit 223. The horizontal and vertical wall signals WH and WV are both

applied to two inputs of an AND gate 211. The output from the AND gate 211 is applied to a collision detecting circuit 6 to be described subsequently as a wall symbol signal and is also applied to a video synthesizing circuit 231.

In the embodiment shown, the vertical addressing signal for the character signal generating circuit 3 is obtained from a character vertical timing signal generating circuit 4. The character vertical timing signal generating circuit 4 is shown in more detail in Fig. 3. Referring to Fig. 3, the character vertical timing signal generating circuit 4 will be described in detail. The vertical addresses of the memory, to be described subsequently, of the character signal generating circuit 3 are designated responsive to the output of the separately provided timing signal generating circuit 4, because it is intended to displace the character symbol group 11 shown in Fig. 1 as a whole in the vertical direction on the screen in the embodiment shown. As to be described in more detail subsequently, according to an example of a game, when the ball symbol 12 collides with a specified block symbol in the block symbol group 11, the display is controlled such that the block symbol group 11 as a whole is moved in the vertical direction such as downward as if the block symbol group 11 falls. If it is not necessary to displace the character symbol group 11 in the vertical direction such as downward, then the vertical timing decoder 205 may be structured in the same manner as in the case of the horizontal timing decoder 203, so that the vertical addressing signal may be applied fixedly to the character signal generating circuit 3.

Referring to Fig. 3, the character vertical timing signal generating circuit 4 is connected to receive a specified character destroying signal SCD obtained from the collision detecting circuit 6. The character destroying signal SCD is applied to a variable number control circuit 41. The variable number control circuit 41 is structured, for example, such that the same is responsive to the signal SCD being the high level or the logic one to vary a preset value in a character subvertical counter 42 to move the character symbol group 11 shown in Fig. 1 in the vertical direction on the screen and is responsive to the signal SCD being the low level or the logic zero to fix a preset value in the character subvertical counter 42. The signal from the variable number control circuit 41 is applied to the subvertical counter 42 for the character symbol group. The vertical reference clock CL2 is applied to the count input of the subvertical counter 42. The count value in the subvertical counter 42 is applied in a bit parallel fashion to a character vertical position decoder 43. The vertical position decoder 43 may comprise a read-only memory, as in the case of the horizontal timing decoder

203 and the vertical timing decoder 205. The vertical position decoder 43 is adapted to decode the count value in the subvertical counter 42 to provide the vertical addressing signals CV1 to CV6 (and CV7) for the character signal generating circuit 3 in association with the count value. At the same time, the vertical position decoder 43 provides a vertical timing signal TV for each vertical timing. The variable number control circuit 41 is responsive to the signal SCD being the high level or the logic one to vary a variable set value associated with the number of the scanning lines in the subvertical counter 42. As a result, the character group 11 shown in Fig. 1 is caused to move downward on the screen 1. If and when the signal SCD is the low level or the logic zero, the subvertical counter 42 functions as a 262-nary counter in a fixed manner.

In order to display a ball symbol 12 on the screen 10 as shown in Fig. 1, a ball symbol signal generating circuit 5 is provided. The ball symbol signal generating circuit 5 is shown in more detail in Fig. 4. The ball symbol signal generating circuit 5 shown in Fig. 4 comprises a horizontal direction circuit 51 and a vertical direction circuit 52. The circuits 51 and 52 each comprise variable number control circuits 511 and 521, a ball symbol subhorizontal counter 512 and a ball symbol subvertical counter 522, and a ball symbol horizontal position decoder 513 and a ball symbol vertical position decoder 523, respectively. The ball symbol signal generating circuit 5 is connected to receive the reference clock CL1 from the block generating circuit 201 and a horizontal collision signal HC from the collision detecting circuit 6 for use in the horizontal direction circuit 51 and the vertical reference clock CL2 from the horizontal timing decoder 203 and a vertical collision signal VC from the collision detecting circuit 6 for use in the vertical direction circuit 52. The ball symbol signal generating circuit 5 is further connected to receive a signal BD/E obtained from the collision detecting circuit 6 and representing whether or not the ball symbol is to be displayed.

Since the horizontal direction circuit 51 and the vertical direction circuit 52 are structured in substantially the same manner, only the horizontal direction circuit 51 will be described, while a description of the vertical direction circuit 52 will be omitted for simplicity. The ball symbol subhorizontal counter 512 is connected to receive the reference clock CL1 at the count input thereto. The preset value associated with the number of the horizontal scanning lines and the speed of the counting operation of the ball symbol subhorizontal counter 512 are controlled by the variable number control circuit 511. The count value in the subhorizontal counter 512 is applied in a bit parallel fashion to the ball symbol horizontal position decoder 513. The

decoder 513 is structured such that when the count value in the counter 512 becomes a given value an output is obtained therefrom.

Thus, as the preset value and the counting speed of the subhorizontal counter 512 are varied by the variable number control circuit 511, the phase and synchronization of the ball symbol horizontal position signal obtained from the decoder 513 are accordingly

changed. The ball symbol horizontal position signal obtained from the decoder 513 is applied to one input of a three-input AND gate 53. Another input of the AND gate 53 is connected to receive a ball symbol vertical

position signal obtained from the ball symbol vertical position decoder 523. The ball display/extinguish signal BD/E obtained from the collision detecting circuit 6 is applied to the remaining inverted input of the AND gate 53.

Accordingly, if and when the horizontal direction collision signal HC and/or the vertical direction collision signal VC are obtained from the collision detecting circuit 6, a ball symbol signal is obtained from the AND gate 53 in which the moving direction and the moving speed of the ball symbol 12 shown in Fig. 1 have been changed. The ball symbol signal is applied to the collision detecting circuit 6 and also to the video synthesizing circuit 231.

Fig. 5A is a block diagram showing in detail a racket symbol signal generating circuit 8. The racket symbol signal generating circuit 8 comprises a series connection of a variable resistor 81 the resistance value of which may be varied by operation of the racket operation knob 27 shown in Fig. 1 and a capacitor 82.

The junction of the variable resistor 81 and the capacitor 82 is connected through a transistor 83 to the ground and is connected to an amplifier 84. The input electrode of the transistor 83 is connected to receive a horizontal synchronizing signal HSYNC obtained from the horizontal timing decoder 203. The amplifier 84 is supplied with a given slice

level voltage eV . The output of the amplifier 84 is applied to a data input of flip-flop 851 included in a racket width generating circuit 85. The flip-flop 851 and another flip-flop 852 and a shift register 854 are supplied with

the reference clock CL1. The output of the flip-flop 851 is applied to a data input of the flip-flop 852 and is also applied to one input of an AND gate 853. Another input of the AND gate 853 is connected to receive the

inverted output of the flip-flop 852. The output of the AND gate 853 is applied to an input of the shift register 854. The shift register 854 serves as a serial-parallel converter to provide the converted output in a bit

parallel fashion. The bit parallel output of the shift register 854 is withdrawn through an OR gate 86 and the output of the OR gate 86 is applied to one input of an AND gate 87. (Fig. 2) as a racket horizontal position signal RH.

Another input of the AND gate 87 is con-

nected to fixedly receive the racket symbol vertical position signal RV from the vertical timing decoder 205.

Now referring to Fig. 5B, the operation of the Fig. 5A circuit will be briefly described. The capacitor 82 is discharged responsive to the horizontal synchronizing signal HSYNC (Fig. 5B(A)), whereupon the capacitor 82 is charged thereafter through the variable resistor 81. Accordingly, a saw-tooth wave voltage (Fig. 5B(B)) is generated, which has a waveform including an abrupt fall defined by discharging of the capacitor 82 is synchronism with the horizontal synchronizing signal

HSYNC and a ramp rise defined by charging of the capacitor 82 with a time constant determined by the variable resistor 81 and the capacitor 82. The saw-tooth wave voltage is sliced at a predetermined slice level of the

amplifier 84 and the output (Fig. 5B(C)) is applied to the racket width generating circuit 85. The racket width generating circuit 85 serves to perform digital differentiation, thereby to provide in a bit parallel fashion a

signal representing the width of the racket from the shift register 854 included in the racket width generating circuit 85. Thus, the horizontal position signal RH of the racket symbol having a racket width determined by the racket width generating circuit 85 is withdrawn from the OR gate 86. By manually operating the knob 27 shown in Fig. 1, the resistance value of the variable resistor 81 can be changed and accordingly the gradient of the ramp rise of the saw-tooth wave voltage applied to the amplifier 84 can be changed.

Accordingly, the phase position of the saw-tooth wave voltage as sliced by the amplifier 84 is accordingly changed and thus the phase of the horizontal position signal RH of the racket symbol obtained from the OR gate 86 is also changed. As a result, the racket symbol 13 having the width determined by the circuit 85 is position controllable in the horizontal

direction by manually operating the knob 27 to change the resistance value of the variable resistor 81. The racket symbol signal for displaying the racket symbol is obtained from the AND gate 87 of the racket symbol signal

generating circuit 8 and is applied to the collision detecting circuit 6 and also to the video synthesizing circuit 231.

Fig. 6 is a block diagram showing an outline of a major portion of the collision detecting circuit 6 and the game control circuit 7. The game control circuit 7 is connected to the serve switch 22, reset switch 24 and the game selection switch 25 shown in Fig. 1.

The game control circuit 7 comprises a one picture frame pulse generating circuit 71 responsive to depression of the reset switch 24 to provide a one picture frame pulse. The one picture frame pulse generating circuit 71 is structured to generate a one picture frame pulse of the high level during one recircula-

tion period of the main vertical counter 204. The one picture frame pulse obtained from the one picture frame pulse generating circuit 71 is applied as a write enable input to the character generating circuit 3, as to be more fully described subsequently, and also to an AND gate 65 included in the collision detecting circuit 6 as one input thereto. The game control circuit 7 comprises a one-pulse generating circuit 72 responsive to depression of the serve switch 22 to generate one pulse. The pulse obtained from the one-pulse generating circuit 72 is applied, as a game starting pulse, to the character symbol generating circuit 3, the character vertical timing signal generating circuit 4, the ball symbol signal generating circuit 5, the collision detecting circuit 6, a score counter 222 and the like, thereby to return them to an initial condition.

The game selection switch 25 may comprise a slide switch, so that a change of an on contact position can select the kind of game to be played. The selection signal obtained from the switch 25 is applied to the character symbol signal generating circuit 3, for example. At the same time, the signal representing a selected kind of game is applied as inverted inputs to OR gates 73 and 74. These OR gates 73 and 74 are provided to apply the signals to the collision detecting circuit 6 such that the collision condition to be detected by the collision detecting circuit 6 may be changed in association with the selected kind of game.

The collision detecting circuit 6 is structured to detect coincidence of the ball symbol signal and the character symbol signal, the racket symbol signal and the wall symbol signal. Coincidence of these last mentioned signals with the ball symbol signal can be observed as a collision of a ball symbol 12 with the block in the block group 11, the racket symbol 13 or the wall symbol, not shown. In order to detect such coincidence and thus collision, the collision detecting circuit 6 comprises AND circuits 61, 62 and 63. The AND circuit 61 is connected to receive the ball symbol signal and the character symbol signal. The AND circuit 62 is connected to receive the ball symbol signal and the wall symbol signal, the wall symbol signal and the racket symbol signal, respectively. There are AND circuits 61, 62 and 63 for both the AND circuits 61, 62 and 63 derive the logical products of their inputs to detect coincidence of the ball symbol signal with the character symbol signal, the wall symbol signal and the racket symbol signal respectively. There are AND circuits 61, 62 and 63 for both the vertical direction and the horizontal direction, and the outputs thereof are withdrawn separately. However, in Fig. 6 this has been illustrated by using only one line to denote signal paths for both the vertical direction and the horizontal direction for simplicity of illus-

tration. The collision detected signals obtained from these AND circuits 61, 62 and 63 are applied to an OR circuit 64. Although there are OR circuits 64 for both the horizontal direction and the vertical direction, again only one is shown in the figure for simplicity of illustration. The output of the AND circuit 61 for detecting coincidence of the ball symbol signal and the character symbol signal is further applied to OR gate 66. Another input of the OR gate 66 is connected to receive the output of an AND gate 65. One input of the AND gate 65 is connected to receive the reference clock CL1. The output of the OR gate 66 is applied to a random-access memory, not shown, included in the character signal circuit 3 as a read/write command signal R/W. At the same time, the output of the AND gate 61 is applied to a score pulse generating circuit 221. The horizontal direction collision detected signal HC and the vertical direction collision detected signal VC obtained from the OR circuit 64 are applied to the ball symbol signal generating circuit 5.

The output from the OR gate 73 or 74 of the game control circuit 7 is applied to the AND circuits 61, 62 and 63 thereby to change the coincidence detecting condition achieved by these circuits 61, 62 and 63.

Referring again to Fig. 2, the score pulse generating circuit 221 is connected to receive a coincidence detected output of the ball symbol signal and the character signal obtained from the collision detecting circuit 6 and also to receive the addressing signal obtained from the character vertical timing signal generating circuit 4. Accordingly, a train of pulses corresponding in number to the score of the character corresponding to the address is provided from the score pulse generating circuit 221. The score pulse train obtained from the score pulse generating circuit 221 is counted by the score counter 222 and the count value is applied to the score symbol signal generating circuit 223. The score symbol signal generating circuit 223 provides a signal for displaying the score as shown in Fig. 1, in response to the horizontal position signal PH and the vertical position signal PV, to the video synthesizing circuit 231.

The video synthesizing circuit 231 receives the ball symbol signal, the wall symbol signal, the racket symbol signal, the character signal and the score symbol signal, thereby to compose them to provide a composite brightness signal. The above described signals are also applied to a chrominance circuit 232. Accordingly, the chrominance circuit 232 generates a chrominance signal in association with these input signals which is applied to a phase modulation circuit 233. The phase modulation circuit 233 generates a color signal as phase modulated responsive to the reference clock CL1 obtained from the clock generating circuit

201. The color signal obtained from the phase modulation circuit 233, the brightness signal obtained from the video synthesizing circuit 231, and a sound signal obtained from a sound signal generating circuit 234 for generating a sound signal responsive to a collision detected signal obtained from the collision detecting circuit 6 are applied to a synthesizing circuit 235, whereby these signals are combined in a television high frequency signal. The television high frequency signal output from the synthesizing circuit 235 is applied to a television receiver (Fig. 1) through the connection lead 21 (Fig. 1).

Fig. 7 is a diagrammatic view showing storing regions in a random-access memory 31 included in the character signal generating circuit 3. The random-access memory 31 comprises storing regions each constituting one bit. The number of regions corresponds to the number of block symbols included in the block group 11 shown in Fig. 1. More specifically, the random-access memory 31 comprises 84 storing regions and thus 84 bits, arranged in fourteen columns in the horizontal direction and six rows in the vertical direction. The random-access memory 31 is loaded with the logic one in the corresponding bit to represent that the corresponding character or the block symbol is to be displayed and with the logic zero in the corresponding bit to represent that the corresponding character or the block symbol is not to be displayed. In the initial condition of a game, the random-access memory is loaded with the logic one in all the bit positions by means of a write control means, as to be described subsequently.

If and when a repulsing block symbol (character) group 11' is to be displayed, beneath the racket symbol 13 at the bottom of the screen, as shown by a dotted line in Fig. 1, the arrangement of the block symbols must comprise seven rows in the vertical direction, and hence the total number of storing regions must be 98 bits. The repulsing block symbol group 11' serves to prevent the ball symbol 12 from disappearing when a player fails in hitting the ball symbol 12 with the racket symbol 13. More specifically, without the block symbol group 11', if the ball symbol 12 is not hit and thus not repulsed by the racket symbol 13 it ultimately reaches the bottom end of the television picture screen 10 to disappear therefrom. However, with the repulsing block symbol group 11' provided, if the ball symbol 12 is not repulsed by the racket symbol 13 it reaches one of the block symbols in the block symbol group 11' and is repulsed thereby, while the said block is extinguished, so that the ball symbol 13 not hit by the racket symbol 13 is saved by the block symbol in the block symbol group 11' only one time and the ball symbol 12 is repulsed toward the character group 11. However, as described previously, the block symbols in the

block symbol group 11' shown in a dotted line are extinguished when the ball symbol 12 collides therewith and accordingly the ball symbol 12 moving downward and not hit by the racket symbol 13 is allowed to pass downward at the place where the block symbol of the block symbol group 11' is extinguished.

The random-access memory 31 included in the above described character signal generating circuit 3 is addressed by the horizontal addressing signals CH1 to CH14 and the vertical addressing signals CV1 to CV6 (and CV7) obtained from the horizontal timing decoder 203 and the character vertical timing signal generating circuit 4.

More specifically, the horizontal timing decoder 203 does not provide the horizontal address signal during a time period of the count value "0" to "29" in the main horizontal counter 202 when the horizontal scanning is progressing. The decoder 203 does provide a horizontal address signal CH1 (Fig. 8A) specifying the horizontal directional address No. 1 of the random-access memory 31 during the period of the count value "30" to "33" in the counter 202 (i.e. a period corresponding to the horizontal directional width of the character or block symbol in the first column from the left side in the character group 11). Further, the decoder 203 does not provide an addressing signal at the count value of "34" of the main horizontal counter 202 and provides an addressing signal CH2 (Fig. 8A) for specifying the horizontal directional address No. 2 during the time period of the count value "35" to "38" in the main horizontal counter 202. The decoder 203 does not provide an addressing signal at the count value of "39" of the main horizontal counter 202. Similarly, thereafter, the decoder 203 repeats an operation wherein the decoder 203 provides each of addressing signals CH3...CH14 specifying the horizontal direction addresses during the time periods of four successive counts of the horizontal counter 202 and the decoder 203 does not provide an addressing signal during a succeeding time period for a count of one with the result that fourteen pulses of the addressing signals CH1 to CH14 are applied to the random-access memory 31 in a time sequential manner and such an operation is repeated for each scanning line.

The vertical position decoder 43 (Fig. 3) included in the character vertical timing signal generating circuit 4 does not provide a vertical addressing signal during the time period of the count value "0" to "64" in the main vertical counter 204 and does provide a vertical addressing signal CV1 (Fig. 8B) specifying the vertical address No. 1 in the random-access memory 31 during a time period of the count value "65" to "70" in the counter 204. The decoder 43 does not provide a vertical addressing signal during a time period

of the count value "71" and "72" in the main vertical counter 204 and does provide the vertical addressing signal CV2 during the time period of the count value "73" to "78"

5 in the main vertical counter 204. Thereafter the decoder 43 does not provide a vertical addressing signal during a time period of the count value "79" and "80". Similarly thereafter, the decoder 43 provides the vertical
10 addressing signals CV3 to CV6 (and CV7) for specifying the vertical addresses No. 3 to 6 (and No. 7) in the random-access memory during time periods of the count values shown in Fig. 8B. Thus, the information stored in the
15 respective storing regions or bits in the random-access memory 31, addressed in the horizontal direction by the decoder 203 and addressed in the vertical direction by the decoder 43, is read out in a bit sequence
20 from the output terminal (out), and is used as a character signal.

Meanwhile, it is necessary to load the logic one in an initial condition of a game in all the bits or storing regions in the random-access
25 memory 31 included in the circuit 30. Therefore, writing or loading of the logic one in the respective bits in the random-access memory 31 for displaying the corresponding characters will be described in the following. To that
30 end the reset switch 24 shown in Fig. 6 is depressed. Then, the one-picture frame pulse of the logic one is obtained from the one-picture frame pulse generating circuit 7 during one vertical scanning period. Accordingly,
35 the said signal is applied from the collision detecting circuit 6 to the circuit 30 as a write input (in). At the same time, the one-picture frame pulse obtained from the one-picture frame pulse generating circuit 71 is applied to
40 the AND gate 65 of the collision detecting circuit 6. Accordingly, an output of the high level or the logic one is obtained from the AND gate 65 for each pulse of the reference clock CL1. Therefore, the output of the logic
45 one is obtained from the OR gate 66 included in the circuit 6 for each of the reference clock CL1 pulses and is applied to the random-access memory 31 as a write command signal. The random-access memory 31 is ad-
50 dressed by the horizontal addressing signals CH1 to CH14 obtained from the horizontal timing decoder 203 and the vertical addressing signals CV1 to CV6 (and CV7) obtained from the decoder 43 of the vertical timing
55 signal generating circuit 4. Accordingly, upon depression of the reset switch 24 by a player after completion of a play of one game, the logic one is loaded in the respective bits as sequentially addressed in the random-access
60 memory 31 during the subsequent one picture frame pulse period.

When the one-picture frame pulse obtained from the one picture frame pulse generating circuit 71 becomes the low level or the logic
65 zero, the low level or the logic zero is applied

to the write input (in). On the other hand, a read command of the low level or the logic zero is applied as a read/write input of the random-access memory 31. Accordingly,
70 thereafter the information is sequentially read out from the bits sequentially addressed by the horizontal timing decoder 203 and the vertical position decoder 43 at the output terminal (out) from the random-access mem-
75 ory 31 and thus from the character signal generating circuit 3. The character signal as read is applied to the collision detecting circuit 6 and the video synthesizing circuit 231. Accordingly, the characters or the block sym-
80 bols are displayed on the television screen 10 as shown in Fig. 1. As described previously, the collision detecting circuit 6 serves to detect collision of the ball symbol with the wall symbol, the racket symbol and the block sym-
85 bols.

If and when the ball symbol 12 collides with the character on the screen 10, the output of the logic one is obtained from the AND circuit 61 of the collision detecting cir-
90 cuit 6. The output of the AND circuit 61 is applied through the OR gate 66 to the circuit 30 as a write command of the random-access memory 31. On the other hand, since the input terminal (in) is already at the logic zero,
95 the logic zero is written in the bit in the random-access memory 31 corresponding to the character with which the ball symbol 12 has collided. Accordingly, thereafter the character symbol is extinguished from the televi-
100 sion screen 10. At the same time, the output of the AND circuit 61 is applied to the score pulse generating circuit 221 and accordingly the score of a game now in progress is added to the score display 14 on the television
105 screen and the sum thereof is displayed.

As described previously, in the case where the information, i.e. the logic one, representing that the character in the character group is to be displayed is written in the random-
110 access memory 31, the logic one may be simply written in all the bit positions in the random-access memory 31. Therefore, a conventional memory such as a read-only memory for fixedly storing an arrangement pattern
115 of characters can be dispensed with and hence the necessity for a write control circuit for transferring information from such a read-only memory to a video random-access memory is eliminated. As a result, the circuit
120 configuration can be extremely simplified and an initial condition of a display of a character group can be simply achieved. Furthermore, since the random-access memory 31 may simply comprise a number of bits correspond-
125 ing to the number of characters in the character group, the necessary storage capacity of the random-access memory 31 can be reduced to approximately 1/350 as compared with a case where the display information
130 signal is stored in a memory having a storage

capacity corresponding to all the picture elements on the screen. As a result, the use of apparatus according to the present invention can considerably reduce the cost of the memory. Another feature of the embodiment is that since in reading information stored in the random access memory 31 the memory 31 is addressed in a hardware manner in accordance with the horizontal directional position of the scanning lines and the vertical directional position, the necessity for performing a reading operation by the use of a microprocessor is eliminated, which reduces the number of operation steps carried out by a microprocessor if one is provided, and accordingly makes it possible to utilize a microprocessor of a lower operation speed and hence of a less expensive cost.

Although in the above described embodiment a cathode ray tube used in combination with a television receiver was described as an example of a display operated by horizontal scanning and vertical scanning, it is needless to say that any other type of display using horizontal scanning and vertical scanning may be utilized. Furthermore, although the above described embodiment was described for a case where rectangular block symbols are displayed by way of an example of characters, such block symbols may be of any other configuration, such as a square, for example. Furthermore, although in the foregoing one character was allotted to one bit in a random-access memory in order to store a character symbol, other arrangements are possible. For example, a square character may be stored in one bit and a rectangular character corresponding to an arrangement of two squares in the horizontal direction may be stored using two bits. In this case, the circuit may be configured such that, to produce a rectangular character, a horizontal addressing signal is generated to read two bits corresponding to two square characters with no horizontal addressing signal for the following one bit to provide a space. Even in this type of arrangement, the necessary storage capacity of the random-access memory can be considerably reduced as compared with a conventional system. The circuit could be configured to permit switching between a display mode in which rectangular characters are displayed and a mode in which square characters are displayed.

Fig. 9 is a block diagram showing another embodiment of the present invention. The embodiment shown is structured to permit changing of the pattern of the character group. To that end, a read-only memory 32 for storing arrangement patterns is provided in addition to the random-access memory 31 shown in Fig. 7 in the character signal generating circuit 3 shown in Fig. 2. The read-only memory 32 as well as the random-access memory 31 is structured to be addressed by

the horizontal addressing signals CH1 to CH14 obtained from the horizontal timing decoder 203 and the vertical addressing signal CV1 to CV6 (and CV7) obtained from the vertical position decoder 43 included in the character vertical timing signal generating circuit 4. The read output OUT from the random-access memory 31 is applied to one input of an AND gate 33. The read output of the read-only memory 32 for storing arrangement patterns is applied to an inverted input of the AND gate 33. The output of the AND gate 33 is withdrawn as a character symbol signal and is applied to the collision detecting circuit 6 and the video synthesizing circuit 231 (Fig. 2).

Fig. 10A is a view showing an example of an arrangement pattern of the character group. The arrangement pattern 11a comprises a pattern of a reversed trapezoid shape wherein the characters have been deleted starting from the third line from the top downward one by one at both sides sequentially. Such pattern 11a is stored in the arrangement pattern storing read-only memory 32. The read-only memory 32 is structured to comprise a plurality of bits arranged in plural rows and plural columns corresponding to plural rows of characters and plural columns of characters in the character group, as shown in Fig. 10B. The logic zero is written in the bits corresponding to the characters being displayed, while the logic one is written in the bits corresponding to the characters not being displayed.

The character symbol signal is generated from the circuit 3 by the use of the random-access memory 31, the arrangement pattern storing read-only memory 32 and the AND gate 33, as described previously. In an initial condition, the random-access memory 31 is loaded with the logic one in all the bits, as described previously. The writing operation is performed in the same manner as described previously. In order to generate a character signal from the circuit 3, a read command signal is applied to the random access memory 31. Then the random-access memory 31 and the read-only memory 32 are simultaneously addressed by the same addressing signals. The output read from the random-access memory 31 and the inverted output read from the read-only memory 32 are ANDed by the AND gate 33, i.e. the logical product of these outputs is derived. It is pointed out that if and when the read-only memory 32 is structured such that, as in the case of the random-access memory 31, the logic one is written in the bits corresponding to the characters being displayed, then the output read from the random-access memory 31 and the output read from the read-only memory 32 may be ANDed, without the necessity for inverting the output read from the read-only memory 32. The output of the AND gate 33 is used as a

character signal. Accordingly, in the case where the logic one has been written in a given bit in the random-access memory 31 and the logic one has been written in the corresponding bit in the read-only memory 32, the output from the AND gate 33 becomes the logic zero and accordingly the character corresponding to the said bit is not displayed on the screen 10 (Fig. 1). On the other hand, in the case where the logic zero has been written in a given bit in the random-access memory 31, the output of the AND gate 33 becomes the logic zero, irrespective of the logical state in the corresponding bit in the read-only memory 32. Conversely, if and when the logic one has been written in a given bit in the random-access memory 31 and the logic zero has been written in the corresponding bit in the read-only memory 32, then the output of the AND gate 33 becomes the logic one. Accordingly, the character corresponding to the said bit is displayed on the screen 10. Accordingly, it would be appreciated that in an initial condition an arrangement pattern as shown in Fig. 10A is displayed based on the information stored in the read-only memory 32 as shown in Fig. 10B.

When a block game machine is implemented using a character signal generating circuit 3 using the above described random-access memory 31, the read-only memory 32 and the AND gate 33, the way of playing the game may be substantially the same as described previously, in which when the ball symbol 12 collides with the character the character is extinguished on the screen 10, while the score corresponding to the extinguished character is added to the total score which is displayed. Fig. 11A shows an example of a different arrangement pattern of the character group and Fig. 11B diagrammatically shows an arrangement of bits in the read-only memory 32 corresponding to the arrangement pattern shown in Fig. 11A.

Preferably, the circuit is configured such that either of the arrangement patterns 11A and 11B shown in Figs. 10A and 11A may be selected. Fig. 12 is a block diagram showing another embodiment of the character signal generating circuit 3 performing such selective display among a plurality of arrangement patterns. The embodiment shown is structured such that the four characters shown hatched in each of Figs. 10A and 11A blink so as to attract the attention of the player. Referring to Fig. 12, the arrangement pattern storing read-only memory 32 comprises 168 bits in 12 rows in the vertical direction and 14 columns in the horizontal direction ($12 \times 14 = 168$ bits). The same vertical addressing signals CV1 to CV6 are applied to a plurality of rows, as shown in Fig. 12. The horizontal addressing signals CH1 to CH14 are individually applied, as described previously. The informa-

tion stored in the upper five rows V1 to V5 in the read-only memory 32 is denoted as a region A, the information stored in the sixth row V6 is denoted as a region B, the information stored in the seventh to tenth rows V7 to V10 is denoted as a region C, and the information stored in the eleventh and twelfth rows V11 and V12 is denoted as a region D, respectively. Referring to Fig. 12, the blank storage regions are ones in which the logic zero has been loaded. The output read from the region A in the read-only memory 32 is applied to one input of an AND gate 301 included in the circuit 3. The output read from the region B in the read-only memory 32 is applied to one input of an AND gate 302. Similarly, the output read from the region C and the output read from the region D are applied to one input of AND gates 303 and 304, respectively. An arrangement pattern selection switch 251 is provided to be switchable in a ganged fashion with the game selection switch 25 shown in Fig. 6, for example. The contact 251s of the selection switch 251 is connected to the high level or the logic one and the contact 251a of the selection switch 251 is connected to the other input of the AND gates 301 and 302. The contact 251b of the selection switch 251 is connected to the other input of the AND gates 303 and 304. The outputs of the AND gates 301 and 303 are both connected to the input of an OR gate 305 and the output of the OR gate 305 is applied, after an inversion by an inverter 307, to an AND gate 33. The AND gate 33 is structured as a 3-input gate. Another input of the AND gate 33 is connected to receive the output as sequentially read from the random-access memory 31, as described previously. The outputs of the AND gates 302 and 304 are both applied to an OR gate 306. The output of the OR gate 306 is applied to one input of an AND gate 308. Another input of the AND gate 308 is connected to receive pulses from a pulse generator 309. The pulse generator 309 is provided to cause a specified character to blink and the frequency of the pulses is selected such that the blink of a specified character can be visually observed. The output of the AND gate 308 is applied to the remaining input of the AND gate 33. The output of the AND gate 33 is withdrawn as the output of the circuit 3, i.e. a character signal.

The bit position corresponding to the character which is caused to blink is loaded with the logic one representing that the character is to be caused to blink. Now let it be assumed that the arrangement pattern shown in Fig. 10A is selected by the switch 251. Then the AND gates 301 and 302 corresponding to the regions A and B including the information associated with the pattern 11A are enabled. The corresponding bits are sequentially addressed by the horizontal addressing signals

CH1 to CH14 and the vertical addressing signals CV1 to CV6 and accordingly a read signal is obtained. The read signal obtained from the region A is inverted by the inverter

- 5 307 and the output signal is obtained, wherein the logic one represents that the corresponding characters are to be displayed and the logic zero represents that the corresponding characters are not to be displayed.
- 10 The read signal obtained from the region B is withdrawn as a signal corresponding to the characters that are to be caused to blink and the said signal representing the blinking characters and a blink displaying pulse obtained
- 15 from the pulse generator 309 are ANDed by the AND gate 308 and the output of the AND gate 308 is applied to the AND gate 33. The output of the inverter 307, the output of the AND gate 308 and the read-out signal from
- 20 the random-access memory 31 are ANDed by the AND gate 33. Accordingly, the characters corresponding to the bits wherein the logic one has been loaded in the region A are not displayed and the characters corresponding to
- 25 the bits wherein the logic one has been loaded in the region B are caused to blink. Thus, by selection by means of the selection switch 251, the character group in the arrangement pattern shown in Fig. 10A can be
- 30 selectively displayed.

Similarly, in order to display the arrangement pattern 11B shown in Fig. 11A, the selection switch 251 is switched to the contact 251b and then the character group of the pattern shown in Fig. 11A is displayed on the screen 10 in a similar manner.

According to the Fig. 12 embodiment, a plurality of kinds of arrangement patterns of the character group 11 can be selectively

40 displayed, using a read-only memory of a relatively small storage capacity. Accordingly, versatility of the apparatus can be achieved by employing such a circuit configuration in a character signal generating circuit of a television game machine.

Although in the foregoing the storage areas for each of the patterns 11A and 11B comprised six rows of storing regions, if the patterns 11A and 11B contain rows of the same content (for example the seventh row V7 and the tenth row V10 of storing regions are the same) the circuit may be structured such that such rows V7 and V10 are replaced by a common row which may be addressed by different vertical addressing signals, in which case the storage capacity of the read-only memory 32 can be further decreased. It is pointed out that this could also be achieved for different rows of the patterns

50 11A and 11B.

The embodiment shown in Fig. 12 was described as structured such that the random-access memory included in the character symbol signal generating circuit 3 is loaded with the logic one in all the bit positions in an

initial condition, whereupon in reading the same the output of the random-access memory 31 and the output of the arrangement pattern storing read-only memory 32 are

- 70 ANDed to provide a character symbol signal. However, alternatively, the circuit may be configured such that the random-access memory 31 is loaded with the logic one or logic zero as a function of the arrangement pattern stored in the read-only memory 32. Fig. 13 is a block diagram showing an embodiment employing such an alternative circuit configuration. In the case of the embodiments shown in Figs. 9 and 12, in writing information in an
- 75 initial condition, the signal of the one-picture frame pulse generating circuit 71 (Fig. 6) is applied as a write input IN. By contrast, in the Fig. 13 embodiment, the output of the one-picture frame pulse generating circuit 71 is
- 80 applied to an AND gate 310. Another input of the AND gate 310 is connected to receive the output read from the arrangement pattern storing read-only memory 32. The output of the AND gate 310 is applied as a write input
- 85 IN of the random-access memory 31. Accordingly, the random-access memory 31 is loaded in the bit positions addressed by the horizontal addressing signals CH1 to CH14 and the vertical addressing signals CV1 to CV
- 90 6 with the data stored in the read-only memory 32. The read output OUT of the random-access memory 31 is withdrawn as the output of the circuit 3 and thus the character symbol signal. Accordingly, in an initial condition, the character group of the arrangement pattern such as the pattern 11A shown in Fig. 10A or the pattern 11B shown in Fig. 11A can be displayed on the screen 10 (Fig. 1) in an initial condition, as in the case of the embodiment shown in Fig. 12.

Although in the above described embodiments the characters being displayed on the screen 10 were of a rectangle shape, the characters may be of any configuration.

- 110 Fig. 14 is a block diagram showing an embodiment for defining a configuration of characters. The embodiment shown comprises a read-only memory 34 for storing a character configuration in addition to the random-access memory 31 in the character signal generating circuit 3 shown in Fig. 2, for example. The read-only memory 34 is adapted to be addressed by eight-bit ring counters or shift registers 35 and 36. The logical product of
- 115 the read output of the random-access memory 31 and the read output of the character configuration storing read-only memory 34 is derived by applying the outputs to the inputs of an AND gate 37, and the output of the
- 120 AND gate 37 is withdrawn as the output of the circuit 3 and thus as the character symbol signal. The random-access memory 31 is supplied with the horizontal addressing signals CH1 to CH14 obtained from the horizontal
- 125 timing decoder 203 and the vertical address-
- 130

ing signals CV1 to CV6 obtained from the vertical position decoder 43 (Fig. 3). The shift register 35 is supplied with the reference clock CL1 as a shift clock pulse and the input thereof is connected to receive the horizontal timing signal TH (Fig. 2) obtained from the horizontal timing decoder 203. The timing signal TH is obtained by extracting the leading edges of the horizontal addressing signals CH1 to CH14, as shown in Fig. 16A. The shift register 36 is supplied with the vertical reference clock CL2 as the shift clock pulse thereof. The input of the shift register 36 is connected to receive the vertical timing signal TV (Fig. 16B) obtained from the vertical position decoder 43 (Fig. 3). The character configuration storing read-only memory 34 is addressed in the horizontal direction by the shift register 35 and is addressed in the vertical direction by the shift register 36. Accordingly, the read-only memory 34 of the embodiment shown in Fig. 14 comprises 64 bits.

Fig. 15A is a view showing an example of such a character configuration. The read-only memory 34 is loaded with the logic one or zero in accordance with the character configuration, as shown in Fig. 15B. The read-only memory 34 is addressed in the horizontal direction by the shift register 35 making one recirculation for each of the horizontal addressing signals CH1 to CH14 and is addressed in the vertical direction by the shift register 36 making one recirculation for each of the vertical addressing signals CV1 to CV6. Accordingly, while one bit of the random-access memory 31 is read, the information stored in all the bits in the read-only memory 34 is sequentially read out. If and when the read output in the bit in the random-access memory 31 is the logic one, the signal associated with the data stored in the read-only memory 34 is provided from the AND gate 37. The signal thus obtained is applied to the video synthesizing circuit 231 and a group of characters each having the configuration shown in Fig. 15A is displayed on the television screen 10 (Fig. 1).

Fig. 17 is a block diagram showing an embodiment adapted for selectively displaying two kinds of character configurations. The Fig. 17 embodiment is structured such that a read-only memory 34A stores a character configuration as shown in Fig. 15A and a read-only memory 34B stores a character configuration shown in Fig. 18A. The read output of the read-only memory 34A is applied to one input of an AND gate 321 and the read output of the read-only memory 34B is applied to one input of an AND gate 323. A timing signal Vn of a relatively long period corresponding to several vertical scans is derived from the vertical timing decoder 205 shown in Fig. 2, for example. The period of the timing signal Vn is selected such that a change of the character configuration on the television screen can be

perceived. The timing signal Vn is applied to another input of the AND gate 321 and, through an inverter 322, to another input of the AND gate 323. The outputs of these AND gates 321 and 323 are applied to one input of an AND gate 37 through an OR gate 324. Accordingly, each time the timing signal Vn obtained from the vertical timing decoder 205 is switched, the read output of either the read-only memory 34a or 34b is applied to the AND gate 37. As a result, the configuration of the character symbol displayed on the screen 10 is changed between the character configuration shown in Fig. 15A and the character configuration shown in Fig. 18A.

Fig. 18B to 18E show modified examples of character configurations. Thus, it would be appreciated that character configurations can be selected as desired according to the present embodiment.

Fig. 19 is a block diagram showing an embodiment adapted for selectively displaying three kinds of character configurations. In the embodiment shown, the vertical addressing signals CV1 to CV6 are utilized for selective display. Thus, the characters of the configuration shown in Fig. 15A are displayed in the first and second rows of the character arrangement, the characters of the configuration shown in Fig. 18A are displayed on the third and fourth rows of the character arrangement, and the characters of the configuration shown in Fig. 18B are displayed on the fifth and sixth rows of the character arrangement. The structure and operation of other portions of the embodiment shown are substantially the same as those of the Fig. 17 embodiment and, therefore, detailed description thereof will be omitted.

Thus, it would be appreciated that the configuration of the character symbols being displayed can be selected as desired. According to the embodiment shown, any particular software processing as required in a conventional system can be dispensed with, by simply utilizing a read-only memory for storing character configurations. Such a read-only memory for storing character configurations may be a simple one of a relatively small number of bits. Thus, by employing such a character symbol signal generating circuit 3 in a television game machine, a variety of games can be played.

Fig. 20 is a block diagram showing a further embodiment of the present invention. The embodiment shown comprises in combination the random-access memory 31 for storing information representing whether or not characters are to be displayed, the read-only memory 32 for storing the arrangement pattern as described in conjunction with Figs. 12 and 13, and the read-only memory 34 for storing the character configurations as described in conjunction with Fig. 14 (and Figs. 17 and 19). The read output of the random-access memory 31 and the read outputs of

the read-only memories 32 and 34 are applied to an AND gate 38 to derive their logical product. The output of the AND gate 38 is obtained as the output signal of the circuit 3 and thus a character symbol signal. Since the operation of the Fig. 20 embodiment could be readily understood by simultaneous consideration of the operations of previously described embodiments, it is not believed necessary to describe the same in more detail. According to the Fig. 20 embodiment, the characters of the configuration as shown in Fig. 15A can be displayed as a character group of an arrangement pattern as shown in Fig. 10A, while the character configuration of the characters can be changed as shown in Figs. 18A to 18E.

CLAIMS

1. An apparatus for displaying a group of characters on a display by repetitive horizontal and vertical scanning of the display, the apparatus comprising:
 - display storage means having storing regions each of which corresponds to a respective one of a number of individual areas of the display and stores information representing whether or not a character is to be displayed in the respective area, the total area occupied by said individual areas corresponding to all said storing regions being less than the total display area,
 - addressing means for sequentially addressing, in association with said horizontal and vertical scanning, said storing regions of said storage means to enable said information to be read out therefrom, said addressing means generating addresses only when said individual areas are being scanned, and
 - converting means responsive to the read-out information for converting information representing that a character is to be displayed into an electrical display signal for displaying said character in the respective area on the display.
2. An apparatus as claimed in claim 1, wherein said characters are displayable in an array having plural rows in the vertical direction and plural columns in the horizontal direction of said display.
3. An apparatus as claimed in claim 1 or claim 2, wherein said storing regions of said storage means are arranged to be addressed by column and row addresses corresponding to respective horizontal and vertical positions on the display, and said addressing means comprises horizontal direction addressing means for providing said column addresses and vertical direction addressing means for providing said row addresses.
4. An apparatus as claimed in claim 3, which further comprises
 - means for generating first reference clocks, and wherein said horizontal direction addressing means comprises
 - horizontal counting means responsive to said first reference clocks for cyclically counting a number of said first reference clocks corresponding to the length in the horizontal direction of said display,
 - horizontal decoding means responsive to the count value in said horizontal counting means for providing column addresses for addressing said storage means, and
 - said vertical direction addressing means comprises
 - means responsive to said horizontal counting means for providing a second reference clock at every predetermined number of said first reference clocks,
 - vertical counting means responsive to said second reference clocks for cyclically counting a number of said second reference clocks corresponding to the length in the vertical direction of said display, and
 - vertical decoding means responsive to the count value in said vertical counting means for providing row addresses for addressing said storage means.
5. An apparatus as claimed in claim 4, wherein said horizontal decoding means is arranged such that the same column address is continually provided during a time period corresponding to the width in the horizontal direction of a displayable character, and said vertical decoding means is arranged such that the same row address is continually provided during a time period corresponding to the width in the vertical direction of the displayable character.
6. An apparatus as claimed in claim 5, wherein said characters are displayable in rows and columns in the horizontal and vertical directions, with a horizontal space between two adjacent characters in the horizontal direction and a vertical space between two adjacent characters in the vertical direction,
 - said horizontal decoding means is arranged such that no column address is provided during a time period corresponding to the width of said horizontal space between two adjacent characters in the horizontal direction, and
 - said vertical decoding means is arranged such that no row address is provided during a time period corresponding to the vertical space between two adjacent characters in the vertical direction.
7. An apparatus as claimed in any one of claims 4 to 6, wherein said horizontal decoding means and vertical decoding means comprise read-only memories responsive to the count values of said horizontal counting means and said vertical counting means respectively for providing said column and row addresses.
8. An apparatus as claimed in any preceding claim, wherein said display storage means comprises a random-access memory, the apparatus further comprises means responsive to said addressing means for loading said information representing whether or not said



the read-only memories 32 and 34 are applied to an AND gate 38 to derive their logical product. The output of the AND gate 38 is obtained as the output signal of the circuit 3 and thus a character symbol signal. Since the operation of the Fig. 20 embodiment could be readily understood by simultaneous consideration of the operations of previously described embodiments, it is not believed necessary to describe the same in more detail. According to the Fig. 20 embodiment, the characters of the configuration as shown in Fig. 15A can be displayed as a character group of an arrangement pattern as shown in Fig. 10A, while the character configuration of the characters can be changed as shown in Figs. 18A to 18E.

CLAIMS

1. An apparatus for displaying a group of characters on a display by repetitive horizontal and vertical scanning of the display, the apparatus comprising:
 - display storage means having storing regions each of which corresponds to a respective one of a number of individual areas of the display and stores information representing whether or not a character is to be displayed in the respective area, the total area occupied by said individual areas corresponding to all said storing regions being less than the total display area,
 - addressing means for sequentially addressing, in association with said horizontal and vertical scanning, said storing regions of said storage means to enable said information to be read out therefrom, said addressing means generating addresses only when said individual areas are being scanned, and
 - converting means responsive to the read-out information for converting information representing that a character is to be displayed into an electrical display signal for displaying said character in the respective area on the display.
2. An apparatus as claimed in claim 1, wherein said characters are displayable in an array having plural rows in the vertical direction and plural columns in the horizontal direction of said display.
3. An apparatus as claimed in claim 1 or claim 2, wherein said storing regions of said storage means are arranged to be addressed by column and row addresses corresponding to respective horizontal and vertical positions on the display, and said addressing means comprises horizontal direction addressing means for providing said column addresses and vertical direction addressing means for providing said row addresses.
4. An apparatus as claimed in claim 3, which further comprises
 - means for generating first reference clocks, and wherein said horizontal direction addressing means comprises
 - horizontal counting means responsive to

said first reference clocks for cyclically counting a number of said first reference clocks corresponding to the length in the horizontal direction of said display,

- horizontal decoding means responsive to the count value in said horizontal counting means for providing column addresses for addressing said storage means, and
- said vertical direction addressing means comprises
 - means responsive to said horizontal counting means for providing a second reference clock at every predetermined number of said first reference clocks,
 - vertical counting means responsive to said second reference clocks for cyclically counting a number of said second reference clocks corresponding to the length in the vertical direction of said display, and
 - vertical decoding means responsive to the count value in said vertical counting means for providing row addresses for addressing said storage means.
5. An apparatus as claimed in claim 4, wherein said horizontal decoding means is arranged such that the same column address is continually provided during a time period corresponding to the width in the horizontal direction of a displayable character, and said vertical decoding means is arranged such that the same row address is continually provided during a time period corresponding to the width in the vertical direction of the displayable character.
6. An apparatus as claimed in claim 5, wherein said characters are displayable in rows and columns in the horizontal and vertical directions, with a horizontal space between two adjacent characters in the horizontal direction and a vertical space between two adjacent characters in the vertical direction,
 - said horizontal decoding means is arranged such that no column address is provided during a time period corresponding to the width of said horizontal space between two adjacent characters in the horizontal direction, and
 - said vertical decoding means is arranged such that no row address is provided during a time period corresponding to the vertical space between two adjacent characters in the vertical direction.
7. An apparatus as claimed in any one of claims 4 to 6, wherein said horizontal decoding means and vertical decoding means comprise read-only memories responsive to the count values of said horizontal counting means and said vertical counting means respectively for providing said column and row addresses.
8. An apparatus as claimed in any preceding claim, wherein said display storage means comprises a random-access memory, the apparatus further comprises means responsive to said addressing means for loading said information representing whether or not said



character is to be displayed in each of said storing regions of said storage means.

9. An apparatus as claimed in any preceding claim, wherein said characters are display-
5 able in a predetermined pattern, the apparatus further comprising second storage means for storing information representative of said pattern.

10. An apparatus as claimed in claim 9,
10 which further comprises
second addressing means for sequentially addressing said second storage means in association with said horizontal and vertical scanning and in synchronism with the ad-
15 dressing of said display storage means, and composing means responsive to said information representing whether or not each said character is to be displayed read from said display storage means and said information
20 representing said pattern of said characters read from said second storage means for composing pattern conditioned information representing whether or not each said character is to be displayed, thereby to display said
25 characters in said pattern.

11. An apparatus as claimed in claim 10, wherein
said second storage means has storing re-
30 gions each corresponding to a respective storing region of said display storage means, and predetermined storing regions of said second storage means, determined by said pattern of the characters, are loaded with information representing that the respective char-
35 acter is to be prevented from being displayed.

12. An apparatus as claimed in claim 10 or 11, wherein said composing means comprises logical product means for deriving a logical product of the information read out of
40 said display storage means and the information read out of said second storage means.

13. An apparatus as claimed in claim 9, wherein said display storage means comprises a random-access memory, and which further
45 comprises writing means responsive to the contents of said second storage means for writing into said display storage means said information representing whether or not a character is to be displayed in each of said
50 storing regions of said display storage means in accordance with said pattern stored in said second storage means.

14. An apparatus as claimed in any one of claims 9 to 13, wherein said second storage means is capable of storing information concerning a plurality of different patterns, and which further comprises selecting means for selecting one of said plurality of patterns.

15. An apparatus as claimed in claim 14,
60 wherein
said second storage means comprises a plurality of areas each for storing a respective pattern, and

said selecting means comprises selective
65 enabling means for selectively enabling one of

said plurality of areas in said second storage means.

16. An apparatus as claimed in claim 14, wherein said second storage means comprises
70 a common area storing information relating to a pattern part which is common to said plurality of patterns, and a plurality of first areas each for storing information representing a part of a respective pattern, said selecting
75 means being operable to selectively enable one of said plurality of first areas.

17. An apparatus as claimed in any preceding claim, which further comprises character configuration storage means for
80 storing information used to determine the configuration of displayed characters.

18. An apparatus as claimed in claim 17, wherein
said character configuration storage means
85 comprises a plurality of bit positions addressable by row addresses and column addresses, the apparatus having bit addressing means for providing said row and column addresses to sequentially address said plurality of bit
90 positions while a storage region of said first storage means is being addressed.

19. An apparatus as claimed in claim 18 when directly or indirectly appendent to claim 3, wherein said bit addressing means com-
95 prises

column addressing means for providing sequential column addresses for said character configuration storage means while said horizontal direction addressing means is providing
100 one column address, and

row addressing means for providing sequential row addresses for said character configuration storage means while said vertical direction addressing means is providing one
105 row address.

20. An apparatus as claimed in claim 19, wherein said column addressing means and row addressing means of said bit addressing means respectively comprise a ring counter
110 making one recirculation during a period when said one column address is provided by said horizontal direction addressing means and a ring counter making one recirculation during a period when said one row address is
115 provided by said vertical direction addressing means.

21. An apparatus as claimed in any one of claims 17 to 20, wherein said character configuration storage means stores a plurality of different character configurations, and which further comprises character configuration selecting means for selecting one of said plurality of character configurations.

22. An apparatus as claimed in claim 21,
125 wherein said character configuration selecting means is operable to select different character configurations for different addresses of said display storage means thereby to display simultaneously characters of different configura-
130 tions.



23. An apparatus as claimed in claim 22, wherein said character configuration selecting means is operable to select one of said plurality of character configurations for a plurality of addresses of said display storage means so that a plurality of displayed characters have a configuration different from that of other displayed characters.

24. An apparatus as claimed in claim 21, 22 or 23, wherein said character configuration selecting means is operable to repetitively select different character configurations so as to cause the configuration of a displayed character to change at a visually perceivable rate.

25. An apparatus as claimed in any one of claims 17 to 24, when directly or indirectly appendent to claim 10, wherein said composing means comprises logical product means for deriving a logical product of the information read out of said display storage means, the information read out of said second storage means and the information read out of said character configuration storage means.

26. An apparatus as claimed in claim 4 or any one of claims 5 to 25 when directly or indirectly appendent to claim 4, including means for changing a preset value applied to said vertical counting means thereby to alter the correspondence between the row addresses applied to said display storage means and the vertical positions on the display and accordingly alter the vertical positions of the displayed characters.

27. An apparatus as claimed in any preceding claim, wherein each said storing region stores only a single bit.

28. A television game machine adapted for displaying on the screen of a television receiver by repetitive horizontal and vertical scanning, a group of characters, a moving symbol moving on said screen and a position controllable symbol, the machine comprising apparatus as claimed in any one of the preceding claims for displaying said group of characters on said screen,

moving symbol signal generating means for generating a moving symbol signal for causing a display of a moving symbol on the screen,

position controllable symbol signal generating means for generating a position controllable symbol signal for causing a display of a position controllable symbol on the screen, and

position controlling means coupled to said position controllable symbol signal generating means for controlling the position of said position controllable symbol displayed on the screen,

said converting means being operable to combine said information read from said display storage means, said moving symbol signal, and said position controllable symbol signal and to convert the combined signal into a

high frequency television display signal.

29. A television game machine as claimed in claim 28, which further comprises resetting means for providing a reset signal, 70 and

picture frame pulse generating means responsive to said reset signal obtained from said resetting means for providing a pulse defining a time period corresponding to the period required for horizontal and vertical scanning of at least one picture frame,

means being provided to write said information representing whether or not said characters are to be displayed into said storing regions of said display storage means as an initial condition during said time period of said picture frame pulse obtained from said picture frame pulse generating means.

30. A television game machine as claimed in claim 29, arranged such that the reading out of said information in said storing regions of said display storage means is initiated upon termination of said picture frame pulse obtained from said picture frame pulse generating means.

31. A television game machine as claimed in any one of claims 28 to 30, which further comprises collision detecting means for detecting collision of said moving symbol and at least one of said characters on the screen, and means responsive to the collision detected output of said collision detecting means for writing information representing that the character is not to be displayed in the storing region of said display storage means corresponding to the character with which said moving symbol collided.

32. A television game machine as claimed in claim 31, wherein said collision detecting means comprises logical product means for deriving the logical product of the information read from said display storage means and the moving symbol signal obtained from said moving symbol signal generating means.

33. A television game machine substantially as herein described with reference to Figs. 1 to 8, optionally modified as described with reference to Figs. 9 to 11 or Fig. 12 or Fig. 13 and/or Figs. 14 to 16 or Figs. 17 and 18 or Fig. 19 or Fig. 20, of the accompanying drawings.