

HIGH VOLTAGE DRIVERS WHICH AVOID $-V_s$ FAILURE MODESABSTRACT OF THE DISCLOSURE

In a level shifted high voltage MOSgate device driver which drives MOSgate devices such as IGBTs and power MOSFETs, effects of negative voltage swings caused by currents commutating through L_{s1} and L_{s2} inductances in the power circuits are avoided due to several measures. First, the values of the inductances L_{s1} and L_{s2} are reduced by keeping short conductor lengths, by other layout/wire bonding techniques to reduce the values of the L_{s1} and L_{s2} inductances. The external, charging capacitor C_s value is increased substantially to reduce the voltage buildup on the internal circuitry. A typical value is $0.47 \mu F$, for a given circuit, IGBT and layout combination. The size of the C_{VCC} capacitor is selected to keep the supply voltage as stiff as possible. Preferably, C_{VCC} is at about ten times the value of the sum of the C_s capacitance in the circuit. The resistance R_s in the bootstrap path is reduced as much as possible, preferably to zero. Finally, a resistor R_{COM} is optionally added between the common nodes of the driver circuit and the power device circuit.

FIGURE 1

