WHAT IS CLAIMED IS:

1. An impedance calibration circuit, comprising:

a calibration module configured to receive a first calibration clock signal, to perform impedance calibration on a basis of the first calibration clock signal, and to output a first stop signal when the calibration is completed;

a first detection module configured to detect calibration time of the impedance calibration circuit, and to output a second stop signal when the calibration time reaches a preset value; and

a calibration control module configured to receive the first stop signal and the second stop signal and to output the first calibration clock signal, wherein when the first stop signal or the second stop signal is received, the calibration control module stops outputting the first calibration clock signal;

wherein the calibration module comprises a first calibration unit, the calibration module being configured to perform impedance calibration on the first calibration unit when the first calibration clock signal is received; and the first calibration unit comprises:

a first resistor unit having a first terminal connected to a first power terminal;

a reference resistor having a first terminal connected to a second terminal of the first resistor unit and a second terminal connected to a second power terminal;

a first comparison unit configured to compare a second terminal voltage of the first resistor unit with a first reference voltage, and to output a first comparison signal; and

a first detection unit configured to determine the first comparison signal as an input signal, to record change of the first comparison signal, and to output the first stop signal when the change of the first comparison signal meets a preset condition.

2. The impedance calibration circuit according to claim 1, wherein the calibration control module comprises a first logic gate circuit, the first logic gate circuit being configured

to receive the first stop signal and the second stop signal, and to perform logic operation processing to output a first control signal, and the calibration control module being configured to stop outputting the first calibration clock signal according to the first control signal.

3. The impedance calibration circuit according to claim 2, wherein the first logic gate circuit comprises an OR gate.

4. The impedance calibration circuit according to claim 1, wherein the first detection unit comprises an odd number of flip-flops cascaded and a second logic gate circuit, first output terminals of the flip-flops of odd-numbered stages being connected to an input terminal of the second logic gate circuit, second output terminals of the flip-flops of even-numbered stages being connected to the input terminal of the second logic gate circuit, and the first stop signal being outputted after logic processing of the second logic gate circuit.

5. The impedance calibration circuit according to claim 1, wherein the first detection unit comprises an odd number of flip-flops cascaded and a second logic gate circuit, second output terminals of the flip-flops of odd-numbered stages being connected to an input terminal of the second logic gate circuit, first output terminals of the flip-flops of even-numbered stages being connected to the input terminal of the second logic gate circuit, and the first stop signal being outputted after logic processing of the second logic gate circuit.

6. The impedance calibration circuit according to claim 1, wherein the first calibration unit further comprises a first calibration code generation unit, the first calibration code generation unit being configured to update a first calibration code according to the first comparison signal, the first calibration code being configured for controlling an equivalent resistance of the first resistor unit.

7. The impedance calibration circuit according to claim 6, wherein the first detection module is configured to detect calibration time of the first calibration unit, and to output the second stop signal when the calibration time of the first calibration unit reaches the preset value.

8. The impedance calibration circuit according to claim 7, wherein the calibration control module is further configured to output a second calibration clock signal, the

calibration module being further configured to receive the second calibration clock signal, and the calibration control module being configured to stop outputting the first calibration clock signal and start to output the second calibration clock signal when the first stop signal or the second stop signal is received.

9. The impedance calibration circuit according to claim 8, wherein the calibration module further comprises a second calibration unit, the calibration module being configured to perform impedance calibration on the second calibration unit when the second calibration clock signal is received, the second calibration unit comprising:

a second resistor unit having a second terminal connected to the second power terminal;

a third resistor unit having a first terminal connected to the first power terminal and a second terminal connected to a first terminal of the second resistor unit, wherein the first calibration code is further configured for controlling an equivalent resistance of the third resistor unit;

a second comparison unit configured to compare a first terminal voltage of the second resistor unit with a second reference voltage, and to output a second comparison signal; and

a second detection unit configured to determine the second comparison signal as an input signal, to record change of the second comparison signal, and to output a third stop signal when the change of the second comparison signal meets a preset condition;

wherein the calibration control module is configured to stop outputting the second calibration clock signal when the third stop signal or the second stop signal is received.

10. The impedance calibration circuit according to claim 9, wherein the first detection module is further configured to detect calibration time of the second calibration unit, and to output the second stop signal when the calibration time of the second calibration unit reaches the preset value.

11. The impedance calibration circuit according to claim 9, wherein the impedance calibration circuit further comprises a clock signal generation module configured to output an initial clock signal, the calibration control module being configured to output the first calibration clock signal and the second calibration clock signal when the initial clock signal is

received; and when the calibration module is configured to perform impedance calibration on the second calibration unit, the calibration control module is configured to output a stop signal to the clock signal generation module when the third stop signal or the second stop signal is received, such that the clock signal generation module stops outputting the initial clock signal.

12. The impedance calibration circuit according to claim 11, wherein the first detection module comprises a counting module; and when the calibration module is configured to perform impedance calibration on the first calibration unit and/or the second calibration unit, the counting module is configured to count the initial clock signal, and to output the second stop signal when a count value reaches a preset value.

13. The impedance calibration circuit according to claim 1, wherein the preset value is less than or equal to forty clock cycles.

14. The impedance calibration circuit according to claim 9, wherein the second calibration unit further comprises a second calibration code generation unit, the second calibration code generation unit being configured to update a second calibration code according to the second comparison signal, the second calibration code being configured for controlling an equivalent resistance of the second resistor unit.