SEMICONDUCTOR DEVICE AND METHOD OF FORMING ENCAPSULATED VERTICAL INTERCONNECT STRUCTURE

Field of the Invention

[0001] The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming an encapsulated vertical interconnect structure.

Background of the Invention

[0002] Semiconductor devices are commonly found in modern electronic products. Semiconductor devices perform a wide range of functions, such as signal processing, high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, photo-electric, and creating visual images for television displays. Semiconductor devices are found in the fields of communications, power conversion, networks, computers, entertainment, and consumer products. Semiconductor devices are also found in military applications, aviation, automotive, industrial controllers, and office equipment.

[0003] A semiconductor wafer typically contains a plurality of semiconductor die separated by a saw street. The semiconductor wafer is singulated into a plurality of individual semiconductor die. A semiconductor package may contain a semiconductor die mounted to an interconnect substrate or structure. The interconnect structure should provide vertical interconnect capability for the semiconductor die, sometimes to a significant height. The stacking of vias to form a high

vertical interconnection can lead to irregular shapes and sizes of the vias, reduce manufacturing yield, high warpage, and increase defects. The vertical interconnect structure can have a limited height to diameter ratio, reducing interconnect density.

Brief Description of the Drawings

[0004] FIGs. 1a-1c illustrate a semiconductor wafer with a plurality of semiconductor die separated by a saw street;

FIGs. 2a-2g illustrate a process of forming an encapsulated vertical interconnect structure;

FIGs. 3a-3d illustrate an alternate process of forming a vertical interconnect structure for encapsulation;

FIGs. 4a-4h illustrate packaging the encapsulated vertical interconnect structure from FIG. 2g with an electrical component;

FIGs. 5a-5e illustrate packaging the encapsulated vertical interconnect structure from FIG. 2f with an electrical component;

FIGs. 6a-6e illustrate a process of forming an encapsulated stacked vertical interconnect structure;

FIGs. 7a-7e illustrate packaging the encapsulated stacked vertical interconnect structure from FIG. 6d with an electrical component; and

FIG. 8 illustrates a printed circuit board (PCB) with different types of packages disposed on a surface of the PCB.

Detailed Description of the Drawings

[0005] The present invention is described in one or more

embodiments in the following description with reference to the figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings. The features shown in the figures are not necessarily drawn to scale. Elements having a similar function are assigned the same reference number in the figures. The term "semiconductor die" as used herein refers to both the singular and plural form of the words, and accordingly, can refer to both a single semiconductor device and multiple semiconductor devices.

[0006] Semiconductor devices are generally manufactured using two complex manufacturing processes: front-end manufacturing and back-end manufacturing. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits. Active electrical components, such as transistors and diodes, have the ability to control the flow of electrical current. Passive electrical components, such as capacitors, inductors, and resistors, create a relationship between voltage and current necessary to perform electrical circuit functions.

[0007] Back-end manufacturing refers to cutting or singulating the finished wafer into the individual semiconductor die and packaging the semiconductor die for structural support, electrical interconnect, and environmental isolation. To

singulate the semiconductor die, the wafer is scored and broken along non-functional regions of the wafer called saw streets or scribes. The wafer is singulated using a laser cutting tool or saw blade. After singulation, the individual semiconductor die are disposed on a package substrate that includes pins or contact pads for interconnection with other system components. Contact pads formed over the semiconductor die are then connected to contact pads within the package. The electrical connections can be made with conductive layers, bumps, stud bumps, conductive paste, or wirebonds. An encapsulant or other molding material is deposited over the package to provide physical support and electrical isolation. The finished package is then inserted into an electrical system and the functionality of the semiconductor device is made available to the other system components.

[0008] FIG. 1a shows a semiconductor wafer 100 with a base substrate material 102, such as silicon, germanium, aluminum phosphide, aluminum arsenide, gallium arsenide, gallium nitride, indium phosphide, silicon carbide, or other bulk material for structural support. A plurality of semiconductor die or electrical components 104 is formed on wafer 100 separated by a non-active, inter-die wafer area or saw street 106. Saw street 106 provides cutting areas to singulate semiconductor wafer 100 into individual semiconductor die 104. In one embodiment, semiconductor wafer 100 has a width or diameter of 100-450 millimeters (mm).

[0009] FIG. 1b shows a cross-sectional view of a portion of semiconductor wafer 100. Each semiconductor die 104 has a back or non-active surface 108 and an active surface 110 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed

within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 110 to implement analog circuits or digital circuits, such as digital signal processor (DSP), application specific integrated circuits (ASIC), memory, or other signal processing circuit. Semiconductor die 104 may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing.

[0010] An electrically conductive layer 112 is formed over active surface 110 using physical vapor deposition (PVD), chemical vapor deposition (CVD), electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 112 can be one or more layers of aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), silver (Ag), or other suitable electrically conductive material. Conductive layer 112 operates as contact pads electrically connected to the circuits on active surface 110.

[0011] In FIG. 1c, semiconductor wafer 100 is singulated through saw street 106 using a saw blade or laser cutting tool 119 into individual semiconductor die 104. The individual semiconductor die 104 can be inspected and electrically tested for identification of known good die or unit (KGD/KGU) post singulation.

[0012] FIGs. 2a-2g illustrate a process of forming an encapsulated vertical interconnect structure. FIG. 2a shows a temporary substrate 120 made with base material 122 as a multi-layer flexible laminate, ceramic, copper clad laminate (CCL), glass, or epoxy molding compound. Base material 122 can contain one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, solder resist, polyimide, BCB, PBO, and other material having similar

insulating and structural properties. Substrate 120 may include one or more laminated layers of polytetrafluoroethylene (PTFE) pre-impregnated (prepreg), FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. Substrate 120 can be silicon, germanium, aluminum phosphide, aluminum arsenide, gallium arsenide, gallium nitride, indium phosphide, silicon carbide, or other bulk material for structural support. In another embodiment, substrate 120 can also be any suitable laminate interposer, PCB, wafer-form, strip interposer, leadframe, or other type of substrate. Substrate 120 has a thickness T of 100 μm or more micrometers (μm) and includes first major surface 124 and second major surface 126 opposite surface 124.

[0013] In FIG. 2b, electrically conductive posts or pillars or columns 130a, 130b, 130c, 130d, and 130e are formed on surface 124. Conductive posts 130a-130e can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. In one embodiment, conductive posts 130a-130e are attached to substrate 120 with conductive paste or solder 132. Bonding material 132 can also be a conductive or non-conductive adhesive thin-film or die attach film (DAF) to form a vertically standing structure of conductive posts 130a to 130e on surface 124 of substrate 120. FIG. 2c shows conductive posts 130a-130e attached to substrate 120 as vertical interconnect structure 136. In one embodiment, conductive posts 130a-130e have a height H1 of about 100 μm and diameter D1 of 50 μm, depending on the desired pitch manufacturing process.

[0014] In another embodiment, and continuing from FIG. 2a, photoresist layer 140 is formed over surface 124 of substrate

120, as shown in FIG. 3a. In FIG. 3b, photoresist layer 140 is patterned and etched to form openings 142. Alternatively, openings 142 can be formed by laser direct ablation (LDA) using laser 144.

[0015] In FIG. 3c, electrically conductive material 146 is deposited into openings 142 by PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive material 146 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material.

[0016] In FIG. 3d, photoresist layer 140 is removed leaving conductive posts or columns or pillars 148a, 148b, 148c, 148d, and 148e formed over surface 124 of substrate 120, as in vertical interconnect structure 150, similar to vertical interconnect structure 136.

[0017] Returning to FIG. 2d, an encapsulant or molding compound 152 is deposited over and around conductive posts 130a-130e and surface 124 of substrate 120 in vertical interconnect structure 136 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 152 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 152 is non-conductive, provides structural support, and environmentally protects the semiconductor device from external elements and contaminants. Although the subsequent process steps are described in terms of vertical interconnect structure 136, a similar encapsulation would apply to vertical interconnect structure 150 if that embodiment is utilized.

[0018] In FIG. 2e, a portion of encapsulant 152 is removed by grinder 156 to planarize surface 158 of encapsulant 152 and

expose surface 154 of conductive pillars 130a-130e. FIG. 2f shows encapsulated vertical interconnect structure 160 post grinding with planarized surface 158 and exposed surface 154 of conductive posts 130a-130e.

[0019] In another embodiment, continuing from FIG. 2d, substrate 120 is removed by chemical mechanical polishing (CMP), mechanical peel-off, mechanical grinding, thermal bake, UV light, or wet stripping, leaving encapsulated vertical interconnect structure 166 with encapsulant 152 covering conductive posts 130a-130e, while planarizing surface 169 of encapsulant 152 and exposing surface 167 of the conductive posts, as shown in FIG. 2g.

[0020] FIG. 4a shows a temporary substrate 170 made with base material 171 as a multi-layer flexible laminate, ceramic, CCL, glass, or epoxy molding compound. Base material 171 can contain one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, solder resist, polyimide, BCB, PBO, and other material having similar insulating and structural properties. Substrate 170 may include one or more laminated layers of PTFE prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. In another embodiment, substrate 120 can also be any suitable laminate interposer, PCB, wafer-form, strip interposer, leadframe, or other type of substrate. Substrate 170 has a thickness T and includes first major surface 172 and second major surface 174 opposite surface 172.

[0021] Encapsulated vertical interconnect structures 166a and 166b from FIG. 2g and electrical component 168 are disposed over surface 172 of substrate 170. For example, electrical component 168 can be similar to, or made similar to, semiconductor die 104

from FIG. 1c with conductive layer 112 oriented toward surface 172. Electrical component 168 can be other semiconductor die, semiconductor packages, surface mount devices, RF components, discrete electrical devices, or integrated passive devices (IPD).

[0022] Encapsulated vertical interconnect structures 166a-166b and electrical component 168 are positioned over substrate 170 using a pick and place operation. Electrical component 168 is disposed between encapsulated vertical interconnect structures 166a-166b, or adjacent to either encapsulated vertical interconnect structure 166a or 166b. Encapsulated vertical interconnect structures 166a-166b and electrical component 168 can be bonded to surface 172 with a bonding layer (not shown). FIG. 4b shows encapsulated vertical interconnect structures 166a-166b and electrical component 168 bonded to substrate 170.

[0023] In FIG. 4c, an encapsulant or molding compound 178 is deposited over and around encapsulated vertical interconnect structures 166a-166b and electrical component 168 and surface 172 of substrate 170 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 178 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 178 is non-conductive, provides structural support, and environmentally protects the semiconductor device from external elements and contaminants.

[0024] In FIG. 4d, a portion of encapsulant 178 is removed by grinder 180 to planarize surface 182 of encapsulant 178 and expose surface 183 of conductive pillars 130a-130e. FIG. 2e shows the encapsulated vertical interconnect structure post

grinding with planarized surface 182 and exposed surface 194 of conductive posts 130a-130e. Surface 182 is planar with a surface of encapsulant 178. Encapsulant 178 may or may not cover back surface 108 of electrical component 168. FIG. 4f is a top view of encapsulated vertical interconnect structures 166a-166b and electrical component 168 bonded to substrate 170.

[0025] In FIG. 4g, substrate 170 is removed by CMP, mechanical peel-off, mechanical grinding, thermal bake, UV light, or wet stripping, leaving semiconductor package 185.

[0026] As an optional feature, a build-up interconnect structure 184 is formed over semiconductor package 185, as in FIG. 4h. Conductive layers 186 and insulating layers 188 are formed within interconnect substrate 184. Conductive layers 186 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layers 186 can be formed using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 186 provides horizontal electrical interconnect across substrate 184 and vertical electrical interconnect through the substrate. Portions of conductive layers 186 can be electrically common or electrically isolated depending on the design and function of electrical component 168. Insulating layers 188 contain one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, solder resist, polyimide, BCB, PBO, and other material having similar insulating and structural properties. Insulating layers 188 can be formed using PVD, CVD, printing, lamination, spin coating, spray coating, sintering or thermal oxidation. Insulating layers 188 provide isolation between conductive layers 186. There can be multiple conductive layers like 186 separated by multiple insulating layers like 188.

[0027] An electrically conductive bump material is deposited over conductive layer 186 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 186 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 189. In one embodiment, bump 189 is formed over an under bump metallization (UBM) having a wetting layer, barrier layer, and adhesive layer. Bump 189 can also be compression bonded or thermocompression bonded to conductive layer 186. Bump 189 represents one type of interconnect structure that can be formed over conductive layer 186. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

[0028] Semiconductor package 185 or 190 represents an encapsulated vertical interconnect structure applicable to wafer level processing (WLP). Conductive posts 130 or 148 provide high post height to diameter ratio. Encapsulated vertical interconnect structures 160 and 166 are pre-formed over substrate 120 prior to mounting to substrate 170. Encapsulated vertical structures 160 and 166 are lamination free so there is little or no risk of delamination. Conductive posts 130 can also be glass or plastic fiber to transmit light in optical applications.

[0029] In another embodiment, FIG. 5a shows encapsulated vertical interconnect structures 160a and 160b from FIG. 2f and electrical component 168 disposed over surface 172 of substrate

170. Components having a similar function are assigned the same reference number. Encapsulated vertical interconnect structures 160a-160b and electrical component 168 are positioned over substrate 170 using a pick and place operation, similar to FIG. 4a-4b. In this case, temporary substrate 120 of encapsulated vertical interconnect structures 160a-160b is oriented away from surface 172. Electrical component 168 is disposed between encapsulated vertical interconnect structures 160a-160b, or adjacent to either encapsulated vertical interconnect structure 160a or 160b. Encapsulated vertical interconnect structures 160a-160b and electrical component 168 can be bonded to surface 172 with a bonding layer.

[0030] In FIG. 5b, an encapsulant or molding compound 192 is deposited over and around encapsulated vertical interconnect structures 160a-160b and electrical component 168 and surface 172 of substrate 170 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 192 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 192 is non-conductive, provides structural support, and environmentally protects the semiconductor device from external elements and contaminants.

[0031] In FIG. 5c, a portion of encapsulant 178 and the entirety of substrate 120 are removed by a grinder, similar to FIG. 4e, to planarize surface 191 of encapsulant 192 and expose surface 193 of conductive pillars 130a-130e. Surface 191 is planar with a surface of encapsulant 192. A top view of encapsulated vertical interconnect structures 160a-160b and electrical component 168 bonded to substrate 170 would be similar to FIG. 4f.

[0032] In FIG. 5d, substrate 170 is removed by CMP, mechanical peel-off, mechanical grinding, thermal bake, UV light, or wet stripping, leaving semiconductor package 195.

[0033] As an optional feature, a build-up interconnect structure 194 is formed over semiconductor package 195, as in FIG. 5e. Conductive layers 196 and insulating layers 198 are formed within interconnect substrate 194. Conductive layers 196 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layers 196 can be formed using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 196 provides horizontal electrical interconnect across substrate 194 and vertical electrical interconnect through the substrate. Portions of conductive layers 196 can be electrically common or electrically isolated depending on the design and function of electrical component 168. Insulating layers 198 contain one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, solder resist, polyimide, BCB, PBO, and other material having similar insulating and structural properties. Insulating layers 198 can be formed using PVD, CVD, printing, lamination, spin coating, spray coating, sintering or thermal oxidation. Insulating layers 198 provide isolation between conductive layers 186. There can be multiple conductive layers like 196 separated by multiple insulating layers like 198.

[0034] An electrically conductive bump material is deposited over conductive layer 196 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb,

high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 196 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 199. In one embodiment, bump 199 is formed over a UBM having a wetting layer, barrier layer, and adhesive layer. Bump 199 can also be compression bonded or thermocompression bonded to conductive layer 196. Bump 199 represents one type of interconnect structure that can be formed over conductive layer 196. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

[0035] Semiconductor package 200 represents an encapsulated vertical interconnect structure applicable to WLP. Conductive posts 130 or 148 provide high post height to diameter ratio. Encapsulated vertical interconnect structures 160 and 166 are pre-formed over substrate 120 prior to mounting to substrate 170. Encapsulated vertical structures 160 and 166 are lamination free so there is little or no risk of delamination. Conductive posts 130 can also be glass or plastic fiber to transmit light in optical applications.

[0036] In another embodiment, the conductive posts like 130a-130e can be stacked. FIG. 6a shows vertical interconnect structure 136 from FIG. 2c, although vertical interconnect structure 150 from FIG. 3d can be used. Vertical interconnect structure 136a is disposed over vertical interconnect structure 136b using a pick and place operation. Conductive posts 130a-130e in vertical interconnect structure 136a are brought into contact with conductive posts 130a-130e in vertical interconnect structure 136b and bonded with conductive paste or solder 202, as vertical interconnect structure 210 in FIG. 6b. In one

embodiment, the stacked conductive posts 211 have a height H2 of 2*H1 and diameter D2 of about the same or larger than D1 to increase the height to diameter aspect ratio suitable for embedded semiconductor die 104 or Si photonic component required a thickness more or equal to 100 μm.

[0037] In FIG. 6c, an encapsulant or molding compound 212 is deposited over and around vertical interconnect structure 210 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 212 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 212 is non-conductive, provides structural support, and environmentally protects the semiconductor device from external elements and contaminants.

[0038] In FIG. 6d, a portion of encapsulant 212 and the entirety of substrate 120 in vertical interconnect structure 136a are removed by grinder 214, similar to FIG. 4e, to planarize surface 218 of encapsulant 192 and expose surface 216 of conductive pillars 130a-130e in vertical interconnect structure 136a. FIG. 6e shows encapsulated vertical interconnect structure 220 post grinding with planarized surface 218 and exposed conductive posts 130a-130e.

[0039] FIG. 7a shows a temporary substrate 230 made with base material 231 as a multi-layer flexible laminate, ceramic, CCL, glass, or epoxy molding compound. Base material 231 can contain one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, solder resist, polyimide, BCB, PBO, and other material having similar insulating and structural properties. Substrate 230 may include one or more laminated layers of PTFE prepreg, FR-4, FR-1, CEM-1,

or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or fabrics. In another embodiment, substrate 230 can also be any suitable laminate interposer, PCB, wafer-form, strip interposer, leadframe, or other type of substrate. Substrate 230 has a thickness T and includes first major surface 232 and second major surface 234 opposite surface 232. Encapsulated vertical interconnect structures 220a-220b from FIG. 6e and electrical component 168 are positioned over substrate 230 using a pick and place operation, similar to FIG. 4a-4b. In this case, the remaining temporary substrate 120 of encapsulated vertical interconnect structures 220a-220b is oriented away from surface 232. Electrical component 168 is disposed between encapsulated vertical interconnect structures 220a-220b, or adjacent to either encapsulated vertical interconnect structure 220a or 220b. Encapsulated interconnect structures 220a-220b and electrical component 168 can be bonded to surface 232 with a bonding layer.

[0040] In FIG. 7b, an encapsulant or molding compound 236 is deposited over and around encapsulated vertical interconnect structures 220a-220b and electrical component 168 and surface 232 of substrate 230 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 236 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 236 is non-conductive, provides structural support, and environmentally protects the semiconductor device from external elements and contaminants.

[0041] In FIG. 7c, a portion of encapsulant 236 and the entirety of substrate 120 of vertical interconnect structure

136a are removed by a grinder, similar to FIG. 4e, to planarize surface 238 of encapsulant 236 and expose surface 239 of conductive pillars 130a-130e. Surface 238 is planar with a surface of encapsulant 236. A top view of encapsulated vertical interconnect structures 220a-220b and electrical component 168 bonded to substrate 230 would be similar to FIG. 4f.

[0042] In FIG. 7d, substrate 230 is removed by CMP, mechanical peel-off, mechanical grinding, thermal bake, UV light, or wet stripping, leaving semiconductor package 241.

[0043] As an optional feature, a build-up interconnect structure 240 is formed over semiconductor package 241, as in FIG. 7e. Conductive layers 242 and insulating layers 244 are formed within interconnect substrate 240. Conductive layers 242 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layers 242 can be formed using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 242 provides horizontal electrical interconnect across substrate 240 and vertical electrical interconnect through the substrate. Portions of conductive layers 242 can be electrically common or electrically isolated depending on the design and function of electrical component 168. Insulating layers 244 contain one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, solder resist, polyimide, BCB, PBO, and other material having similar insulating and structural properties. Insulating layers 244 can be formed using PVD, CVD, printing, lamination, spin coating, spray coating, sintering or thermal oxidation. Insulating layers 244 provide isolation between conductive layers 242. There can be multiple conductive layers like 242 separated by multiple insulating layers like 244.

[0044] An electrically conductive bump material is deposited over conductive layer 242 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 242 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 248. In one embodiment, bump 248 is formed over a UBM having a wetting layer, barrier layer, and adhesive layer. Bump 248 can also be compression bonded or thermocompression bonded to conductive layer 242. Bump 248 represents one type of interconnect structure that can be formed over conductive layer 242. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

[0045] Semiconductor package 241 or 250 represents an encapsulated vertical interconnect structure applicable to WLP. Conductive posts 211 provide a higher post height to diameter ratio by nature of being stacked. Encapsulated vertical interconnect structures 160 and 166 are pre-formed over substrate 120 prior to mounting to substrate 170. Encapsulated vertical structures 160 and 166 are lamination free so there is little or no risk of delamination. Conductive posts 211 can also be glass or plastic fiber to transmit light in optical applications.

[0046] FIG. 8 illustrates electrical device 400 having a chip carrier substrate or PCB 402 with a plurality of semiconductor packages disposed on a surface of PCB 402, including

semiconductor packages 185, 190, 195, 200, 241, and 250. Electrical device 400 can have one type of semiconductor package, or multiple types of semiconductor packages, depending on the application.

[0047] Electrical device 400 can be a stand-alone system that uses the semiconductor packages to perform one or more electrical functions. Alternatively, electrical device 400 can be a subcomponent of a larger system. For example, electrical device 400 can be part of a tablet, cellular phone, digital camera, communication system, or other electrical device. Alternatively, electrical device 400 can be a graphics card, network interface card, or other signal processing card that can be inserted into a computer. The semiconductor package can include microprocessors, memories, ASIC, logic circuits, analog circuits, RF circuits, discrete devices, or other semiconductor die or electrical components. Miniaturization and weight reduction are essential for the products to be accepted by the market. The distance between semiconductor devices may be decreased to achieve higher density.

[0048] In FIG. 8, PCB 402 provides a general substrate for structural support and electrical interconnect of the semiconductor packages disposed on the PCB. Conductive signal traces 404 are formed over a surface or within layers of PCB 402 using evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. Signal traces 404 provide for electrical communication between each of the semiconductor packages, mounted components, and other external system components. Traces 404 also provide power and ground connections to each of the semiconductor packages.

[0049] In some embodiments, a semiconductor device has two packaging levels. First level packaging is a technique for

mechanically and electrically attaching the semiconductor die to an intermediate substrate. Second level packaging involves mechanically and electrically attaching the intermediate substrate to the PCB. In other embodiments, a semiconductor device may only have the first level packaging where the die is mechanically and electrically disposed directly on the PCB. For the purpose of illustration, several types of first level packaging, including bond wire package 406 and flipchip 408, are shown on PCB 402. Additionally, several types of second level packaging, including ball grid array (BGA) 410, bump chip carrier (BCC) 412, land grid array (LGA) 416, multi-chip module (MCM) or SIP module 418, quad flat non-leaded package (QFN) 420, quad flat package 422, embedded wafer level ball grid array (eWLB) 424, and wafer level chip scale package (WLCSP) 426 are shown disposed on PCB 402. In one embodiment, eWLB 424 is a fan-out wafer level package (Fo-WLP) and WLCSP 426 is a fan-in wafer level package (Fi-WLP). Depending upon the system requirements, any combination of semiconductor packages, configured with any combination of first and second level packaging styles, as well as other electrical components, can be connected to PCB 402. In some embodiments, electrical device 400 includes a single attached semiconductor package, while other embodiments call for multiple interconnected packages. By combining one or more semiconductor packages over a single substrate, manufacturers can incorporate pre-made components into electrical devices and systems. Because the semiconductor packages include sophisticated functionality, electrical devices can be manufactured using less expensive components and a streamlined manufacturing process. The resulting devices are less likely to fail and less expensive to manufacture resulting in a lower cost for consumers.

[0050] While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

forming a first vertical interconnect substrate;

forming a second vertical interconnect substrate;

depositing a first encapsulant over the first vertical interconnect structure and second vertical interconnect structure; and

disposing an electrical component between the first vertical interconnect structure and second vertical interconnect structure.

2. The method of claim 1, further including depositing a second encapsulant around the electrical component.

3. The method of claim 2, further including removing a portion of the second encapsulant to expose a surface of the first vertical interconnect structure.

4. The method of claim 1, further including forming the first vertical interconnect structure over a substrate.

5. The method of claim 4, further including removing the substrate to expose a surface of the first vertical interconnect structure.

6. A method of making a semiconductor device, comprising:

forming a vertical interconnect substrate;

depositing a first encapsulant over the vertical interconnect structure; and

disposing an electrical component adjacent to the vertical interconnect structure.

7. The method of claim 6, further including depositing a second encapsulant around the electrical component.

8. The method of claim 7, further including removing a portion of the second encapsulant to expose a surface of the vertical interconnect structure.

9. The method of claim 6, further including forming the vertical interconnect structure over a substrate.

10. The method of claim 9, further including removing the substrate to expose a surface of the vertical interconnect structure.

11. A semiconductor device, comprising:

a first vertical interconnect substrate;

a second vertical interconnect substrate;

a first encapsulant deposited over the first vertical interconnect structure and second vertical interconnect structure; and

an electrical component disposed between the first vertical interconnect structure and second vertical interconnect structure.

12. The semiconductor device of claim 11, further including a second encapsulant deposited around the electrical component.

13. The semiconductor device of claim 12, wherein a surface of the first vertical interconnect structure is planar with a surface of the second encapsulant.

14. The semiconductor device of claim 11, wherein the first vertical interconnect structure includes a plurality of stacked vertical conductive posts.

15. The semiconductor device of claim 11, further including a substrate, wherein the first vertical interconnect structure is formed over the substrate.