

High-frequency differential amplifier stage and amplifier comprising such a differential amplifier stage.

The invention relates to a high-frequency differential amplifier stage comprising a first transistor and a second transistor whose emitters, which are coupled to each other, are connected to a first current source, whose bases are connected to input terminals for receiving input signals, and whose collectors are connected to the emitters of a third and a fourth transistor respectively, which third and fourth transistors have their collectors connected to power-supply terminals for connection to a supply-voltage source via a first and a second bias resistor respectively, the bases of the third transistor and the fourth transistor being connected to the collectors of the fourth and the third transistor respectively. The invention also relates to a multi-stage amplifier comprising such a differential amplifier stage.

Such a differential stage is described in the Applicant's Patent Application no. 86 200 756.4

(publication number 0,201,964), filed on May 2nd, 1986.

The amplifier stage forms the input stage of an amplifier which further comprises an output stage cascaded with the input stage. Further, the amplifier has a gain which can be made higher than 1 for a maximum operating frequency of the amplifier, for example 1 GHz, which closely approximates to the intrinsic cut-off frequency of the transistors used, whilst it has a high gain for frequencies situated in the central part of its operating frequency range.

The input stage is a tuned amplifier, which is capable of amplifying small signals and which has a substantial gain at frequencies situated in the central part of its operating frequency range and which has a

slightly higher maximum gain at frequencies situated in the upper part of its operating frequency range.

It is the object of the present invention to improve the operation of the input stage, enabling signals
5 of a substantial level to be handled without any problems.

The Applicant has found that in the saturated mode this input stage exhibits charge-storage effects in a specific part of the frequency band. As will be explained in the description, a result of these cross-
10 storage effects is that in response to a sinusoidal input signal of a high level an output signal is produced which exhibits a saturation plateau below the nominal saturation level to be expected normally, the level of this plateau decreasing as the level of the input signal
15 increases.

The present invention enables the saturation level to be raised, thus allowing the input stage to handle signals of a higher level before reaching a saturated mode, and the operation in the saturated mode
20 to be regulated. The basic idea of this improvement is to modify the operation of the third transistor and the fourth transistor in the current operating mode.

According to the invention the differential amplifier stage is characterized in that it comprises a
25 second current source connected to the junction point between the collector of the second transistor and the emitter of the fourth transistor, and a third current source connected to the junction point between the collector of the first transistor and the emitter of the
30 third transistor, the currents of the third current source and the fourth current source being directed in such a way that they tend to raise the emitter currents of the fourth transistor and the third transistor respectively, and the sum of their currents being smaller than the
35 current of the first current source.

If the currents meet this requirement the stage will not function as an oscillator.

The ratio between the sum of the currents of the second current source and the third current source and the current of the first current source is suitably of the order of 0.2.

6 The invention, in accordance with a preferred embodiment, also relates to a high-frequency amplifier comprising a plurality of cascaded differential stages, which is characterized in that said stages comprise an input stage in accordance with the invention, coupled
10 directly to a subsequent stage, and in that the product of the current of the second current source or the third current source and the resistance of the first bias resistor or the second bias resistor is smaller than the linear input range of the subsequent stage so as to
15 prevent the latter stage from oscillating.

The subsequent stage may be of the logic type, for example a current-switching stage, known per se, or a linear stage, for example the output stage in conformity with said European Patent Application 86 200 756.4
20 (publication number 0,201,964).

If the subsequent stage is the above-mentioned output stage the collectors of the fifth transistor and the sixth transistor may each be connected to the base of an output transistor arranged as an emitter-follower.

25 In order to limit the gain for d.c. components of the input signals, the amplifier may comprise a second resistive divider bridge which is arranged between the collector of the fifth transistor and earth and whose centre point, which is decoupled by means of a second
30 capacitor, is connected to the base of the first transistor by a first input resistor, and a third resistive divider bridge which is arranged between the collector of the sixth transistor and earth and whose centre point, which is decoupled by means of a third capacitor, is connected
35 to the base of the second transistor via a second input resistor.

Finally, it is to be noted that the output stage may operate in the saturated mode and thus produce clipped

output signals in response to sinusoidal input signals, as a result of which it can perform a shaping function which renders the amplifier in accordance with the invention very suitable for use as an input amplifier for
5 a frequency prescaler, which receives the output signals from the local oscillator of a television receiver, which output signals have a level which may vary between some millivolts and some hundreds of millivolts.

Finally, in accordance with a second embodiment,
10 the invention relates to a high-frequency amplifier comprising a plurality of cascaded differential stages, which is characterized in that said stages comprise an input stage in accordance with the invention, coupled to an emitter-coupled stage comprising a seventh transistor
15 and an eight transistor whose bases receive the output signals of the input stage, and in that the input stage and the emitter-coupled stage are coupled by a first base resistor and a second base resistor which are arranged in series in the base of the seventh transistor and the
20 eight transistor respectively and whose resistance values lie between 1 and 2 times and preferably substantially 1.2 times the value of the intrinsic base resistance of said seventh transistor and eight transistor, so as to prevent the emitter-coupled stage from oscillating.

25 The invention will be more fully understood upon reading the following description, given by way of example, with reference to the Figures, in which

- Fig. 1 is a circuit diagram of the amplifier in accordance with the afore-mentioned Patent Application;

30 - Fig. 2 shows the response curves of each of the two stages of said amplifier in the operating-frequency band of the amplifier;

- Fig. 3 is an equivalent diagram of the loop which limits the gain for the d.c. component of the
35 signal,

- Fig. 4 is an equivalent diagram for the input impedance of the output stage.

- Fig. 5 shows the response curve of said amplifier.

- Fig. 6 shows the waveforms of the signals at the output of the first stage of said amplifier for a positive half-cycle in the saturated mode for input signals of different values,

- Fig. 7 shows the first stage of said amplifier, modified in accordance with the invention.

The input stage of the amplifier in Fig. 1 comprises a differential stage with two transistors T_1 and T_2 whose emitters are coupled and are connected to a current source comprising a transistor T_5 whose emitter is connected to earth via a resistor R_3 , the base of the transistor T_5 receiving a control voltage U which determines the current $2I_1$ supplied by the current source.

The inputs E_1 and E_2 of the amplifier are formed by the bases of the transistors T_1 and T_2 respectively. Two transistors T_3 and T_4 constituting the resonant circuit of the input stage have their emitters connected to the collectors of the transistors T_1 and T_2 respectively, the base of the transistor T_3 being connected to the collector of the transistor T_4 and vice versa. The collectors of the transistors T_3 and T_4 are connected to a supply voltage source via bias resistors R_1 and R_2 respectively of the same value. This voltage source is represented as a power supply $+V$ whose potential is reduced by one emitter-base voltage (approximately 0.8 V) by means of a diode-connected transistor T_{14} which for this purpose has its collector and base connected to the power supply $+V$ and its emitter to the junction point between the resistors R_1 and R_2 .

The output stage comprises a differential stage with two transistors T_6 and T_7 whose emitters are interconnected by a capacitor C_1 in parallel with a resistive bridge (R_8 , R_9) whose centre point is connected to a current source comprising a transistor T_8 whose emitter

is connected to earth by a resistor R_{10} , the base of the transistor T_8 receiving the control voltage U which determines the current $2I_2$ supplied by the current source. The resistors R_8 and R_9 and the capacitor C_1 constitute
5 a phase-lead circuit which enables the gain of the output stage in the upper part of the operating-frequency range to be improved.

The output signals of the input stage are applied from the collectors of the transistors T_1 and T_2 to the
10 bases of the transistors T_6 and T_7 respectively. The collectors of the transistors T_6 and T_7 are connected to a supply-voltage source via resistors R_6 and R_7 respectively. This voltage source comprises a power supply V whose voltage is reduced by means of a resistor
15 R_5 arranged in series between the power supply V and the junction point between the resistors R_6 and R_7 , and in which therefore always the current $2I_2$ flows.

The outputs of the output stage are formed by the collectors of the transistors T_6 and T_7 and can
20 be used directly. The transistors T_9 and T_{10} are shown as emitter-follower arrangements, their collectors being connected to the power supply V , their bases to the collectors of the transistors T_6 and T_7 respectively, and their emitters to diode-connected transistors T_{11}
25 and T_{12} poled in the forward direction, which results in total shift by two base-emitter voltages (approximately 1.6 V). For this purpose, the collectors of the transistors T_{11} and T_{12} are short-circuited to their bases and are connected to the emitters of the transistors T_9 and T_{10}
30 respectively. The emitters of the transistors T_{11} and T_{12} , which are connected to earth via resistors R_{25} and R_{26} respectively, constitute the outputs S_1 and S_2 of the amplifier.

Fig. 2 shows the response curves of the input
35 stage, when coupled to the output stage, and of the output stage in the operating-frequency band of the amplifier, between a minimum frequency F_m and a maximum frequency F_M .

The response curve of the input stage 1, when coupled to the output stage, exhibits a substantially constant gain G_1 in the lower part of the frequency range of the amplifier. Under the influence of the resonant circuit, the gain increases distinctly from a frequency F_1 up to an anti-resonant frequency F'_1 corresponding to a maximum gain above which the gain again decreases to approximate to an asymptote 10 with a slope of -12dB/octave, the gain remaining higher than or equal to 1 (0 dB) at the maximum frequency F_M .

In the lower part of the frequency range of the amplifier the response curve of the output stage 2 exhibits a substantially constant gain G_2 which may be close to G_1 . Under the influence of the phase-lead circuit the gain becomes slightly higher starting from a frequency F_0 up to a frequency F'_0 , above which the gain again decreases to approximate to an asymptote 20 with a slope of -6 dB/octave, the gain remaining higher than or equal to 1 (0 dB) at the selected maximum frequency F_M .

In the lower part of the operating frequency range of the amplifier, the two stages have substantially equal gain factors ($G_1 \sim G_2$) up to a frequency F_1 , above which the input stage has a higher gain as a result of the presence of said resonant circuit (hatched area). As the asymptote 10 of the curve 1 has a stronger slope than the asymptote 20 of the curve 2 there is a cross-over frequency which may be lower or, preferably, higher than F_M .

Hereinafter it will be explained how the circuit parameters are suitably selected in order to obtain the above response curves. This is illustrated by means of an example where $F_m = 40$ MHz and $F_M = 1$ GHz, which corresponds to an input amplifier intended for a frequency divider which can be used in a television receiver operating in this frequency band.

According to the Applicant the response curve

$G_1(s)$ of the input stage alone, i.e. when not coupled to the output stage, may be represented in a first approximation by the following formula:

$$5 \quad G_1(s) = \frac{G_1(1-sT_1)}{(1+sT_2)(1+sT_3)}$$

where

$$10 \quad G_1 = \frac{R_1 I_1}{V_T}$$

$$T_1 = C_{BC} [4R_1 + R_b (1 + G_1)] = \frac{1}{2\pi F_1}$$

$$T_2 = C_{BC} (R_b + 4R_1) = \frac{1}{2\pi F_2}$$

$$15 \quad T_3 = K C_{BE} \frac{V_T}{I_1} = \frac{1}{2\pi F_3} \quad \text{where } K \cong 4 \text{ and } V_T = 26 \text{ mV.}$$

C_{BC} and C_{BE} are the base-collector and the base-emitter capacitances of the transistors T_3 and T_4 respectively.

20 The relationship $T_1 > T_2$ is always valid. The relationship $T_2 > T_3$ is also always valid because $C_{BE} \cong 2C_{BC}$ for the integrated-circuit transistors used and the term $\frac{V_T}{I_1}$ is small ($I_1 \cong 1\text{mA}$) relative to $R_b + 4R_1$,

25 so that:

$$F_1 < F_2 < F_3.$$

The curve 1 in Fig. 2 is therefore characteristic of the circuit arrangement of the input stage.

For more information about the design of
30 transistors for use at very high frequencies reference may be made to the publication by P.R. GRAY and R.G. MEYER "Analysis and Design of Analog Integrated Circuits" (published by John Wiley and sons USA-1977).

In the case of a transistor having an intrinsic
35 cut-off frequency f_T of the order of 5 GHz, when $R_1 = 100\Omega$ and $I_1 = 1 \text{ mA}$ and consequently $G_1 \cong 4$, this yields the following values:

$F_1 \approx 300 \text{ MHz}$, $F_2 \approx 540 \text{ MHz}$, $F_3 \approx 900 \text{ MHz}$.

It is to be noted that the choice of high value for G_1 results in the value F_3 being reduced. Optimum results are obtained by adjusting the various parameters so as to ensure that F_M is as high as possible (once the two stages are coupled).

The input stage may be used separately, but in the situation described here it is coupled to an output stage. The values of T_1 , T_2 and T_3 are then modified slightly and the curve $G(s)$ tends to approximate to an asymptote having a slope of -12 dB/octave for frequencies higher than F_3 . In the above example the frequency F_M for which the input stage has a gain of 1 is distinctly higher than 1 GHz.

In the central and the lower part of the operating-frequency range the feedback of the transistors T_3 and T_4 has no effect and the gain has the value G_1 , which can be calculated in the same way as for a conventional differential stage.

$$G_1 = \frac{R_1 I_1}{V_T}$$

The impedance of the second stage as seen from the output of the first stage is shown diagrammatically in Fig. 4. It comprises the intrinsic base resistance $R\lambda_6$ of the transistor T_6 in series with a part of the base-emitter resistance R_{BE6} of T_6 and the resistor R_8 , the base-emitter capacitance C_{BE6} of T_6 across R_{BE6} and a capacitor of the value $2C_1$ across R_4 .

The response curve $G'(s)$ of the second stage may be expressed by the formula:

$$G'(s) = \frac{G_2(1 + sT_0)}{(1 + sT_4)(1 + sT_5)} \quad \text{where } T_0 = 2 R_8 C_1$$

so that

$$F_0 = \frac{1}{4 \pi R_8 C_1}$$

and with $R_6 = R_7$

$$G_2 = \frac{R_6 I_c}{V_T + R_8 I_2} \approx \frac{R_6}{R_8}$$

5 For example, when $C_1 = 2.5$ pF, $R_6 = 360 \Omega$ and $R_8 = 80 \Omega$, this results in $G_2 = 4.5$ and $F'_0 \approx 400$ MHz.

However, it is to be noted that the amplifier can be optimised only when the two stages are adjusted when they are coupled to each other, the output stage in its turn being preferably connected to the circuit to be driven. Indeed, as stated in the foregoing, the input impedance of this output stage considerably influences the high-frequency characteristics of the input stage.

15 A good approach to the overall adjustment of the amplifier is to determine first of all the parameters of the inputs tage alone, as indicated above, to select the desired gain G_2 of the output stage by determining a ratio $\frac{R_7}{R_9} = \frac{R_6}{R_8}$, to select the frequency F_0 near the
20 frequency F_1 of the input stage, and to vary the values of $R_8 = R_9$ and of C_1 , whilst maintaining the ratio $\frac{R_7}{R_8} = \frac{R_6}{R_9}$ and the product $R_8 C_1$ constant until a maximum
25 frequency is obtained which corresponds to a gain of 1 (0 dB), which means that the two stages are correctly matched to one another.

In an advantageous embodiment the amplifier comprises a circuit which introduces a coupling between its output and its input in order to limit the d.c. gain.

30 To this end the collector of the transistor T_6 is connected to earth via a first divider bridge comprising two resistors R_{11} and R_{12} , a capacitor C_2 being connected across the resistor R_{12} , between the tapping point of the divider bridge and earth. The centre
35 point of the divider bridge is connected to the base of the transistor T_1 via an input resistor R_{14} . Similarly, the collector of the transistor T_7 is connected to earth

via a second divider bridge comprising two resistors R_{21} and R_{22} , a capacitor C_3 being connected across the resistor R_{22} , between the centre point of the second divider bridge and earth. The centre point of the second divider bridge is connected to the base of the transistor T_2 by an input resistor R_{24} . R_{12} , R_{13} , C_2 and C_3 are selected in such a way that in the operating-frequency band of the amplifier $C_2 = C_3$ constitute a short-circuit, which at these frequencies has the same effect as arranging R_{14} and R_{24} between the base of T_3 and T_4 respectively and earth. Consequently, R_{14} and R_{24} determine the input impedance of the input stage. For example, $R_{14} = R_{24} = 500 \Omega$. Below a frequency

$$F_m = \frac{1}{2\pi R_{12} C_2} = \frac{1}{2\pi R_{22} C_3}$$

the gain of the amplifier decreases to a value G_0 (see Fig. 3) equal to $1 + \frac{R_{11}}{R_{12}} = 1 + \frac{R_{21}}{R_{22}}$,

which is the value of the gain obtained for the d.c. component of the signal. For a gain lower than 2 it is necessary that $R_{11} < R_{12}$. Indeed, for direct current the capacitors C_2 and C_3 are charged via the resistors R_{14} and R_{24} respectively. Both terminals of R_{14} are at a potential e_1 and those of R_{24} at a potential e_2 . As a result of this, the equivalent diagram is as shown in Fig. 3, which represents an amplifier A having two inputs e_1 and e_2 and two outputs s_1 and s_2 , the resistor R_{12} being arranged between e_1 and earth, the resistor R_{22} between e_2 and earth, the resistor R_{11} between s and e_1 , and the resistor R_{21} between s and e_2 .

The value of the above-mentioned gain follows from the requirement that the currents in each of the branches should be balanced.

For example, for $R_{11} = R_{21} = 5.4 \text{ k}\Omega$, $R_{12} = R_{22} = 7.4 \text{ k}\Omega$, $C_2 = C_3 = 1 \text{ pF}$, this yields $F_m \approx 42 \text{ MHz}$ and $G_0 = 1.73$ for an overall gain $G = G_1 G_2 \approx 18$ of the

amplifier when the same values as in the above examples are used.

A signal-shaping function can be obtained by means of the output stage by clipping of sinusoidal signals (operation in the saturated mode). For this purpose, the supply voltage of the output stage should be selected, for example, by choosing the value of the resistor R_5 in such a way that, if the gain G is obtained, clipping is effected for input signals E_1 , E_2 of the lowest level envisaged under normal operating conditions of the amplifier.

As is shown in Fig. 6, when the level ($E_1 - E_2$) of the sinusoidal input signals reaches the value e_0 (for example 70 mV), the output signal ($s_1 - s_2$) of the input stage reaches but does not exceed the nominal saturation level s_0 of the stage.

This means that $s_0 = 2I_1 R_1$.

For input signals having a level $e' > e$, (for example $e' = 100$ mV) there is a saturation plateau of a level $s' < s_0$ and there is also a dip in output level at 11 before the curve returns to the saturation level s_0 at 15.

For input signals of a level $e'' > e'$ (for example, $e'' = 150$ mV), the level of the saturation plateau is $s'' < s'$ and the dip in the level (at 12) is even more pronounced and may even reach the 0 V level, thus causing spurious signal transients which are very annoying for use in frequency dividers.

This effect occurs only in a part of the pass-band of the input stage, namely at frequencies below but close to the resonant frequency of the resonant circuit (R_1 , R_2 , T_3 , T_4).

It is to be noted that the effects occurring at very high frequencies are very complex and cannot be explained by means of approximations. According to the Applicant these effects may be interpreted as follows. At frequencies below its resonant frequency the resonant circuit in principle behaves as an inductance.

For weak signals the transistors T_3 and T_4 are not switched completely and the behaviour of the load remains linear. However, when the amplifier operates in the saturated mode, the resonant circuit behaves as a flip-flop. Charges are then temporarily stored in the collector-base capacitance of the transistors T_1 and T_2 and the base-emitter capacitance of the transistors T_3 and T_4 . The saturation plateau (having a level s' or s'' in Fig. 6) is caused by the discharge of the base-emitter capacitance of the transistor T_3 or the transistor T_4 depending on the half-cycle of the sinusoidal input signal. The dip in level (at 11 or at 12 in Fig. 6) is in itself caused by discharging of the collector-base capacitance of the transistor T_1 or the transistor T_2 depending on the half-cycle of the sinusoidal input signal.

This charge-storage effect in the collector-base capacitance of the transistors T_1 and T_2 and the emitter-base capacitance of the transistors T_3 and T_4 can be mitigated by ensuring that the transistors T_3 and T_4 are not driven into full conduction by impressing an emitter current upon them.

This can be achieved by means of the circuit shown in Fig. 7. In this circuit, the input stage comprises the same elements R_1 , R_2 , R_3 , T_1 , T_2 , T_3 , T_4 , T_5 and T_{14} as in Fig. 1. The outputs s_1 and s_2 formed by the collectors of the transistors T_2 and T_1 respectively are connected to the bases of the transistors T_7 and T_6 respectively.

Moreover, in accordance with the invention, the circuit of Fig. 7 comprises two current sources, suitably supplying the same current I . To this end a transistor T_{31} , whose base receives the voltage U , has its collector connected to the output s_2 , which is the junction point between the collector of the transistor T_1 and the emitter of the transistor T_3 , and has a resistor R_{31} arranged between its emitter and earth. A transistor T_{32} , whose base receives the voltage U , has its collector connected to the output s_1 , which is

the junction point between the collector of the transistor T_2 and the emitter of the transistor T_4 , and has a resistor R_{32} , preferably having the same resistance value as R_{31} , arranged between its emitter and earth.

5 The current I_0 can be very small, but it will be appreciated that in this case a really significant result can be obtained only if this current is at least equal to the dynamic base current of the transistors T_6 and T_7 of the second stage.

10 This dynamic base current has the value I_2/β , β being the current gain (approximately 50) of the transistors T_6 and T_7 .

For example, for $I_2 = 1.5$ mA, this means that $I_0 > 30$ μ A.

15 It is evident that the compensation for the charge-storage effects becomes more effective as the value of I_2 increases. It is to be noted also that for the operation of the stage in the normal saturated mode the currents I_0 supplied by the two current sources contribute to the current $2I_1$ for the operation of the transistors T_3 and T_4 . It follows that the saturation level s_2 is raised and has a value:

$$s_{10} = 2(I_1 + I_0)R_1$$

The optimum value of I_0 is estimated to be $0.2 I_1$.

25 For $I_1 = 1$ mA and $I_0 = 0.2$ mA this yields $s_0 = 200$ mV and $s_{10} = 240$ mV.

Suitably, care is taken that $I_0 < I_1$ in order to prevent the stage from oscillating due to an excessive current I_0 being switched. The high-frequency differential stage in accordance with the invention may be used as such or as an input stage for an amplifier comprising a plurality of cascaded differential stages.

30 Such an amplifier can be realised with a direct coupling between the output of the stage in accordance with the invention and the input of a subsequent stage, which is also of the differential type. The subsequent stage may be of the logic type, for example a current-switching logic circuit, or a

linear circuit, for example the output stage shown in Fig. 1. In either case, and as indicated above, I_0 is suitably selected to be at least equal to the dynamic input current of the subsequent stage, i.e. in the present case the dynamic base current of the transistors of the subsequent stage, and smaller than I_1 .

An additional requirement is that the subsequent stage should not oscillate. For this purpose the relationship $R_1 I_0 = R_2 I_0 < \Delta V$ must be satisfied, ΔV being the linear peak-to-peak range at the input of the subsequent stage (see Fig. 9).

When the subsequent stage is the output stage of Fig. 1, this means that:

$$\Delta V = 2V_t + R_8 I_2 \text{ where } V_t = 26 \text{ mV.}$$

If, more in particular, the situation is considered where the amplifier is used as an input amplifier for a frequency prescaler in a television receiver, the output stage, which is of the phase-lead type is also used, as stated above, for the purpose of signal shaping by clipping.

For weak or average signals the input stage operates in the linear mode and clipping is effected by the output stage only, which is to be preferred. For signals of a high level, the input stage clips the signals. The influence of the current I_0 on the rise of the clipping level s_0 is advantageous because it enables the input stage to handle higher levels without clipping.

In Fig. 8 the stage in accordance with the invention described above can drive a differential stage comprising two transistors whose emitters are coupled directly. The collectors of these transistors may be connected to a power supply $+V$ by resistors R_{36} and R_{37} . The coupled emitters of the transistors T_{36} and T_{37} are connected to a current source and for this purpose they are connected to the collector of a transistor T_{38} whose base receives the voltage U and whose emitter

is connected to earth via a resistor R_{38} . In this arrangement, the stage can be prevented from oscillating by arranging coupling resistors R_{41} and R_{42} in series between the collectors of the transistors T_2 and T_1 and the bases of the transistors T_{36} and T_{37} respectively. These coupling resistors, which are preferably of the same value, have a resistance higher than the intrinsic base resistance of the transistors T_{36} and T_{37} but smaller than twice this value and preferably substantially equal to 1.2 times this value. The function of the resistors R_{41} and R_{42} is illustrated in Fig. 9.

Under static conditions the differential stage has a linear peak-to-peak input range ΔV . The resistors R_{41} and R_{42} enable this linear range to be extended to $\Delta V'$ under dynamic conditions, as is indicated in broken lines.

A really significant extension of this linear range can be obtained only if R_{41} and R_{42} have values higher than the intrinsic base resistance of the transistors T_{36} and T_{37} . However, if the values of the resistors R_{41} and R_{42} becomes too high and exceed twice the intrinsic base resistance, the speed of the stage shown in Fig. 8 will be reduced substantially.

CLAIMS:

1. A high-frequency differential amplifier stage comprising a first transistor and a second transistor whose emitters, which are coupled to each other, are connected to a first current source, whose bases are connected to input terminals for receiving input signals, and whose collectors are connected to the emitters of a third and a fourth transistor respectively, which third and fourth transistors have their collectors connected to power-supply terminals for connection to a supply-voltage source via a first and a second bias resistor respectively, the bases of the third transistor and the fourth transistor being connected to the collectors of the fourth and the third transistor respectively, characterized in that it comprises a second current source (R_{32} , T_{32}) connected to the junction point between the collector of the second transistor (T_2) and the emitter of the fourth transistor (T_4), and a third current source (R_{31} , T_{31}) connected to the junction point between the collector of the first transistor (T_1) and the emitter of the third transistor (T_3), the currents of the second current source (R_{32} , T_{32}) and the third current source (R_{31} , T_{31}) being directed in such a way that they tend to raise the emitter currents of the fourth transistor (T_4) and the third transistor (T_3) respectively, and the sum of their currents (210) being smaller than the current (211) of the first current source (R_3 , T_5).

2. An amplifier stage as claimed in Claim 1, characterized in that the ratio between the sum of the currents (210) of the second current source (R_{32} , T_{32}) and the third current source (R_{31} , T_{31}) and the current (211) of the first current source (R_3 , T_5) is



substantially equal to 0.2.

3. A high-frequency amplifier comprising a plurality of direct-coupled cascaded differential stages, characterized in that said stages comprise an input stage as claimed in Claim 1 which is coupled directly to a subsequent stage, and in that the product of the current from the second current source or the third current source and the resistance of the first bias resistor or the second bias resistor is smaller than the linear input range (ΔV) of the subsequent stage.

4. An amplifier as claimed in Claim 3, characterized in that the subsequent differential stage is an output stage comprising a fifth transistor (T_6) and a sixth transistor (T_7) whose bases are connected to the collectors of the first transistor (T_1) and the second transistor (T_2) respectively, whose collectors are connected to the power-supply terminals for connection to said supply-voltage source by a third bias resistor (R_6) and a fourth bias resistor respectively (R_7) and whose emitters are interconnected by a first capacitor (C_1) arranged in parallel with a first resistive divider bridge (R_8, R_9) whose centre point is connected to a second current source (R_{10}, T_8), and in that the elements (R_8, R_9) of the first resistive divider bridge, the first capacitor (C_1) and the bias resistors are selected in such a way that the amplifier has an overall gain higher than 1 in its operating frequency range.

5. An amplifier as claimed in Claim 4, characterized in that said choice is such that the amplifier also has a gain higher than a given nominal value at its minimum operating frequency.

6. An amplifier as claimed in Claim 4 or 5, characterized in that the collectors of the fifth transistor (T_6) and the sixth transistor (T_7) are connected to the bases of an output transistor (T_9, T_{10}) arranged as an emitter-follower.



7. An amplifier as claimed in any one of Claims 4 to 6, characterized in that, in order to limit the gain for d.c. components of the input signals (E_1 , E_2), it comprises a second resistive divider bridge (R_{11} , R_{12}) which is arranged between the collector of the fifth transistor (T_6) and earth and whose centre point, which is decoupled by means of a second capacitor (C_2), is connected to the base of the first transistor (T_1) by a first input resistor (R_{14}) and a third resistive divider bridge (R_{21} , R_{22}) which is arranged between the collector of the sixth transistor (T_7) and earth and whose centre point, which is decoupled by means of a third capacitor (C_3), is connected to the base of the second transistor (T_2) via a second input resistor (R_{24}).

8. An amplifier as claimed in any one of the Claims 4 to 7, characterized in that its gain is such that for input signals of a level higher than a nominal minimum level the output stage operates in the saturated mode, in such a way that clipped output signals are produced in response to sinusoidal input signals.

9. A high-frequency amplifier comprising a plurality of cascaded differential stages, characterized in that said stages comprise an input stage as claimed in Claim 1, coupled to an emitter-coupled stage comprising a seventh transistor (T_{36}) and an eight transistor (T_{37}) whose bases receive the output signals of the input stage, and in that the input stage and the emitter-coupled differential stage are coupled by a first base resistor (R_{42}) and a second base resistor (R_{41}) which are arranged in series in the base of the seventh transistor (T_{36}) and the eight transistor (T_{37}) respectively and whose resistance values lie between 1 and 2 times the intrinsic base resistance of said seventh and eighth transistor.

10. A high-frequency amplifier as claimed in Claim 9, characterized in that the value of one said base resistors is substantially equal to 1.2 times said intrinsic base resistance.

