

ABSTRACT OF THE DISCLOSURE

MEMORY CONTROLLER WITH PROGRAMMABLE ADDRESS CONFIGURATION

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A memory controller (110) comprises a programmable interface (114) coupled to address circuitry (113). The programmable interface (114) receives a configuration signal (119) into the memory controller (110) indicating a selected address configuration.

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The address circuitry (113) processes system addresses (103) based on the selected address configuration to generate memory addresses (106). The configuration signal (119) may also indicate a selected memory configuration, and the address circuitry (113) processes the system addresses (103) based on the selected memory configuration to generate memory device selections (117).

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Figure 1