# CLAIMS

1. A data receiving circuit, comprising:

a first amplification module, configured to receive a data signal, a first reference signal and a second reference signal, perform first comparison on the data signal and the first reference signal in response to a sampling clock signal and output a first signal pair as a result of the first comparison, and perform second comparison on the data signal and the second reference signal, and output a second signal pair as a result of the second comparison, wherein a level of the first reference signal is different from a level of the second reference signal, the first signal pair comprises a first signal and a second signal, and the second signal pair comprises a third signal and a fourth signal; and

a second amplification module, configured to receive an enable signal and a feedback signal, selectively receive the first signal pair or the second signal pair as an input signal pair based on the feedback signal during a period in which the enable signal is at a first level, receive the first signal pair as the input signal pair during a period in which the enable signal is at a second level, amplify a voltage difference of the input signal pair, and output a first output signal and a second output signal as an amplification result, wherein the feedback signal is obtained based on previously received data.

2. The data receiving circuit of claim 1, wherein the first amplification module is further configured to receive the enable signal, perform the first comparison to output the first signal pair and perform the second comparison to output the second signal pair during the period in which the enable signal is at the first level, and merely perform the first comparison to output the first signal pair during the period in which the enable signal is at the second level, wherein a level of the first reference signal is greater than a level of the second reference signal.

3. The data receiving circuit of claim 2, wherein the sampling clock signal comprises a first sampling clock signal and a second sampling clock signal; and the first amplification module comprises:

a first comparison circuit, having a first node and a second node, and configured to

receive the data signal and the first reference signal, perform the first comparison in response to the first sampling clock signal, output the first signal through the first node, and output the second signal through the second node;

a clock generation circuit, configured to receive the enable signal and an original sampling clock signal, and output the second sampling clock signal, wherein a phase of the second sampling clock signal is opposite to a phase of the original sampling clock signal during the period in which the enable signal is at the first level, and the second sampling clock signal is a logic high-level signal during the period in which the enable signal is at the second level; and

a second comparison circuit, having a third node and a fourth node, and configured to receive the data signal and the second reference signal, perform the second comparison in response to the second sampling clock signal during the period in which the enable signal is at the first level, output the third signal through the third node and output the fourth signal through the fourth node, turn on a connection path between the third node and ground when the enable signal is at the second level, and turn on a connection path between the fourth node and ground.

4. The data receiving circuit of claim 3, wherein the first comparison circuit comprises:

a first current source, connected between a power node and a fifth node, and configured to supply a current to the fifth node in response to the first sampling clock signal;

a first comparison unit, connected to the first node, the second node and the fifth node, and configured to receive the data signal and the first reference signal, perform the first comparison when the first current source supplies the current to the fifth node, and output the first signal and the second signal; and

a first reset unit, connected to the first node and the second node, and configured to reset the first node and the second node in response to the first sampling clock signal; and

the second comparison circuit comprises:

a second current source, connected between the power node and a sixth node, and configured to supply a current to the sixth node in response to the second sampling clock signal;

a second comparison unit, connected to the third node, the fourth node and the sixth node, and configured to receive the data signal and the second reference signal, perform the second comparison when the second current source supplies the current to the sixth node, and output the third signal and the fourth signal; and

a second reset unit, connected between the third node and the fourth node, and configured to reset the third node and the fourth node in response to the second sampling clock signal.

5. The data receiving circuit of claim 4, wherein the first current source comprises:

a first PMOS transistor, connected between the power node and the fifth node, wherein a gate of the first PMOS transistor is configured to receive the first sampling clock signal; and

the second current source comprises:

a second PMOS transistor, connected between the power node and the sixth node, wherein a gate of the second PMOS transistor is configured to receive the second sampling clock signal.

6. The data receiving circuit of claim 4, wherein the first comparison unit comprises:

a third PMOS transistor, connected between the first node and the fifth node, wherein a gate of the third PMOS transistor is configured to receive the data signal; and

a fourth PMOS transistor, connected between the second node and the fifth node, wherein a gate of the fourth PMOS transistor is configured to receive the first reference signal; and

the second comparison unit comprises:

a fifth PMOS transistor, connected between the third node and the sixth node, wherein a gate of the fifth PMOS transistor is configured to receive the data signal; and

a sixth PMOS transistor, connected between the fourth node and the sixth node, wherein a gate of the sixth PMOS transistor is configured to receive the second reference signal.

7. The data receiving circuit of claim 4, wherein the first reset unit comprises:

a first NMOS transistor, connected between the first node and ground, wherein a gate of the first NMOS transistor is configured to receive the first sampling clock signal; and

a second NMOS transistor, connected between the second node and ground, wherein a gate of the second NMOS transistor is configured to receive the first sampling clock signal; and

the second reset unit comprises:

a third NMOS transistor, connected between the third node and ground, wherein a gate of the third NMOS transistor is configured to receive the second sampling clock signal; and

a fourth NMOS transistor, connected between the fourth node and ground, wherein a gate of the fourth NMOS transistor is configured to receive the second sampling clock signal.

8. The data receiving circuit of claim 3, wherein the clock generation circuit comprises:

a first NAND gate circuit, wherein one input of the first NAND gate circuit is configured to receive the original sampling clock signal, the other input of the first NAND gate circuit is connected to a power node, and an output of the first NAND gate circuit is configured to output the first sampling clock signal.

9. The data receiving circuit of claim 3, wherein the clock generation circuit comprises:

a second NAND gate circuit, wherein one input of the second NAND gate circuit is configured to receive the original sampling clock signal, and the other input of the second NAND gate circuit is configured to receive the enable signal; and an output of the second NAND gate circuit is configured to output the second sampling clock signal.

10. The data receiving circuit of claim 1, wherein the second amplification module comprises:

a decision equalization enable unit, configured to receive the feedback signal and the enable signal;

a first input unit, connected to a seventh node and an eighth node, and configured to be connected to the decision equalization enable unit, be turned on under control of the decision equalization enable unit, receive the first signal pair, perform third comparison, and provide signals to the seventh node and the eighth node respectively as a result of the third comparison;

a second input unit, connected to the seventh node and the eighth node, and configured to be connected to the decision equalization enable unit, be turned on under control of the decision equalization enable unit, receive the second signal pair, perform fourth comparison, and provide signals to the seventh node and the eighth node respectively as a result of the fourth comparison, wherein

the first input unit and the second input unit are alternatively turned on under control of the decision equalization enable unit; and

a latch unit, connected to the seventh node and the eighth node, and configured to amplify and latch the signal of the seventh node and the signal of the eighth node, and output the first output signal through a first output node and output the second output signal through a second output node.

11. The data receiving circuit of claim 10, wherein the feedback signal comprises a differential first feedback signal and a second feedback signal; and the decision equalization enable unit comprises:

a first enable unit, connected between ground and the first input unit and between ground and the second input unit, and configured to receive the enable signal, the first feedback signal and the second feedback signal, to control one of the first input unit and the second input unit to be connected to ground; and

a second enable unit, connected between ground and the first input unit and between ground and the second input unit, and configured to receive a complementary enable signal, to control the first input unit to be connected to ground, wherein a level of the complementary enable signal is opposite to a level of the enable signal; wherein

the first enable unit and the second enable unit are alternatively selected to be turned on.

12. The data receiving circuit of claim 11, wherein the first input unit comprises:

a fifth NMOS transistor, wherein a drain of the fifth NMOS transistor is connected to the seventh node, a source of the fifth NMOS transistor is connected to the first enable unit and the second enable unit, and a gate of the fifth NMOS transistor is configured to receive the first signal; and

a sixth NMOS transistor, wherein a drain of the sixth NMOS transistor is connected to the eighth node, a source of the sixth NMOS transistor is connected to the first enable unit and the second enable unit, and a gate of the sixth NMOS transistor is configured to receive the second signal; and

the second input unit comprises:

a seventh NMOS transistor, wherein a drain of the seventh NMOS transistor is connected to the seventh node, a source of the seventh NMOS transistor is connected to the first enable unit and the second enable unit, and a gate of the seventh NMOS transistor is configured to receive the third signal; and

an eighth NMOS transistor, wherein a drain of the eighth NMOS transistor is connected to the eighth node, a source of the eighth NMOS transistor is connected to the first enable unit and the second enable unit, and a gate of the eighth NMOS transistor is configured to receive the fourth signal.

13. The data receiving circuit of claim 12, wherein the first enable unit comprises:

a ninth NMOS transistor and a tenth NMOS transistor, wherein a drain of the ninth NMOS transistor is connected to the source of the fifth NMOS transistor and the source of the sixth NMOS transistor, a source of the ninth NMOS transistor is connected to a drain of the tenth NMOS transistor, a gate of the ninth NMOS transistor is configured to receive the first feedback signal, a gate of the tenth NMOS transistor is configured to receive the enable signal, and a source of the tenth NMOS transistor is connected to ground; and

an eleventh NMOS transistor and a twelfth NMOS transistor, wherein a drain of

the eleventh NMOS transistor is connected to the source of the seventh NMOS transistor and the source of the eighth NMOS transistor, a source of the eleventh NMOS transistor is connected to a drain of the twelfth NMOS transistor, a gate of the eleventh NMOS transistor is configured to receive the second feedback signal, a gate of the twelfth NMOS transistor is configured to receive the enable signal, and a source of the twelfth NMOS transistor is connected to ground;

and/or

wherein the second enable unit comprises:

a thirteenth NMOS transistor, wherein a drain of the thirteenth NMOS transistor is connected to the source of the fifth NMOS transistor and the source of the sixth NMOS transistor, a source of the thirteenth NMOS transistor is connected to ground, and a gate of the thirteenth NMOS transistor is configured to receive the complementary enable signal; and

a fourteenth NMOS transistor, wherein a drain of the fourteenth NMOS transistor is connected to the source of the seventh NMOS transistor and the source of the eighth NMOS transistor, a source of the fourteenth NMOS transistor is connected ground, and a gate of the fourteenth NMOS transistor is configured to receive the complementary enable signal.

14. The data receiving circuit of claim 10, wherein the latch unit comprises:

a fifteenth NMOS transistor and a seventh PMOS transistor, wherein a gate of the fifteenth NMOS transistor and a gate of the seventh PMOS transistor are connected to the second output node, a source of the fifteenth NMOS transistor is connected to the seventh node, a drain of the fifteenth NMOS transistor and a drain of the seventh PMOS transistor are connected to the first output node, and a source of the seventh PMOS transistor is connected to a power node; and

a sixteenth NMOS transistor and an eighth PMOS transistor, wherein a gate of the sixteenth NMOS transistor and a gate of the eighth PMOS transistor are connected to the first output node, a source of the sixteenth NMOS transistor is connected to the eighth node, a drain

of the sixteenth NMOS transistor and a drain of the eighth PMOS transistor are connected to the second output node, and a source of the eighth PMOS transistor is connected to the power node.

15. The data receiving circuit of claim 14, wherein the second amplification module further comprises:

a third reset unit, connected between the power node and an output of the latch unit, and configured to reset the output of the latch unit.

16. The data receiving circuit of claim 15, wherein the third reset unit comprises:

a ninth PMOS transistor, connected between the first output node and the power node, wherein a gate of the ninth PMOS transistor is configured to receive an original sampling clock signal; and

a tenth PMOS transistor, connected between the second output node and the power node, wherein a gate of the tenth PMOS transistor is configured to receive the original sampling clock signal.

17. A data receiving system, comprising:

a plurality of cascaded data transmission circuits, each of which comprises the data receiving circuit of any of claims 1 to 16 and a latch circuit connected to the data receiving circuit, wherein

an output signal of the data transmission circuit at a previous stage is used as a feedback signal of the data transmission circuit at a subsequent stage; and

an output signal of the data transmission circuit at a last stage is used as a feedback signal of the data transmission circuit at a first stage.

18. The data receiving system of claim 17, wherein the data receiving circuit is configured to receive data in response to a sampling clock signal; and the data receiving system comprises 4 cascaded data transmission circuits, and a phase difference between the sampling clock signals of the data receiving circuits at adjacent stages is 90°.

19. The data receiving system of claim 17, wherein a first output signal and a second output signal outputted by a second amplification module of the data receiving circuit at the previous stage are used as feedback signals of the data receiving circuit at the subsequent stage; or a signal outputted by the latch circuit at the previous stage is used as the feedback signal of the data receiving circuit at subsequent stage.

20. A memory device, comprising:

a plurality of data ports; and

a plurality of data receiving systems of any of claims 17 to 19, each of which corresponds to one data port.