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(54) Title: WORK FUNCTION LAYER FOR PMOS STACK

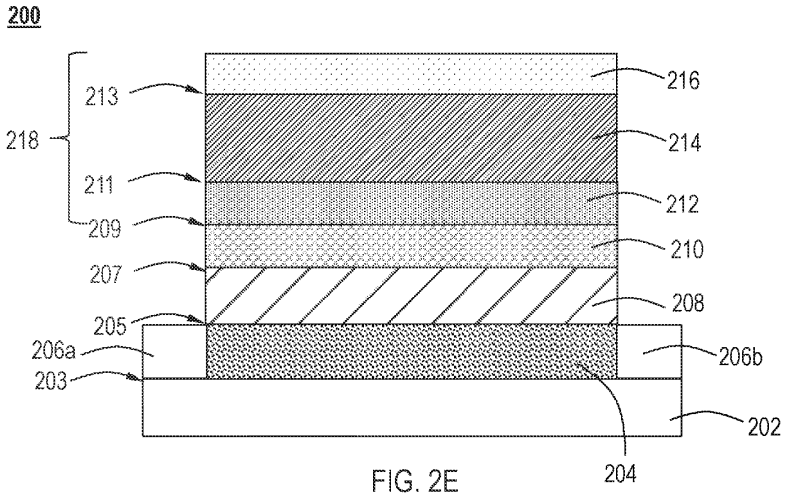

FIG. 2E

(57) Abstract: Methods of manufacturing semiconductor devices are described. Embodiments of the disclosure advantageously provide semiconductor devices which comprise a PMOS high-k metal gate (HKMG) stack having a depinning layer to achieve the desired bandedge performance because of the significant flatband voltage (V_{fb}) rolloff. The semiconductor devices described comprise a channel separating a source region and a drain region, an interfaciai layer on the channel, a high-K dielectric layer on the interfaciai layer, a depinning layer on the high-K dielectric layer, a P-metal layer on the depinning layer, and a barrier layer on the depinning layer.

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