

ABSTRACT

The present invention provides a digital signal processing apparatus and a method for controlling the apparatus that allow for a reduction of circuit size to minimize an increase in power consumption and the costs of circuitry and an improvement in signal processing speed. To achieve this, the present invention eliminates a circuit arrangement that was conventionally required for executing a compare instruction, conditional jump instruction, and jump instruction, by adding a relatively small-sized circuit such as an encoder 51 for processing an external signal 10 and a capability of decoding a condition determination data select instruction.



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