

SEMICONDUCTOR STRUCTURE AND MEMORY

ABSTRACT

Embodiments of the disclosure provide a semiconductor structure and a memory. The semiconductor structure includes a first active area; a first gate located on the first active area, the first active area and the first gate being configured to form a first transistor; a second active area, the second active area and the first active area being arranged along a first direction, the second active area and the first active area being independent from each other; a second gate located on the second active area, the second active area and the second gate being configured to form a second transistor, wherein sizes of the first transistor and the second transistor are same, a deviation between an electrical parameter of the first transistor and an electrical parameter of the second transistor is below a preset threshold, and the first transistor and the second transistor belong to a cross coupling amplifying unit.

[Fig. 4]