THIN INTEGRAL RESISTOR/CAPACITOR/INDUCTOR PACKAGE, METHOD OF MANUFACTURE

Abstract of the disclosure

A thin electrical circuitry structure is formed which contains conductive circuitry traces, integral capacitors and integral resistors. A first laminate structure comprises a conductive foil having a layer of embeddable dielectric material laminated thereto. A second laminate structure comprises a conductive foil having a layer of resistive material on one side, the thickness of the resistive material layer being less than that of the layer of embeddable dielectric material. The resistive material layer is circuitized to produce resistive patches, and the two structures are laminated together, embedding the resistive patches in the dielectric material layer. One of the foils is circuitized providing circuitry traces, optional inductor coils, and capacitor plates. That foil embedded in dielectric laminate to support the structure for further processing. The other foil is then circuitized providing circuitry traces, optional inductor coils and capacitor plates. Traces on one side connector with the resistive material patches to provide the resistors.

Fig. 6