Solar cell and method for manufacturing such a solar cell

Field

The present invention relates to a solar cell. Also, the present invention relates to a method for manufacturing such a solar cell.

Background

Such a solar cell relates to a solar cell with p- or n-type base.

The solar cell comprises a semiconductor substrate, e.g. silicon, which is covered on a back side by the p- or n-type back surface field (BSF) layer and on a front side by an emitter layer of a conductivity type opposite to that of the base layer. The front side of the substrate is arranged to be directed towards a light source during use of the solar cell.

In the prior art, the p- or n-type back surface field layer (BSF layer), is for example manufactured by a screen printing process (but also $POCl_3$ face-to-face tube furnace diffusion, spray coating, spin coating, etc. can be used). During the screen printing process, a paste that comprises a p- or n-type element as dopant element is printed one-sidedly on the back side of the substrate. Next, a first diffusion process is carried out in which the substrate with the printed paste is heated to diffuse the p- or n-type element into the substrate to form the p- or n-type BSF layer. Such a heat treatment is typically carried out in an inline diffusion furnace. Subsequently, on the front side a layer of opposite conductivity type is formed by a second diffusion process, which is carried out in a second diffusion furnace. Alternatively, the emitter layer may be created first, followed by a creation of the BSF base layer.

The prior art manufacturing process has some disadvantages. The screen printing method to form the BSF layer on the back side may cause contamination of the front side of the substrate by parasitic diffusion or spill over of the dopant source to the front side. Parasitic diffusion of the dopant on the front side results in a non-uniform dopant concentration profile for the emitter layer which will adversely affect the efficiency of the solar cell. For example, shunt or high reverse current are typical effects. Furthermore, screen printing reduces the yield of the manufacturing process due to a relatively high chance of breakage of substrates.

Also, for n-type BSF layers that use phosphorus as n-type dopant, a one-sided diffusion results in a less efficient gettering of impurities from the substrate.

Summary of the invention

It is an object of the present invention to provide a method for manufacturing the solar cell with p- or n-type base, which overcomes or reduces the disadvantages as mentioned above.

According to a first aspect of the invention, the object is achieved by a method for manufacturing a solar cell from a semiconductor substrate of a first conductivity type, the semiconductor substrate having a front surface and a back surface, the method comprising in a sequence:

texturing the front surface to create a textured front surface ;

creating by diffusion of a dopant of the first conductivity type a first conductivity-type doped layer in the textured front surface and a back surface field layer of the first conductivity type in the back surface;

removing the first conductivity-type doped layer from the textured front surface by an etching process adapted for retaining texture of the textured front surface;

creating a layer of a second conductivity type on the textured front surface by diffusion of a dopant of the second conductivity type into the textured front surface.

Advantageously, the method provides an enhanced manufacturing with less variation between individual solar cells: A parasitic doping (either p-type or n-type) from one surface of the silicon substrate to another surface, especially from the BSF side to the emitter side, is prevented in an easy way by the method. Also, a screen printing step is omitted which reduces yield loss due to breakage. Moreover, two-sided diffusion of phosphorus in both front and back surfaces allows an improved gettering of impurities from the silicon substrate.

In an embodiment, the invention relates to the method as described above, wherein texturing the front surface to create a textured front surface comprises texturing the back surface to create a textured back surface.

In an embodiment, the invention relates to the method as described above, wherein the creation of the back surface field layer is preceded by polishing the textured back surface of the semiconductor substrate.

In an embodiment, the invention relates to the method as described above, comprising during the diffusion of the dopant of the first conductivity type, a formation

of a dopant containing glassy layer on the front surface and the back surface from a precursor of the first conductivity type, the dopant containing glassy layer acting as dopant source for the semiconductor substrate.

In an embodiment, the invention relates to the method as described above, comprising removing the dopant containing glassy layer from the front surface and the back surface preceding the removal of the first conductivity-type doped layer from the textured front surface.

In an embodiment, the invention relates to the method as described above, comprising removing the dopant containing glassy layer from the front surface while removing the first conductivity-type doped layer from the textured front surface, in a single sided etching process.

In an embodiment, the invention relates to the method as described above, comprising removing the dopant containing glassy layer from the back surface after the removal of the dopant containing glassy layer from the front surface and the first conductivity-type doped layer from the textured front surface in the single sided etching process.

In an embodiment, the invention relates to the method as described above, comprising preceding the removal of the first conductivity-type doped layer from the textured front surface:

- removing the dopant containing glassy layer from the front surface and the back surface, and
- creating a protective layer on the back surface field layer.

In an embodiment, the invention relates to the method as described above, comprising:

- after creating the first conductivity-type doped layer in the textured front surface and the back surface field layer of the first conductivity type in the back surface: creating a protective layer on the back surface field layer,

before the removal of the dopant containing glassy layer from the front surface while removing the first conductivity-type doped layer from the textured front surface in a single sided etching process.

In an embodiment, the invention relates to the method as described above, comprising:

after the removal of the dopant containing glassy layer from the front surface while

removing the first conductivity-type doped layer from the textured front surface in a single sided etching process and preceding the creation of the layer of the second conductivity type on the textured front surface:

- removing the protective layer and the dopant containing glassy layer from the back surface.

In an embodiment, the invention relates to the method as described above, wherein the protective layer comprises a coating layer containing at least one material selected from a group of aluminum oxide (Al2O3), silicon nitride (SiNx), a dielectric, and a resist.

In an embodiment, the invention relates to the method as described above, wherein creating the back surface field layer by diffusion of the dopant of the first conductivity type comprises exposing the back surface to a precursor of the first conductivity type at elevated temperature.

In an embodiment, the invention relates to the method as described above, wherein the precursor of the first conductivity type contains the dopant of the first conductivity type; the precursor being selected from one of a gaseous precursor, a liquid precursor, a paste precursor and a plasma precursor.

In an embodiment, the invention relates to the method as described above, wherein the diffusion of the dopant of the first conductivity type is optimized to create a thickness of the first conductivity-type doped layer in the textured front surface which is 0.7 micron or less.

In an embodiment, the invention relates to the method as described above, wherein the diffusion of the dopant of the first conductivity type is optimized to create a thickness of the first conductivity-type doped layer in the textured front surface which is 0.3 micron or less. In an embodiment, the invention relates to the method as described above, wherein creating the layer of the second conductivity type on the textured front surface by diffusion of the dopant of the second conductivity type comprises exposing the textured front surface to a precursor of the second conductivity type at elevated temperature.

In an embodiment, the invention relates to the method as described above, wherein the precursor of the second conductivity type is a gaseous precursor, the gaseous precursor containing the dopant of the second conductivity type.

In an embodiment, the invention relates to the method as described above, wherein the first conductivity type is n-type and the second conductivity type is p-type, or

the first conductivity type is p-type and the second conductivity type is n-type.

In an embodiment, the invention relates to the method as described above, wherein a thickness of the first conductivity-type doped layer is less than an average height of a texture feature on the textured front surface.

In an embodiment, the invention relates to the method as described above, wherein the average height of the texture feature on the textured front surface is at least about 2 micron and the thickness of the first conductivity type doped layer is about 0.7 micron or less.

In an embodiment, the invention relates to the method as described above, wherein the average height of the texture feature on the textured front surface is at least about 2 micron and the thickness of the first conductivity type doped layer is about 0.3 micron or less.

In an embodiment, the invention relates to the method as described above, wherein the etching process adapted for retaining texture of the textured front surface is performed by a single-sided wet-chemical process using an etching agent.

In an embodiment, the invention relates to the method as described above, wherein the etching agent comprises a component for texturing a semiconductor surface.

In an embodiment, the invention relates to the method as described above, wherein the etching agent further comprises a component for polishing the semiconductor surface.

In an embodiment, the invention relates to the method as described above, wherein the etching process adapted for retaining texture of the textured front surface is performed by a dry etching method.

In an embodiment, the invention relates to the method as described above, wherein the removing of the first conductivity type doped layer from the textured front side and the dopant containing glassy layer from the front surface is performed during the etching process adapted for retaining texture of the textured front surface.

In an embodiment, the method as described above further comprises partly smoothening the textured front surface.

The partial smoothening may be performed by etching with a HF and/or HNO_3 containing liquid. The partial smoothening may for instance result in removing away a layer of about 50 nm – 2 μm.

Also advantageously, the method may result in higher efficiency of the solar cells due to improved surface passivation of surfaces with doped layers, when the texture features on these surfaces are (even slightly) smoothened.

Also, the invention relates to a solar cell comprising a semiconductor substrate of a first conductivity type having a textured front surface and a back surface, wherein the textured front surface comprises a second conductivity-type doped layer, wherein the back surface comprises a surface field layer of the first conductivity type.

In an embodiment, the invention relates to the solar cell as described above, wherein the textured front surface comprises a pyramidal shapes containing front surface with intermediate valleys having widths selected from the range of 50-500 nm.

In an embodiment, the invention relates to the solar cell as described above, wherein the textured front surface has valleys with curvatures having radii selected from the range of 25-250 nm.

Further embodiments are defined by the dependent claims as appended.

Brief description of drawings

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying schematic drawings in which corresponding reference symbols indicate corresponding parts, and in which:

Figure 1 shows a flow diagram for a method for manufacturing a solar cell in accordance with a first aspect of the invention;

Figure 2 shows a flow diagram for a method for manufacturing a solar cell in accordance with a second aspect of the invention;

Figure 3 shows a flow diagram for a method for manufacturing a solar cell in accordance with a third aspect of the invention;

Figure 4 shows a flow diagram for a method for manufacturing a solar cell in accordance with a fourth aspect of the invention;

Figure 5 shows a cross-section of a semiconductor substrate for manufacturing the solar cell;

Figure 6a, 6b show a cross-section of the solar cell after a next stage of the method;

Figure 7 shows a cross-section of the solar cell after a further stage of the method;

Figure 8 shows a cross-section of the solar cell after a next stage of the method;

Figure 9 shows a cross-section of the solar cell after a subsequent stage of the method;

Figure 10 shows a cross-section of the solar cell after a further stage of the method;

Figure 11 shows a cross-section of the solar cell after yet a further stage of the method;

Figure 12 shows a cross-section of the solar cell after a further stage in accordance with the second aspect;

Figure 13 shows a cross-section of the solar cell after a subsequent stage in accordance with the second aspect;

Figure 14 shows a cross-section of the solar cell after a further stage in accordance with the third aspect;

Figure 15 shows a cross-section of the solar cell after a next stage in accordance with the third aspect;

Figure 16 shows a cross-section of the solar cell after a further stage in accordance with the fourth aspect;

Figure 17 shows a cross-section of the solar cell after a next stage in accordance with the fourth aspect;

Figure 18 shows a cross-section of the solar cell after a subsequent stage in accordance with the fourth aspect;

Figures 19a, 19b show in some more detail a front surface texture after partial smoothening.

Detailed description

Figure 1 shows a flow diagram for a method for manufacturing a solar cell in accordance with a first aspect of the invention.

According to the first aspect, the method comprises a sequence 100 of processes to manufacture a solar cell with either p- or n-type base.

Below, the sequence 100 is illustrated for a solar cell with n-type base.

A single crystal or multi-crystalline semiconductor substrate i.e., a silicon substrate 1 with n-type conductivity is provided as precursor for the solar cell. The silicon substrate has a front surface 2 and a back surface 3. The front surface is arranged as surface for receiving light during use of the solar cell.

In an alternative embodiment, the silicon substrate is doped to have a conductivity of p-type.

Figure 5 shows a cross-section of the silicon substrate for manufacturing the solar cell.

Referring again to figure 1, next, in process 102, the method provides texturing of the surfaces 2, 3 of the silicon substrate 1 by exposing the surface(s) to be textured to a texture etching agent.

The front surface 2 is textured to create a surface topography (also referred to as texture features) resulting in a low reflectivity of the surface. For example, the texturing recipe can be tuned to obtain as texture features large pyramids on the surface (e.g. an average pyramid height of about 2 microns or more).

In this method the texturing process may be adjusted to maintain a low reflectivity after a later removal step of a doped surface layer. The back surface 3 is either textured to create a surface topography (also referred to as texture features) resulting in a low reflectivity of the surface or polished to create a surface topography resulting in a high reflectivity.

The textured surface of the back surface 3 does not have to be identical to the textured front surface 2.

It is possible to create a surface texture either in a single-sided manner on the front surface 2a or in a two–sided manner on both front and back surfaces 2a, 3a.

In case of two-sided texturing, the back surface 3a may be polished in a single-side polishing etching step to remove the texture, and to improve optical and passivation properties.

Additionally, in process 102 the texturing may be combined with an etching process for saw damage removal. Combining saw damage removal and texturing may be advantageous for silicon substrates that have not been pre-polished after slicing from a silicon ingot. Alternatively, the texturing 102 may also be preceded by such an etching process for saw damage removal.

Figure 6a and 6b show a cross-section of the solar cell after creation of texture.

In the process 102 as described above, the texture is created by exposing the surface(s) to be textured to a texture etching agent. Such a texturing agent may be an alkaline or acid solution, but it could also be a plasma for dry etching.

Figure 6a shows a cross-section of the solar cell after creation of texture on the front and back surfaces 2a, 3a. As shown in figure 6b, it is alternatively possible to create texture in a single-sided manner on only the front surface 2a.

In a further alternative embodiment, it is alternatively possible to create texture in a single-sided manner on only the front surface 2a, by first creating texture in a two sided manner on the front and back surfaces 2a, 3a and subsequently polishing the textured back surface 3a.

Referring again to figure 1, in a subsequent process 103, a back surface field (BSF) layer 4 is created by diffusion of an n-type dopant into the back surface 3; 3a and a doped layer 2c is created by diffusion of an n-type dopant into the textured front surface 2. The doped layer 2c has the same conductivity type as the BSF layer 4 on the back surface 3; 3a.

In an embodiment, the process 103 comprises exposing the back surface 3; 3a to a gaseous n-type precursor in a tube furnace at elevated temperature. The n-type precursor contains the n-type dopant. In an exemplary case, the n-type dopant is phosphorus and the gaseous n-type precursor comprises $POCl_3$ (phosphoryl chloride). On the back surface of the silicon substrate a phosphorus containing glass layer (PSG) 5 is formed during the formation of the BSF layer. The PSG layer 5 acts as dopant source for the silicon substrate 1.

Process 103 is controlled by its process parameters in such a way that the doped layer 2c and the BSF layer 4 will be congruent with the textured shape of the respective surface. To this end, a thickness of the doped layer 2c and the BSF layer is arranged to be less than the height of texture features on the surface(s).

Other diffusion methods, e.g. belt furnace, and diffusion sources, e.g. phosphoric acid containing liquids, applied by spray, vapour, spinning, printing, etc., or plasma implantation doping, etc., may be used.

In an alternative embodiment, the creation of the BSF layer 4 is performed in a front-to-front configuration. This increases throughput and provides a partial screening of the textured front surface(s) from the dopant.

Figure 7 shows a cross-section of the solar cell after process 103 for the creation of the back surface field layer.

In the subsequent process 103 on both the front surface 2 and back surface 3 of the silicon substrate 1 n-type doped layer 2c and BSF layer 4, are respectively created

by diffusion of n-type dopant from an n-type dopant source into the front and back surfaces of the substrate 1.

On the back surface 3; 3a, the BSF layer 4 is formed. On the textured front surface 2a, the n-type doped layer 2c is formed which extends into the substrate 1 until an interface 2b. It is noted that the thickness of the n-type doped layer 2c is arranged to be less than the height of the texture features. In this manner the shape of the n-type doped layer 2c is congruent with the surface texture: i.e. the interface 2b also has a texture.

In the embodiment that the n-type dopant is phosphorus, on the textured front surface and the back surface of the silicon substrate a phosphorus containing glass layer (PSG) 5 is formed during the formation of the BSF layer and the n-type doped layer 2c.

The parameters of BSF diffusion may be specifically tuned, e.g. by increase of oxygen or $POCl_3$ flow, or addition of water vapor, to control the thickness of the PSG layers.

In an embodiment, the diffusion process may be carried out at an elevated temperature, which may be any suitable elevated temperature suitable for the specific diffusion process being applied, for instance depending on the materials that are used. The elevated temperature may also depend on the time during which the elevated temperature is applied. In general the elevated temperature may be between about 600 and about 1200 °C, or between about 780 – 1200 °C. The PSG layer 5 may act as dopant source for the silicon substrate 1.

In an embodiment, the diffusion of phosphorus (the dopant of the first conductivity type) is optimized to create a thickness of the back surface field layer and of the n-type doped layer 2c (a diffused layer containing the dopant of the first conductivity type) of about 0.7 microns.

In an alternative embodiment, a shallow back surface field layer and a shallow n-type doped layer 2c are created. The diffusion of phosphorus (the dopant of the first conductivity type) is then optimized to create a thickness of 0.3 micron or less for the BSF layer and the n-type doped layer 2c. Since the ability to retain texture is determined to some extent by the thickness of the n-type doped layer 2c, for a shallow n-type doped layer 2c (about 0.3 micron or less thick) the texture may be retained more fully and the reflectivity of the front surface may be lower than for a thicker n-type doped layer (say about 0.7 micron thick).

In figure 7, the embodiment is shown in which the back surface is flat, not textured. The skilled person will appreciate that the process 103 may also be executed on a substrate that comprises a textured back surface 3a.

Referring again to figure 1, in a following process 104, the method provides a removal of a layer such as a PSG layer covering n-type doped layers 2c and 4 from the textured front surface 2a and from the back surface 4 by an etching process i.e., either wet or dry etching.

Figure 8 shows a cross-section of the solar cell after process 104.

During process 104, the method provides a removal of any top layer such as the PSG layer from the doped layers on the back surface and the textured front surface,

On the front surface the n-type doped layer 2c is exposed after the removal of the top layer such as the PSG layer. On the back surface the back surface field layer 4 is exposed after removal of the PSG layer.

Because the removal of the PSG layer exposes the semiconductor surface at the back surface and renders the back side hydrophobic it will beneficially help to avoid that in a further single sided etching process to remove the n-type doped layer 2c (as will be described below in more detail), the etching liquid will wet the back surface.

Referring again to figure 1, in a subsequent process 105, the method provides etching of the n-type doped layer 2c for removal from the textured front surface 2a by an etching agent. The etching agent is arranged to retain a texture of the front surface (second textured front surface 2b) so as to maintain a low reflectivity of the second textured front surface 2b. This can be satisfied if the shape of the n-type doped layer 2c on the front surface is congruent with the texture in the original textured front surface.

Such an etching agent may be an alkaline etching agent in case of a single-crystalline or a multi-crystalline substrate.

In an embodiment, a texturizing component of the alkaline etching agent comprises an alkaline component soluble in water such as potassium hydroxide or sodium hydroxide. In a further embodiment, the alkaline etching agent comprises one or more additives such as isopropanol.

Alternatively, the etching agent may be an acidic etching agent, which can be used for both single crystalline and multi-crystalline textured surfaces. The acidic etching agent can optionally be arranged for minor polishing, or it can be arranged for further texturing to increase the fine texture of the (second) textured front surface 2b.

In an embodiment, a polishing component of the acidic etching agent comprises an oxidizing component for creating an oxidized surface layer and an oxide etchant for etching the oxidized surface layer. In an example, the oxidizing component is nitric acid (HNO_3) and the oxide etchant is fluoric acid (HF). In a further example, the oxidizing component also comprises additives like water or acetic acid.

A typical removal of silicon from the textured front surface would be between about 0.1 micron and about 2 micron. This will depend on the thickness of the n-type dopant layer 2c, i.e., the extension of the dopant concentration profile into the front surface. This will in turn depend on process parameters such as the temperature and the duration of the BSF-diffusion process.

In this embodiment, the etching is performed as a single-side etch; that means the etching liquid will wet the front surface, but not the rear surface or only a very minor edge region of the rear surface.

Alternatively, the etching can be done by a dry plasma etching step.

Experimentally it is verified that the texture is retained during the etching of the n-type doped layer 2c. An optical reflection of a light beam on the textured front surface at a wavelength of 1000 nm, after removing of the first conductivity doped layer, increases by less than 5% and preferably by less than 3%.

Figure 9 shows a cross-section of the solar cell after process 105.

During process 105, the exposed n-type doped layer 2c from the front surface is removed by an etching process. The etching process is arranged to retain a texture of the textured front surface (second textured front surface 2b after etching) so as to maintain a low reflectivity of the second textured front surface 2b.

Referring again to figure 1, in a next process 106, the method provides the creation of a p-type (emitter) layer 6 on the second textured front surface 2b. The second textured front surface 2b is exposed at elevated temperature to a p-type dopant.

The p-type dopant is for example boron. The p-type dopant may be a gaseous p-type precursor, for example a boron containing gas e.g. BBr_3 (boron tri bromide).

In an embodiment, the elevated temperature may be any suitable elevated temperature suitable for the specific diffusion process being applied for instance depending on the materials that are used.. The elevated temperature may also depend on the time during which the elevated temperature is applied. In general the elevated

temperature may be between about 700 and about 1200 °C, or between about 780 – 1200 °C.

During the process 106 for creating the emitter layer 6 which is a diffusion-driven process, a boron containing glassy layer (BSG layer) 7 is formed on the second textured front surface 2b and on the back surface 4.

It is noted that the BSF layer 4 on the back surface develops further by co-diffusion, i.e., diffusion of the n-type dopant from the BSF layer deeper into the silicon substrate simultaneously with the formation of the p-type emitter layer on the front surface.

In an embodiment, after co-diffusion the BSF layer has a sheet resistance between about 20 and about 30 Ohm/square and the emitter layer has a sheet resistance between about 50 and about 70 Ohm/square.

In another embodiment, after co-diffusion the BSF layer has a sheet resistance between about 5 and about 100 Ohm/square and the emitter layer has a sheet resistance between about 50 and about 150 Ohm/square.

In an alternative embodiment, advantageously, the diffusion is performed in a back-to-back configuration. This increases throughput and provides a partial screening of the back surface(s) from the dopant.

However, it is also noted that for solar cell efficiency the BSF advantageously has a higher doping level than the emitter. Concomitantly, if an emitter diffusion is performed on top of the BSF then this will usually not fully compensate the dopant level in the BSF layer. It is therefore usually not required to have a protection layer (such as a PSG or a dielectric coating such as SiN_x) on top of the BSF during the emitter diffusion. However, a partial compensation of the BSF by the emitter diffusion may reduce the field-effect passivation by the BSF. To eradicate such an effect one can use a protection layer as described in relation to Fig. 3 to prevent or minimize emitter diffusion on top of the BSF. Moreover, a higher doping level for the BSF enhances the rear-side field-effect passivation while a higher doping level in the emitter can enhance recombination losses.

Figure 10 shows a cross-section of the solar cell after process 106.

During process 106, the method provides the creation of a p-type (emitter) layer 6 by diffusion in the second textured front surface 2b.

The second textured front surface 2b is exposed to a p-type dopant, for example boron. The p-type dopant may be a boron containing gas e.g. BBr_3. A boron containing glassy layer (BSG layer) 7 is formed on the textured front surface 2b and on the back surface field layer 4 on the back surface.

It is noted that the creation of the p-type layer 6 may be done by various diffusion methods, e.g. tube or belt furnace, and diffusion sources, e.g. boric acid containing liquids, applied by spray, vapour, spinning, printing, etc., or plasma implantation doping.

Referring again to figure 1, next in process 107, the method provides a removal of the BSG layer 7 from the second textured front surface 2b and to expose the p-type emitter layer. Also, the method provides a removal of the BSG layer 7 from the back surface field layer 4 on the back surface and to expose the BSF layer.

After the sequence of processes as described above, the method provides a silicon substrate which comprises an n-type back surface field layer 4 on the back surface 3; 3a and a p-type emitter layer 6 on the second textured front surface 2b.

Figure 11 shows a cross-section of the solar cell after process 107.

During process 107, the BSG layer 7 is removed from the p-type emitter layer 6 at the second textured front surface and from the back surface field layer 4 by etching.. The solar cell in this stage comprises the silicon substrate 1, the back surface field layer 4 on the back surface 3 of the substrate, and a p-type emitter layer 6 on the textured front surface 2b of the substrate.

The solar cell manufacturing process may be completed with methods known in the state of the art, such as depositions of passivating and antireflective coating, screen printing of metallization patterns, firing-through, junction isolation, etc.

Figure 2 shows a flow diagram for a method 100a for manufacturing a solar cell in accordance with a second aspect of the invention.

In Figure 2 entities with the same reference number as shown in the preceding figures refer to corresponding entities.

According to this aspect, in the sequence, after process 101, 102 and 103 (i.e., providing the semiconductor substrate; texturing at least the front surface of the semiconductor substrate, and the creation of the back surface field layers on the textured front surface and on the back surface), the method comprises in a process 104a

a removal of the PSG layer 5 from the textured front surface and a removal of the n-type doped layer 2c from the textured front surface by a single side etching process.

Figure 12 shows a cross-section of the solar cell after process 104a in accordance with the second aspect.

In Figure 12 entities with the same reference number as shown in the preceding figures refer to corresponding entities.

After process 104a, the secondary textured front surface 2b is exposed, while on the back surface 3 the back surface field layer 4 is present directly on the semiconductor 1. The back surface field layer 4 is covered by the back surface PSG layer 5.

Referring again to figure 2, in a subsequent process 105a after process 104a, the method provides a removal of the PSG layer 5 from the back surface so as to expose the back surface field layer 4.

Figure 13 shows a cross-section of the solar cell after process 105a.

Next, the method according to the second aspect of the invention continues with processes 106 and 107 as described above with reference to figures 1, 10 and 11.

Figure 3 shows a flow diagram for a method 100b for manufacturing a solar cell in accordance with a third aspect of the invention.

In Figure 3 entities with the same reference number as shown in the preceding figures refer to corresponding entities.

According to this aspect, in the sequence, after process 101, 102, 103 and 104 (i.e., providing the semiconductor substrate; texturing at least the front surface of the semiconductor substrate, the creation of the back surface field layers on the textured front surface and on the back surface, and the removal of the PSG layers from the textured front surface and the back surface), the method comprises in a process 108a a creation of a protective layer 5a on the back surface field layer 4.

Figure 14 shows a cross-section of the solar cell after process 108a in accordance with the third aspect.

In Figure 14 entities with the same reference number as shown in the preceding figures refer to corresponding entities.

After process 108a, the back surface 3 of the semiconductor substrate 1 is covered by the back surface field layer 4. The back surface field layer is covered by the

protective layer 5a. On the textured front surface 2, the semiconductor substrate 1 is covered by the n-type doped layer 2c.

In an embodiment, the method provides a deposition of a coating layer as protective layer 5a on the back surface field layer 4. Such a coating layer may comprise aluminum oxide (Al_2O_3), silicon nitride (SiN_x), or another dielectric.

Referring again to figure 3, after process 108a to create the protective layer 5a on the back surface field layer, the method continues with process 105 to remove the n-type doped layer 2c from the textured front surface by either a single sided etching process as described above with reference to figure 1 or by a two sided etching process since the protective layer covers the back surface field layer. The result is shown in figure 15 which shows a cross-section of the solar cell after process 105.

After process 105 to remove the n-type doped layer 2c from the textured front surface, the back surface 3 of the semiconductor substrate 1 is covered by the back surface field layer 4. The back surface field layer is covered by the protective layer 5a. The secondary textured front surface 2b is freely exposed.

Next, the method according to the third aspect of the invention continues with processes 106 and 107 as described above with reference to figures 1, 10 and 11.

Figure 4 shows a flow diagram for a method 100c for manufacturing a solar cell in accordance with a fourth aspect of the invention.

In Figure 4 entities with the same reference number as shown in the preceding figures refer to corresponding entities.

According to this aspect, in the sequence, after process 101, 102 and 103 (i.e., providing the semiconductor substrate; texturing at least the front surface of the semiconductor substrate, the creation of the back surface field layers on the textured front surface and on the back surface), the method comprises in a process 108b a creation of a protective layer 5a directly on the PSG layer 5 on the back surface of the semiconductor substrate.

In an embodiment, the method provides a deposition of a coating layer as protective layer 5a on the PSG layer 5. Such a coating layer may comprise aluminum oxide (Al_2O_3), silicon nitride (SiN_x), or another dielectric, or a resist, etc..

According to this fourth aspect, the PSG layer 5 on the back surface of the semiconductor substrate is not removed before the creation of the protective layer 5a.

Figure 16 shows a cross-section of the solar cell after process 108b in accordance with the fourth aspect.

In Figure 16 entities with the same reference number as shown in the preceding figures refer to corresponding entities.

After process 108b, the back surface 3 of the semiconductor substrate 1 is covered by the back surface field layer 4. The back surface field layer itself is covered by the PSG layer 5. The PSG layer 5 on the back surface field layer 4 is covered by the protective layer 5a. On the textured front surface 2, the semiconductor substrate 1 is covered by the n-type doped layer 2c.

The textured front surface of the semiconductor substrate is covered by the n-type doped layer 2c, which itself is covered by the front side PSG layer 5.

Referring again to figure 4, after process 108b to create the protective layer 5a on the back surface field layer 4, the method continues with a subsequent process 104a for a removal of the PSG layer 5 from the textured front surface and a removal of the n-type doped layer 2c from the textured front surface by either a single sided etching process or a two sided etching process.

Figure 17 shows a cross-section of the solar cell after process 104a in accordance with the fourth aspect. In Figure 17 entities with the same reference number as shown in the preceding figures refer to corresponding entities.

After process 104a, the back surface 3 of the semiconductor substrate 1 is still covered by the back surface field layer 4. The back surface field layer itself is covered by the PSG layer 5. The PSG layer 5 on the back surface field layer 4 is covered by the protective layer 5a. After removal of the PSG layer 5 and the n-type doped layer 2c from the textured front surface in process 104a, the textured front surface 2 of the semiconductor substrate 1 is exposed.

Referring again to figure 4, after process 104a to remove the PSG layer 5 and the n-type doped layer 2c from the textured front surface, the method continues with a further process 109 to remove the protective layer 5a and the PSG layer 5 from the back surface field layer 4.

Figure 18 shows a cross-section of the solar cell after process 109 in accordance with the fourth aspect.

In Figure 18 entities with the same reference number as shown in the preceding figures refer to corresponding entities.

After process 109, the back surface 3 of the semiconductor substrate 1 is covered by the back surface field layer 4. The secondary textured front surface 2b is freely exposed.

Next, the method according to the fourth aspect of the invention continues with processes 106 and 107 as described above with reference to figures 1, 10 and 11.

It is noted that to obtain a back surface field BSF layer of p-type conductivity and an n-type dopant layer on the front surface, process 103 is to be carried out with p-type dopant such as boron, and process 106 is to be carried out with n-type dopant such as phosphorus.

As will be appreciated by the skilled person, due to the reversal of the conductivity types, the formation and removal of the PSG layers 5 and BSG layer 7 in the sequences as described above will be reversed and need to be adapted.

In a further embodiment, the textured front surface 2a is partly smoothened.

The partly smoothening may be done in a process step between the texturing 102 of the front surface and the creation 106 of the emitter layer on the textured front surface.

For example, the partly smoothening is done either directly after the texturing 102 of the front surface or more preferably directly preceding the creation 106 of the emitter layer on the textured front surface.

The partial smoothening may be performed by etching with a HF and/or HNO_3 containing liquid. The partial smoothening may for instance result in removing away a layer of average thickness of about 50 nm – 2 μm.

Especially, the partial smoothening may be performed by the process 104a or 105 (remove doped layer from textured front surface), where the etching agent may be arranged for minor polishing.

Advantageously, the partly smoothening may result in higher efficiency of the solar cells due to improved surface passivation of surfaces with doped layers, when the texture features on these surfaces are (even slightly) smoothened.

The partly smoothening may include a broadening of intermediate valleys between the elevated pyramidal shaped areas, with resulting valley widths between 50 and 1000 nm, especially between 50 and 500nm, or a rounding of these intermediate valleys with a curvature with a radius between 25 and 500 nm, especially between 25 and 250nm.

For the front surface the partial smoothening is preferably very light to avoid increasing reflectance by an unacceptable amount, e.g. by more than 2 or 3 percentage points at a wavelength of 1000 nm (relative to the non-smoothened textured surface).

Figure 19a shows in some more detail a front surface texture after partial smoothening; and figure 19b shows in some more detail the interpretation of valley width and curvature.

The valleys in between are rounded, and may have radii r selected from the range of about 25-500 nm, especially the range of about 25-250nm. Note that here the textured front surface 2a after partial smoothening indicated with reference 20 is schematically displayed. Figure 19b in some more detail depicts the understanding of valley width and radius. Facets (or pyramid facets) f, especially the 111 crystal facets of Si, may meet in a valley v. In non-smoothened variants, the valley v at the bottom will be very narrow, i.e. w is small, such as < 50 nm. After smoothening, the valley v may be a bit rounded, leading to a broader valley, with a width w for instance in the range of about 50-500 nm. At least part of the valley v, after smoothening, may be curved, having a radius r in for instance in the range of about 25-250 nm.

Advantageously, the method provides an enhanced manufacturing with less variation between individual solar cells. A parasitic doping (either p-type or n-type) from one surface of the silicon substrate to another surface, especially from the BSF side to the emitter side, is prevented by the method. Also, a screen printing step is omitted which reduces yield loss due to breakage. Moreover, two-sided diffusion of phosphorus in both front and back surfaces is possible, which results in an improved gettering of impurities from the silicon substrate. Additionally, the diffused back surface field layer improves the efficiency of the solar cell.

The skilled person will appreciate that alternatively, it is not needed to form PSG layer(s) or BSG layer(s) while creating the n or p type doped layer at either the back surface or the front surface, depending on the actual precursor of the dopant(s). in that case, the above mentioned process steps to remove a BSG or PSG glassy layer can be omitted.

It will be apparent to the person skilled in the art that other embodiments of the invention can be conceived and reduced to practice without departing from the true spirit of the invention, the scope of the invention being limited only by the appended

claims. The description illustrates the invention and is not intended to limit the invention.

Claims

1. A method (100; 100a; 100b; 100c) for manufacturing a solar cell from a semiconductor substrate (1) of a first conductivity type, the semiconductor substrate having a front surface (2) and a back surface (3), the method comprising in a sequence:
texturing (102) the front surface to create a textured front surface (2a);
creating (103) by diffusion of a dopant of the first conductivity type a first conductivity-type doped layer (2c) in the textured front surface and a back surface field layer (4) of the first conductivity type in the back surface;
removing (105; 104a) the first conductivity-type doped layer from the textured front surface by an etching process adapted for retaining texture of the textured front surface;
creating (106) a layer (6) of a second conductivity type on the textured front surface by diffusion of a dopant of the second conductivity type into the textured front surface.

2. The method according to claim 1, wherein texturing (102) the front surface to create a textured front surface comprises texturing the back surface to create a textured back surface (3a).

3. The method according to claim 2, wherein the creation of the back surface field layer (4)is preceded by polishing the textured back surface (3a)of the semiconductor substrate.

4. The method according to claim 1 or claim 3, comprising during the diffusion of the dopant of the first conductivity type, a formation of a dopant containing glassy layer (5) on the front surface and the back surface from a precursor of the first conductivity type, the dopant containing glassy layer acting as dopant source for the semiconductor substrate (1).

5. The method according to claim 4, comprising removing the dopant containing glassy layer (5) from the front surface and the back surface preceding the removal (105) of the first conductivity-type doped layer from the textured front surface.

6. The method according to claim 4, comprising removing (104a) the dopant containing glassy layer (5) from the front surface while removing the first conductivity-type doped layer from the textured front surface, in a single sided etching process.

7. The method according to claim 6, comprising removing (105) the dopant containing glassy layer from the back surface after the removal (104a) of the dopant containing glassy layer from the front surface and the first conductivity-type doped layer from the textured front surface in the single sided etching process.

8. The method according to claim 4, comprising preceding the removal (105) of the first conductivity-type doped layer from the textured front surface:
- removing (104b) the dopant containing glassy layer from the front surface and the back surface, and
- creating (108a) a protective layer (5a) on the back surface field layer (4).

9. The method according to claim 6, comprising:
- after creating the first conductivity-type doped layer (2c) in the textured front surface and the back surface field layer (4) of the first conductivity type in the back surface:
- creating (108a) a protective layer on the back surface field layer,
before the removal (104a) of the dopant containing glassy layer from the front surface while removing the first conductivity-type doped layer from the textured front surface in a single sided etching process.

10. The method according to claim 9, comprising: after the removal (104a) of the dopant containing glassy layer from the front surface while removing the first conductivity-type doped layer from the textured front surface in a single sided etching process and preceding the creation of the layer of the second conductivity type on the textured front surface:
- removing (109) the protective layer and the dopant containing glassy layer from the back surface

11. The method according to claim 8 or claim 10, wherein the protective layer (5a) comprises a coating layer containing at least one material selected from a group of aluminum oxide (Al_2O_3), silicon nitride (SiN_x), a dielectric, and a resist.

12. The method according to claim 1, wherein creating the back surface field layer by diffusion of the dopant of the first conductivity type comprises exposing the back surface to a precursor of the first conductivity type at elevated temperature.

13. The method according to claim 12, wherein the precursor of the first conductivity type contains the dopant of the first conductivity type; the precursor being selected

from one of a gaseous precursor, a liquid precursor, a paste precursor and a plasma precursor.

14. The method according to claim 1, wherein the diffusion of the dopant of the first conductivity type is optimized to create a thickness of the first conductivity-type doped layer (2c) in the textured front surface of 0.7 micron or less.

15. The method according to claim 1, wherein the diffusion of the dopant of the first conductivity type is optimized to create a thickness of the first conductivity-type doped layer (2c) in the textured front surface of 0.3 micron or less.

16. The method according to claim 1, wherein creating the layer of the second conductivity type on the textured front surface by diffusion of the dopant of the second conductivity type comprises exposing the textured front surface to a precursor of the second conductivity type at elevated temperature.

17. The method according to claim 16, wherein the precursor of the second conductivity type is a gaseous precursor, the gaseous precursor containing the dopant of the second conductivity type.

18. The method according to any one of the preceding claims, wherein the first conductivity type is n-type and the second conductivity type is p-type, or the first conductivity type is p-type and the second conductivity type is n-type.

19. The method according to claim 1, wherein a thickness of the first conductivity-type doped layer (2c) is less than an average height of a texture feature on the textured front surface.

20. The method according to claim 19, wherein the average height of the texture feature on the textured front surface is at least about 2 micron and the thickness of the first conductivity type doped layer is about 0.7 micron or less.

21. The method according to claim 19, wherein the average height of the texture feature on the textured front surface is at least about 2 micron and the thickness of the first conductivity type doped layer is about 0.3 micron or less.

22. The method according to claim 1, wherein the etching process adapted for retaining texture of the textured front surface is performed by a single-sided wet-chemical process using an etching agent.

23. The method according to claim 22, wherein the etching agent comprises a component for texturing a semiconductor surface.

24. The method according to claim 23, wherein the etching agent further comprises a component for polishing the semiconductor surface.

25. The method according to claim 1, wherein the etching process adapted for retaining texture of the textured front surface is performed by a dry etching method.

26. The method according to claim 1, wherein the removing of the first conductivity type doped layer from the textured front side and the dopant containing glassy layer from the front surface is performed during the etching process adapted for retaining texture of the textured front surface.

27. The method according to claim 1, further comprising partly smoothening the textured front surface.

28. The method according to claim 27, wherein the partial smoothening includes at least one of a broadening and a rounding of intermediate valleys between pyramidal shapes of the textured front surface.

29. A solar cell comprising a semiconductor substrate of a first conductivity type having a textured front surface and a back surface, wherein the textured front surface comprises a second conductivity-type doped layer, wherein the back surface comprises a surface field layer of the first conductivity type.

30. The solar cell according to claim 29, wherein the textured front surface comprises a pyramidal shapes containing front surface with intermediate valleys having widths selected from the range of 50-500 nm.

31. The solar cell according to claim 29, the textured front surface having valleys with curvatures having radii selected from the range of 25-250 nm.