

A METHOD FOR PHOTOLITHOGRAPHY-FREE SELF-ALIGNED REVERSE ACTIVE ETCH

TECHNICAL FIELD

The present disclosure relates to fabrication of semiconductor integrated circuits, and
5 more particularly, to a method of fabricating semiconductor integrated circuits using
photolithography-free self-aligned reverse active etch.

BACKGROUND

There are inherent problems in trying to align a reverse active etch photomask to the
already patterned active shallow trench isolation (STI). Because of small variations and
10 errors in the lithographic process, there is a built-in overlap. In addition to the lithographic
margin, the typical high density plasma (HDP) oxide fill at this process step is sloped due to
the nature of the HDP oxide process. This slope forces a certain amount of overlap to prevent
printing the photo-resist on the angled portion of the HDP fill.

SUMMARY

15 Therefore, what is needed is an improved way to perform accurate reverse-active etch
patterning without the use of photolithography.

According to an aspect, there is provided a method for photolithography-free self-
aligned reverse active etch of a semiconductor wafer, said method comprising the steps of:
depositing a pad oxide on a silicon substrate of a semiconductor wafer; depositing an active
20 silicon nitride on the pad oxide; forming shallow trench isolation (STI) wells in the silicon
substrate; forming an oxidization liner in the STI wells, wherein the oxidization liner is only
formed where the silicon substrate is exposed; depositing an oxide over the silicon nitride and
the STI wells; depositing a partially planarized organosilicate (DUO) layer over the oxide;
performing a dry plasma etch to remove the partially planarized organosilicate layer from the
25 oxide by first non-selective etching thereby removing some of the partially planarized
organosilicate layer and some of the oxide and then selectively etching the oxide thereby only
removing the oxide, wherein the oxide above the silicon nitride is removed to a predefined
thickness; performing a chemical-mechanical polish (CMP) to remove all of the oxide
covering the active silicon nitride; and removing the active silicon nitride, wherein portions
30 of the silicon substrate are exposed between the remaining oxide and ready for the step of
active transistor element doping in the silicon substrate.

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According to an embodiment of the method, the pad oxide may be silicon oxide. According to a further embodiment of the method, the step of forming STI wells may comprise the step of etching the silicon substrate to form the STI wells. According to a

further embodiment of the method, the oxidization liner may be silicon oxide. According to a further embodiment of the method, the step of depositing an oxide over the oxidation liner may comprise the step of depositing a high density plasma (HDP) oxide over the oxidation liner. According to a further embodiment of the method, the step of depositing the DUO layer over the oxide may comprise the step of spin-coating the DUO layer onto the oxide. According to a further embodiment of the method, the step of removing the DUO layer from the oxide may comprise the steps of doing a tuned etch to open the DUO layer, and etching a short selective etch to the DUO layer, wherein the semiconductor wafer may be etched in an oxide etcher. According to a further embodiment of the method, the step of removing the DUO layer from the oxide may comprise the steps of multiple dry plasma etching. According to a further embodiment of the method, the steps of multiple dry plasma etching may comprise the steps of etching non-selective to oxide and etching partial to oxide. According to a further embodiment of the method, the step of etching non-selective to oxide may use gases selected from the group consisting of CF_4 , O_2 , and Ar. According to a further embodiment of the method, the step of etching partial to oxide may use gases selected from the group consisting of C_5F_8 , O_2 , N_2 , and Ar. According to a further embodiment of the method, the step of removing the DUO layer from the oxide may be performed until the step of performing the dry plasma etch may be completed.

There is also disclosed a semiconductor integrated circuit prepared by a process comprising the steps of: depositing a pad oxide on a silicon substrate of a semiconductor wafer; depositing an active silicon nitride on the pad oxide; forming shallow trench isolation (STI) wells in the silicon substrate; forming an oxidization liner in the STI wells, wherein the oxidization liner is only formed where the silicon substrate is exposed; depositing an oxide over the silicon nitride and the STI wells; depositing a partially planarized organosilicate (DUO) layer over the oxide; performing a dry plasma etch to remove the DUO layer from the oxide; performing a chemical-mechanical polish (CMP) to remove all of the oxide covering the active silicon nitride; and removing the active silicon nitride, wherein portions of the silicon substrate are exposed between the remaining oxide and ready for the step of active transistor element doping in the silicon substrate.

According to an embodiment of the process, the step of depositing an oxide over the oxidation liner may comprise the step of depositing a high density plasma (HDP)

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oxide over the oxidation liner. According to a further embodiment of the process, the step of

removing the DUO layer from the oxide may comprise the steps of doing a tuned etch to open the DUO layer, and etching a short selective etch to the DUO layer, wherein the semiconductor wafer may be etched in an oxide etcher. According to a further embodiment of the process, the step of removing the DUO layer from the oxide may comprise the steps of multiple-step dry plasma etching. According to a further embodiment of the process, the steps of multiple-step dry plasma etching may comprise the steps of etching non-selective to oxide and etching partial to oxide. According to a further embodiment of the process, the step of etching non-selective to oxide may use gases selected from the group consisting of CF₄, O₂, and Ar. According to a further embodiment of the process, the step of etching partial to oxide may use gases selected from the group consisting of C₅F₈, O₂, N₂, and Ar.

There is disclosed a semiconductor wafer having a surface treated in accordance with the steps of: depositing a pad oxide on a silicon substrate of a semiconductor wafer; depositing an active silicon nitride on the pad oxide; forming shallow trench isolation (STI) wells in the silicon substrate; forming an oxidization liner in the STI wells, wherein the oxidization liner is only formed where the silicon substrate is exposed; depositing an oxide over the silicon nitride and the STI wells; depositing a partially planarized organosilicate (DUO) layer over the oxide; performing a dry plasma etch to remove the DUO layer from the oxide; performing a chemical-mechanical polish (CMP) to remove all of the oxide covering the active silicon nitride; and removing the active silicon nitride, wherein portions of the silicon substrate are exposed between the remaining oxide and ready for the step of active transistor element doping in the silicon substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present disclosure may be acquired by referring to the following description taken in conjunction with the accompanying drawings wherein:

Figure 1 illustrates a schematic flow diagram of prior art process fabrication steps used to form field oxides and expose a silicon substrate for further processing of active transistor element doping in the silicon substrate;

CLAIMS

1. A method for photolithography-free self-aligned reverse active etch of a semiconductor wafer, said method comprising the steps of:

5 depositing a pad oxide on a silicon substrate of a semiconductor wafer;
 depositing an active silicon nitride on the pad oxide;
 forming shallow trench isolation (STI) wells in the silicon substrate;
 forming an oxidization liner in the STI wells, wherein the oxidization liner is
only formed where the silicon substrate is exposed;
10 depositing an oxide over the silicon nitride and the STI wells;
 depositing a partially planarized organosilicate layer over the oxide;
 performing a dry plasma etch to remove the partially planarized organosilicate
layer from the oxide by first non-selective etching thereby removing some of the
partially planarized organosilicate layer and some of the oxide and then selectively
15 etching the oxide thereby only removing the oxide, wherein the oxide above the
silicon nitride is removed to a predefined thickness;
 performing a chemical-mechanical polish (CMP) to remove all of the oxide
covering the active silicon nitride; and
 removing the active silicon nitride, wherein portions of the silicon substrate
20 are exposed between the remaining oxide and ready for the step of active transistor
element doping in the silicon substrate.

2. The method according to claim 1, wherein the pad oxide is silicon oxide.

3. The method according to claim 1 or 2, wherein the step of forming STI wells
comprises the step of etching the silicon substrate to form the STI wells.

25 4. The method according to any one of the preceding claims, wherein the
oxidization liner is silicon oxide.

5. The method according to any one of the preceding claims, wherein the step of
depositing an oxide over the oxidation liner comprises the step of depositing a high density
plasma (HDP) oxide over the oxidation liner.

6. The method according to any one of the preceding claims, wherein the step of depositing the partially planarized organosilicate layer over the oxide comprises the step of spin-coating the partially planarized organosilicate layer onto the oxide.

7. The method according to claim 6, wherein the step of spin-coating comprises
5 even spin-on-glass.

8. The method according to any one of the preceding claims, wherein the step of performing the dry plasma etch comprises the steps of doing a tuned etch to open the partially planarized organosilicate layer above the silicon nitride, and etching a short selective etch removing only the HDP oxide layer, wherein the semiconductor wafer is etched in an oxide etcher.

9. The method according to any one of the preceding claims, wherein the step of non-selective etching uses gases selected from the group consisting of CF_4 , O_2 , and Ar.

10. The method according to any one of the preceding claims, wherein the step of selectively etching partial to oxide uses gases selected from the group consisting of C_5F_8 , O_2 , N_2 , and Ar.

11. The method according to one of the preceding claims, wherein after performing the dry plasma etch and before performing the CMP, remaining partially planarized organosilicate is stripped off.

12. The method according to claim 11, comprising the step of performing an oxidizing ash to strip off the remaining partially planarized organosilicate.

13. The method according to claim 11, comprising the step of performing an HF strip to strip off the remaining partially planarized organosilicate.