**WHAT IS CLAIMED IS:**

1. An integrated circuit comprising:

a digital logic circuit having a plurality of inputs, wherein the digital logic circuit comprises a plurality of logic gates; and

a first polarization circuit configured to receive a standby signal and a digital input signal comprising a plurality of bits, wherein when the standby signal is deactivated, the first polarization circuit is configured to control the plurality of inputs of the digital logic circuit based on the digital input signal, and wherein when the standby signal is activated the first polarization circuit is configured to control the plurality of inputs of the digital logic circuit to a low power state associated with a smaller leakage current of the plurality of logic gates relative to at least one other state of the digital logic circuit.

2. The integrated circuit of Claim 1, wherein the low power state is associated with the smallest leakage current of the plurality of logic gates relative to all other states of the digital logic circuit.

3. The integrated circuit of any of Claims 1 or 2, wherein the plurality of logic gates comprises a plurality of standard cells.

4. The integrated circuit of any of Claims 1 to 3, wherein when the standby signal is activated, the first polarization circuit is configured to control the plurality of inputs of the digital logic circuit by buffering the digital input signal.

5. The integrated circuit of any of Claims 1 to 3, wherein when the standby signal is activated, the first polarization circuit is configured to control the plurality of inputs of the digital logic circuit by inverting the digital input signal.

6. The integrated circuit of any of Claims 1 to 5, further comprising a first plurality of state elements configured to generate the digital input signal.

7. The integrated circuit of Claim 6, wherein a circuit layout of the first polarization circuit is integrated within a circuit layout of the first plurality of state elements.

8. The integrated circuit of Claim 6, wherein the first plurality of state elements comprise a plurality of flip-flops.

9. The integrated circuit of Claim 6, further comprising a second plurality of state elements configured to receive a digital output signal from the digital logic circuit.

10. The integrated circuit of Claim 9, wherein the second plurality of state elements are configured to load a value of the digital output signal in response to a transition of a clock signal, and wherein the clock signal is inhibited from transitioning when the standby signal is deactivated.

11. The integrated circuit of any of Claims 1 to 10, wherein the digital logic circuit comprises a combinational logic circuit.

12. The integrated circuit of Claim 11, wherein the digital logic circuit does not include any state elements.

13. The integrated circuit of any of Claims 1 to 12, wherein the first polarization circuit comprises a plurality of logic gates having a first input configured to receive the standby signal and a second input, wherein each second input of the plurality of logic gates of the first polarization circuit receives a different bit of the digital input signal.

14. The integrated circuit of Claim 13, wherein the plurality of logic gates of the first polarization circuit comprises at least one gate configured to generate a polarization bit based on a logical AND operation of a bit of the digital input signal and a logically inverted version of the standby signal.

15. The integrated circuit of Claim 13, wherein the plurality of logic gates of the first polarization circuit comprises at least one gate configured to generate a polarization bit based on a logical OR operation of a bit of the digital input signal and the standby signal.

16. The integrated circuit of any of Claims 1 to 15, wherein the digital logic circuit comprises two or more digital logic subcircuits including a first digital logic subcircuit and a second digital logic subcircuit, wherein the first polarization circuit is configured to control a plurality of inputs of the first digital logic subcircuit, and wherein a second polarization circuit is configured to control a plurality of inputs of the second digital logic subcircuit.

17. The integrated circuit of any of Claims 1 to 16, wherein the digital logic circuit comprises a subcircuit of a larger digital circuit.

18. An electronically-implemented method of leakage reduction in a digital circuit, the method comprising:

receiving a standby signal into a polarization circuit;

receiving a digital input signal into the polarization circuit;

controlling a plurality of inputs of a digital logic circuit based on the digital input signal using the polarization circuit when the standby signal is deactivated, the digital logic circuit comprising a plurality of logic gates; and

controlling the plurality of inputs of the digital logic circuit to a low power state using the polarization circuit when the standby signal is activated, wherein the low power state is associated with a smaller leakage current of the plurality of logic gates relative to at least one other state of the digital logic circuit.

19. The method of Claim 18, wherein controlling the plurality of inputs of the digital logic circuit to the low power state comprises controlling the plurality of inputs of the digital logic circuit to a state associated with the smallest leakage current of the plurality of logic gates relative to all other states of the digital logic circuit.

20. The method of Claims 18 or 19, wherein controlling the plurality of inputs of the digital logic circuit based on the digital input signal comprises buffering the digital input signal.

21. The method of Claims 18 or 19, wherein controlling the plurality of inputs of the digital logic circuit based on the digital input signal comprises inverting the digital input signal.

22. The method of any of Claims 18 to 21, wherein the digital logic circuit comprises a combinational logic circuit.

23. The method of any of Claims 18 to 22, further comprising generating a digital output signal using the digital logic circuit and providing the digital output signal to a plurality of state elements.

24. The method of Claim 23, further comprising inhibiting the plurality of state elements from loading a value of the digital output signal when the standby signal is activated.

25. A method of integrated circuit (IC) design, the method comprising:

designing the IC to include a first digital logic circuit having a plurality of inputs and including a plurality of digital logic gates;

determining leakage current data of the first digital logic circuit, wherein the leakage current data indicates a leakage current of the first digital logic circuit for each state of the inputs, wherein the leakage current data is determined at least in part by simulating the first digital logic circuit;

selecting a low power state of the first digital logic circuit based on the leakage current data, wherein the low power state is associated with a smaller leakage current of the plurality of logic gates relative to at least one other state of the first digital logic circuit; and

designing the IC to include a first polarization circuit to control the inputs of the first digital logic circuit, wherein the first polarization circuit is operable to control the first digital logic circuit to the low power state when the IC is in a standby mode.

26. The method of Claim 25, further comprising:

designing the IC to include a plurality of flip-flops, wherein designing the IC to include the first polarization circuit comprises implementing a first portion of the plurality of flip-flops using a first type of flip-flop and implementing a second portion of the plurality of flip-flops using a second type of flip-flop, wherein the first type of flip-flop outputs a logical "1" in the standby mode, and wherein the second type of flip-flop outputs a logical "0" in the standby mode.

27. The method of Claims 25 or 26, further comprising:

designing the IC to include a second digital logic circuit; and

omitting a second polarization circuit to control the inputs of the second digital logic circuit when the second digital logic circuit controls an input of a sensitive circuit, wherein a change of a value of the input of the sensitive circuit disturbs the functionality of the IC.

28. The method of Claims 25 or 26, further comprising:

designing the IC to include a second digital logic circuit;

determining a leakage current overhead associated with including a second polarization circuit to control the inputs of the second digital logic circuit;

determining a leakage current savings associated with including the second polarization circuit to control the inputs of the second digital logic circuit; and

designing the IC to include the second polarization circuit when the leakage current overhead is less than the leakage current savings.

29. The method of any of Claims 25 to 28, wherein determining leakage current data of the first digital logic circuit comprises simulating the first digital logic circuit using a circuit simulator.

30. The method of any of Claims 25 to 29, further comprising:

designing the first polarization circuit of the IC to control the inputs of the first digital logic circuit based on a digital input signal when the IC is not in the standby mode.

31. The method of any of Claims 25 to 30, wherein selecting a low power state of the first digital logic circuit comprises selecting a state of the first digital logic circuit having the smallest leakage current of the plurality of logic gates relative to all other states of the first digital logic circuit.

**WHAT IS CLAIMED IS:**

1. An integrated circuit comprising:

a digital logic circuit having a plurality of inputs, wherein the digital logic circuit comprises a plurality of logic gates;

a first polarization circuit configured to receive a standby signal and a digital input signal comprising a plurality of bits, wherein when the standby signal is deactivated, the first polarization circuit is configured to control the plurality of inputs of the digital logic circuit based on the digital input signal, and wherein when the standby signal is activated the first polarization circuit is configured to control the plurality of inputs of the digital logic circuit to a low power state associated with a smaller leakage current of the plurality of logic gates relative to at least one other state of the digital logic circuit; and

a first plurality of state elements, wherein the digital logic circuit is configured to generate a digital output signal and to provide the digital output signal to the first plurality of state elements,

wherein the integrated circuit is configured such that the first plurality of state elements are inhibited from loading a value of the digital output signal when the standby signal is activated.

2. The integrated circuit of Claim 1, wherein the low power state is associated with the smallest leakage current of the plurality of logic gates relative to all other states of the digital logic circuit.

3. The integrated circuit of Claim 1, wherein the plurality of logic gates comprises a plurality of standard cells.

4. The integrated circuit of Claim 1, wherein when the standby signal is deactivated, the first polarization circuit is configured to control the plurality of inputs of the digital logic circuit by buffering the digital input signal.

5. The integrated circuit of Claim 1, wherein when the standby signal is deactivated, the first polarization circuit is configured to control the plurality of inputs of the digital logic circuit by inverting the digital input signal.

6. The integrated circuit of Claim 1, further comprising a second plurality of state elements configured to generate the digital input signal.

7. The integrated circuit of Claim 6, wherein a circuit layout of the first polarization circuit is integrated within a circuit layout of the second plurality of state elements.

8. The integrated circuit of Claim 6, wherein the second plurality of state elements comprise a plurality of flip flops.

9. The integrated circuit of Claim 1, wherein the digital logic circuit comprises a combinational logic circuit.

10. The integrated circuit of Claim 9, wherein the digital logic circuit does not include any state elements.

11. The integrated circuit of Claim 1, wherein the first polarization circuit comprises a plurality of logic gates having a first input configured to receive the standby signal and a second input, wherein each second input of the plurality of logic gates of the first polarization circuit receives a different bit of the digital input signal.

12. The integrated circuit of Claim 11, wherein the plurality of logic gates of the first polarization circuit comprises at least one gate configured to generate a polarization bit based on a logical AND operation of a bit of the digital input signal and a logically inverted version of the standby signal.

13. The integrated circuit of Claim 11, wherein the plurality of logic gates of the first polarization circuit comprises at least one gate configured to generate a polarization bit based on a logical OR operation of a bit of the digital input signal and the standby signal.

14. The integrated circuit of Claim 1, wherein the digital logic circuit comprises two or more digital logic subcircuits including a first digital logic subcircuit and a second digital logic subcircuit, wherein the first polarization circuit is configured to control a plurality of inputs of the first digital logic subcircuit, and wherein a second polarization circuit is configured to control a plurality of inputs of the second digital logic subcircuit.

15. The integrated circuit of Claim 1, wherein the digital logic circuit comprises a subcircuit of a larger digital circuit.

16. An electronically-implemented method of leakage reduction in a digital circuit, the method comprising:

receiving a standby signal into a polarization circuit;

receiving a digital input signal into the polarization circuit;

controlling a plurality of inputs of a digital logic circuit based on the digital input signal using the polarization circuit when the standby signal is deactivated, the digital logic circuit comprising a plurality of logic gates;

controlling the plurality of inputs of the digital logic circuit to a low power state using the polarization circuit when the standby signal is activated, wherein the low power state is associated with a smaller leakage current of the plurality of logic gates relative to at least one other state of the digital logic circuit;

generating a digital output signal using the digital logic circuit and providing the digital output signal to a plurality of state elements; and

inhibiting the plurality of state elements from loading a value of the digital output signal when the standby signal is activated.

17. The method of Claim 16, wherein controlling the plurality of inputs of the digital logic circuit to the low power state comprises controlling the plurality of inputs of the

digital logic circuit to a state associated with the smallest leakage current of the plurality of logic gates relative to all other states of the digital logic circuit.

18. The method of Claim 16, wherein controlling the plurality of inputs of the digital logic circuit based on the digital input signal comprises buffering the digital input signal.

19. The method of Claim 16, wherein controlling the plurality of inputs of the digital logic circuit based on the digital input signal comprises inverting the digital input signal.

20. The method of Claim 16, wherein the digital logic circuit comprises a combinational logic circuit.