

Description

The invention relates to an arrangement for reducing the power consumption in a television circuit during a period when such circuit is not required to perform at least some of its functions.

A television receiver, for example, may include a pulse-width modulator or voltage regulator that generates a pulse-width modulated control signal at a horizontal related frequency. The control signal controls a run power supply that supplies run supply voltage such as a regulated B+ supply voltage. The B+ supply voltage energizes a horizontal output stage during a power-up mode. The voltage regulator circuitry may be combined with a horizontal deflection circuitry and incorporated in an integrated circuit (IC) that is referred to herein as the deflection IC. The horizontal drive circuitry generates a horizontal drive signal that is coupled to a horizontal output stage. The deflection IC may be required to operate selectively in a power-up mode and in a standby mode in accordance with an on/off control signal provided by a remote receiver in the power-up mode. Such pulse-width voltage regulator may be required to supply the pulse-width modulated control signal for controlling the run power supply that generates the regulated B+ supply voltage used for operating deflection circuitry of a horizontal output stage of the receiver. When operation in a standby mode is required, such control signal may be required to prevent the power supply from energizing the deflection circuitry until such time as a user initiates a power-up command via the remote receiver that causes a start-up interval to begin.

A first portion of the deflection IC that includes, for example, the main voltage regulator and the horizontal deflection circuitry may be required to be energized during the power-up mode and during a start-up interval but may not need to be energized during the standby mode. On the other hand, the deflection IC may include a second portion, such as a shunt regulator internal to the IC, for example, that is required to be energized during both the power-up and the standby modes.

In one prior art circuit as disclosed in US-A-4,500,923, a shunt switch is coupled between ground and a supply voltage receiving terminal of the deflection IC that receives an energizing voltage that supplies the entire power requirements of the deflection IC. During operation in the standby mode, the shunt switch that is controlled by the on/off control signal develops a low impedance between the terminal and a common conductor such as ground that reduces the energizing voltage to approximately zero volts that disables the deflection IC. Disadvantageously, such shunt switch, when conductive, causes a substantial power dis-

sipation.

The remote receiver, for example, may be energized, during both the power-up mode and the standby mode, by a separate standby power supply. The standby power supply may include a standby transformer having a primary winding that is coupled to an alternating current (AC) mains supply source. A voltage that is developed at a secondary winding of the transformer may be rectified to produce a DC standby energizing voltage.

The standby energizing voltage and a run supply voltage of the run power supply may be selectively applied to a supply voltage receiving terminal of the deflection IC to form an energizing voltage at such terminal that energizes the deflection IC. The standby energizing voltage energizes those portions of the deflection IC that are required to be energized during the standby mode and during the start-up interval; whereas during the power-up mode, the run-mode power supply provides the entire or principal energizing voltage to the terminal of the deflection IC.

It may be desirable to reduce the supply current that is required from the standby transformer so as to reduce the cost of such transformer. To this end, it may be desirable to reduce the current consumption of the deflection IC during the standby mode.

In accordance with an aspect of the invention, during the standby mode, the on/off control signal provided by the remote receiver is coupled to the deflection IC to cause a reduction of energizing current consumption that is supplied by the standby power supply. Without the operation of the on/off control signal, current that is supplied by the standby power supply would flow in the first portion of the deflection IC that need not be energized during the standby mode.

In carrying out a feature of the invention, the deflection IC receives its energizing voltage at the same terminal during both the power-up mode and the standby mode. Such arrangement advantageously simplifies the construction and design of the deflection IC, for example, by reducing the number of external connections, and also, interconnection between the deflection IC and other television circuitry within the television receiver.

In carrying out another aspect of the invention, reducing the energizing or supply current of the deflection IC is accomplished by applying the on/off control signal during the standby mode to corresponding control electrodes of predetermined selected stages of the deflection IC. Such selected stages are required to be active only during the normal operation power-up mode. In this way, the energizing current in the deflection IC during the standby mode is reduced. The energizing current consumption is reduced, advantageously, by re-

ducing during the standby mode the quiescent current in each corresponding stage in accordance with the on/off control signal.

In accordance with a further aspect of the invention, the quiescent current in a given stage of the deflection IC is temperature compensated in accordance with a temperature compensated control signal, during the power-up mode. However, during the standby mode, the temperature compensated control signal is at a second level that switches off the quiescent current in the given stage.

A deflection circuit of a television apparatus embodying the invention produces a deflection current in a deflection winding during operation in a power-up mode. A source of a first supply voltage is developed during operation of the television apparatus in each of the power-up and in a standby mode. A control circuit is coupled to the deflection circuit for controlling the operation of the deflection circuit during operation in the power-up mode and for preventing the production of the deflection current during operation in the standby mode. The control circuit includes at least a first circuit stage that is coupled, during operation in each of the power-up and standby modes, to the source of the first supply voltage to form a current path. A first portion of a supply current flows in the current path from the source of the first supply voltage during operation in the power-up mode. A source of an on/off control signal that is selectively indicative of operation of said television apparatus in the power-up mode and in the standby mode is used for generating a second control signal during television apparatus operation in the power-up mode. The second control signal is applied to the first circuit stage to control the first portion of the supply current. During operation of the television apparatus in the standby mode, the second control signal causes the first portion of the supply current that flows in the first circuit stage to be reduced.

In the Drawing:

FIGURE 1, that includes portions 1A and 1B, illustrates a television power supply including a deflection IC embodying the invention; and FIGURES 2a-2b illustrate waveforms useful for explaining the operation of the deflection IC of FIGURE 1 during the start-up interval.

FIGURE 1 illustrates a portion of a television receiver incorporating a deflection IC 100, embodying the invention. Such portion of the television receiver includes a bridge rectifier 101 that rectifies a mains supply voltage V_{AC} to produce a DC, unregulated voltage V_{UR} . A conventional power supply output stage or switch regulator 102, that may include a silicon controlled rectifier (SCR) produces during a normal operation power-up mode a regulated voltage $B+$ that is coupled to a

flyback transformer T1. An input supply terminal 102c of regulator 102 is coupled to unregulated voltage V_{UR} . Regulated voltage $B+$ is developed at an output terminal 102d of switch regulator 102. Transformer T1 is coupled to a collector electrode of a deflection switching transistor Q1 of a horizontal circuit output stage 99 operating at a horizontal rate f_H . A control signal H_r , at the horizontal rate f_H , that is produced in a corresponding portion of deflection IC 100, referred to herein as a horizontal processor 100a (Fig. 1B), is coupled via a horizontal driver 666 to the base electrode of transistor Q1. The frequency of signal H_r is determined by a horizontal oscillator, not shown in the FIGURES, that may be included in IC 100. Signal H_r controls the switching of transistor Q1 to generate a deflection current i_y in a deflection winding L_y of output stage 99. A retrace voltage V_{w2} is produced in a conventional manner across a winding W2 of transformer T1 in each retrace interval of each horizontal period H. A second retrace voltage H_{in} in a winding W3 of transformer T1 that is coupled to horizontal processor 100a is used in synchronizing deflection current i_y to a synchronizing signal H_s . Signal H_s is generated in a sync separator, not shown in the FIGURES.

A run supply voltage $V+$ is produced by rectifying voltage V_{w2} in a rectifier arrangement 104 that is coupled to winding W2. DC Voltage $V+$ is coupled to a corresponding portion of deflection IC 100, that is referred to herein as switch mode regulator processor 100b, to provide a feedback signal V_{IN} . Processor 100b generates a pulse width modulated signal S_c that controls the duration, in each horizontal interval H, in which switch regulator 102 is conductive. The duty cycle of signal S_c varies, in accordance with a difference between the feedback signal, that is proportional to voltage $V+$, and a reference voltage V_{NIN} that may be produced in a conventional manner. Signal S_c causes regulated voltage $B+$ to be at a predetermined DC voltage level such as, illustratively, +125 volts. Signal S_c , voltage $B+$ and voltage $V+$ are produced, illustratively, when deflection IC 100 operates in the power-up mode but are not produced during television receiver standby mode operation.

Voltage $V+$ is coupled to a voltage divider 605 that includes series coupled resistors 601, 604 and 602. Resistor 604 includes a wiper k for developing a voltage that is representative of, for example, voltage $B+$. The voltage at wiper k, that is adjustable by varying the position of wiper k, is coupled to an inverting input terminal 608 of an error amplifier 610 via a resistor 607.

An integrating lowpass filter, not shown in FIGURE 1, is coupled between inverting input terminal 608 and an output terminal 610a of amplifier 610 to provide the loop filter of regulator processor 100b.

A filtered error voltage V_0 , developed at terminal 610a, is coupled to a pulse width modulator 100b- (1), that produces pulse width modulated signal S_c . Signal S_c is coupled to a control terminal 102a of switch regulator 102 to turn on a pass switch 102b for a duration, in each period H, that varies in accordance with the duty cycle of signal S_c . The duration, during each horizontal period H, in which switch 102b conducts, that is controlled by signal S_c is determined by the level of error voltage V_0 of error amplifier 610. Thus, the level of each of regulated voltages B+ and V+ is determined by a reference voltage V_{NIN} that is produced in a conventional manner, not shown in the FIGURES.

A standby transformer T0 steps down voltage V_{AC} . The stepped down voltage is rectified in a rectifier arrangement 106 to produce a standby voltage V_{SB} . Standby voltage V_{SB} is coupled to an energizing voltage receiving terminal 120 of deflection IC 100 through a resistor R1 that charges a capacitor 66, during, for example, the standby mode operation, to produce in capacitor 66 an energizing voltage V_{cc} at terminal 120 of deflection IC 100. Regulated voltage V+ is coupled to terminal 120 via a diode D2 and resistor 150 to supply voltage V_{cc} from voltage V+ when deflection IC 100 operates in the power-up mode but not when the standby mode operation occurs.

Standby voltage V_{SB} is coupled to a remote receiver 107 to provide the operating voltage of remote receiver 107. Remote receiver 107 is coupled via an MOS transistor 108 to IC 100. When transistor 108 is conductive, a low impedance is formed between a junction terminal 109 of a resistor R734 and ground. The low impedance occurs after, for example, a user initiates a power-on command via an infra-red communication link that causes a start-up interval to occur, as described later on.

In the power-up mode that follows the start-up interval, the television receiver is fully operative. Conversely, after a power-off command is initiated by the user, transistor 108 becomes nonconductive and forms a high impedance circuit at terminal 109 that causes a standby mode to occur. In the standby mode the raster scanning on a display device of the television receiver is turned-off.

A transistor Q705, operating as a constant current source, has its collector coupled to junction terminal 109. As a result of the operation of transistors Q705 and 108, an on/off signal 110 is developed. Signal 110 is at a high level, or a second state, when transistor 108 is nonconductive, that corresponds to operation in the standby off-mode, and at a low level, or a first state, when it is conductive, that corresponds with operation in the power-up on-mode.

An input supply current i_{PS} is coupled through terminal 120 to deflection IC 100 for providing the energizing current of deflection IC 100. During operation in the power-up mode, current i_{PS} is supplied mainly by rectifier arrangement 104 through diodes D2 and D4; whereas, during operation in the standby mode, current i_{PS} is supplied from standby transformer 106 via rectifier arrangement 106 and resistor R1.

Voltage V_{cc} is regulated in deflection IC 100 by a shunt regulator 131 that may be required to regulate voltage V_{cc} during operation in both the standby mode and the power-up mode. Regulation of voltage V_{cc} during the standby mode may be desirable for protecting deflection IC 100 from an overvoltage condition at terminal 120 that may occur should voltage V_{cc} exceed the voltage rating of deflection IC 100. If permitted to occur, such overvoltage condition may damage deflection IC 100. Also regulation of voltage V_{cc} during the standby mode may be desirable for operating circuitry in deflection IC 100 that may be required to operate during the standby mode such as, for example, transistor Q705. Shunt regulator 131 regulates voltage V_{cc} in accordance with a reference voltage V_{BG2} that is generated during both the power-up and standby modes. Voltage V_{BG2} is generated in, for example, a bandgap type voltage source 105 that is, therefore, required to operate during both the standby and the power-up modes.

Deflection IC 100 includes various circuit portions that, unlike shunt regulator 131 and bandgap voltage source 105, need not be energized during operation in the standby mode. For example, each of horizontal processor 100a and regulator processor 100b need not be energized during operation in the standby mode.

Reducing the level of current i_{PS} that is supplied from standby transformer T0 during the standby mode and the start-up interval is desirable in order to relax the specifications of transformer T0 so as to reduce its cost. Such cost is related to the current requirement imposed on transformer T0 that is directly related to current i_{PS} . By coupling standby voltage V_{SB} to capacitor 66 via resistor R1, that is relatively large, the current supplied by transformer T0 is maintained low during both standby and start-up.

A circuit portion of deflection IC 100, that does not have to be energized during the standby mode, may include a first plurality of transistors. Such arrangement is depicted by transistors 90a-90n of the P-N-P type. Each such transistor may be arranged in a common base configuration to form at the collector of such transistor a current source having a high output impedance. Each of transistors 90a-90n has its base electrode coupled to a common conductor that is referred to as PNP bus

11. It should be understood that some of transistors 90a-90n may be included in, for example, horizontal driver 100a and some others in regulator processor 100b.

Transistor 90f, for example, illustrates one typical example of a circuit stage that is formed by a corresponding one of transistors 90a-90n. In such stage, a collector current i_{90f} is coupled to circuitry that is symbolically referred to as load circuit 90f1. A second typical example is shown in the arrangement of amplifier 610 that is included in regulator processor 100b. Amplifier 610 of FIGURE 1 forms a differential amplifier in which transistor 90n provides a current i_{90n} that is coupled to the emitters of transistors 90n2 and 90n3 of differential amplifier 610. Output voltage V_o of FIGURES 1 and 2 is developed at the collector of transistor 90n3 of FIGURE 1.

The collector current in each of transistors 90a-90n is controlled by a voltage V_{BR} that is coupled, via PNP bus 11, to the corresponding base electrode of each of transistors 90a-90n and that is generated by a temperature compensated current control arrangement 300. The emitter electrodes of the above-mentioned transistors 90a-90n are coupled through corresponding resistors to supply voltage V_{cc} that is, as described before, a fixed DC voltage. Because of such arrangement, the collector currents in each of transistors 90a-90n track each other over a wide range of temperature to form a current mirror arrangement. Current control arrangement 300 controls voltage V_{BR} in such a way that the collector current in each of transistors 90a-90n stays substantially constant when the temperature changes.

Current control arrangement 300 includes transistors 90a, 90b, 73, 76, 77 and 80. The collector of transistor 73 is grounded. The collector of transistor 90a is coupled to the base of transistor 73 and, at a terminal 300c, to the collectors of transistors 76 and 77. The emitter of transistor 77 is coupled to a terminal 300a via a resistor R61. The emitter of transistor 76 is coupled to the base of transistor 77, to the base of transistor 80 and, via a resistor R60, to terminal 300a. Transistor 80 is arranged in a common emitter configuration. The base of transistor 76 is coupled, at a terminal 300b, to the collectors of both transistor 80 and 90b. The emitter of transistor 80 is coupled to terminal 300a. Transistors 76, 77 and 80 form a temperature compensating feedback network that controls via transistor 73 voltage V_{BR} and maintains constant currents i_{90a} and i_{90b} in respective transistor 90a and 90b.

Transistor 76 forms, with transistor 80, a feedback arrangement that causes a collector current i_{90b} of transistor 90b to flow also as a collector current in transistor 80, by developing the corresponding base-emitter voltage in transistor 80

and across resistor R60. As described later on, current i_{90b} is maintained constant over a wide range of temperatures.

When the temperature is constant, this feedback action tends to maintain a substantially constant current flow through resistor R60 and thus a corresponding constant current through the collector-emitter junctions of each of transistors 76 and 80. As the temperature varies, the base-emitter forward voltage of transistor 80 also varies.

In order to compensate for the variation of the base-emitter forward voltage of transistor 80 so as to insure corresponding constant currents through each of terminals 300c and 300a, transistor 77 is coupled with its base to sensing resistor R60. The current in resistor R60 is proportional to the voltage across the base-emitter junction of transistor 80 that varies inversely with temperature. Whereas, for a given voltage across resistor R60, the voltage across resistor R61 that determines the collector current in transistor 77 varies directly with the temperature. Thus, variations of the base-emitter forward voltages of transistors 77 and 80 have opposite effects on the sum of the currents in resistors R60 and R61 that causes, via a feedback arrangement, a collector current i_{90a} in transistor 90a to be substantially constant when the temperature varies.

An example of an arrangement that provides temperature compensation similar to current control arrangement 300 is described in detail in U.S. Patent No. 3,886,435, in the name of S. A. Steckler, entitled VBE VOLTAGE SOURCE TEMPERATURE COMPENSATION NETWORK.

By selecting a predetermined ratio between resistors R60 and R61, collector current i_{90a} flowing through terminal 300c, that is approximately equal to the sum of the currents in the collectors of transistors 76 and 77 or in resistors R60 and R61, is maintained constant throughout a wide range of operating temperatures. Because of the feedback arrangement of transistor 73, voltage V_{BR} causes the corresponding collector current in each of the other ones of transistors 90a-90n to be also temperature independent.

Terminal 300a is coupled to an I²L injector line 12 that provides a temperature compensated injection current that is equal to the sum of currents i_{90a} and i_{90b} to a portion of deflection IC 100 that utilizes the well known I²L technology. Transistors 290a-290j, that are coupled to line 12, represent the injector transistors of such portion of deflection IC 100.

Another example of an arrangement that is similar to that of transistors 90a-90n is depicted by transistors 190a-190m of the N-P-N type that may be utilized in various stages of deflection IC 100. Each of transistors 190a-190m has its base elec-

trode coupled to a common conductor, or rail line, that is referred to as NPN bus 10 and has its emitter electrode coupled via a corresponding resistor to ground.

Voltage V_{cc} at terminal 120 is coupled to the collector of a transistor 81 which has its base coupled to the collector of transistor 90i. The emitter of transistor 81 is coupled to the base of a transistor 82 which is coupled back via its collector to the collector of transistor 90i. Transistors 81 and 82 produce a temperature compensated voltage V_{BR1} on bus 10 that performs a function analogous to voltage V_{BR} of bus 11 and that is controlled by voltage V_{BR} . Thus, voltage V_{BR1} enables the collector currents in transistors 190a-190m to flow only when voltage V_{BR} enables the flow of the collector currents in transistors 90a-90n. Transistors 81 and 82 that are coupled to transistor 90i cause the collector current in each of transistors 190a-190m to be the current mirror of the collector current in transistor 90i that is controlled by voltage V_{BR} , and therefore, temperature independent.

Each of horizontal processor 100a and regulator processor 100b of FIGURE 1 that produce signals H_r and S_c , respectively, may include transistors from each of the groups 90a-90n, 190a-190m and 290a-290j. Thus, voltage V_{BR} controls the operation of processor 100a and of regulator processor 100b. An example of a manner by which, during normal operation, transistors such as transistors 90a-90n and 190a-190m of FIGURE 1 may be used for generating control signals such as, for example, signals S_c and H_r , is depicted in a data sheet for linear integrated circuits CA3210E and CA3223E of the RCA Corporation, published May, 1982, and entitled TV Horizontal/Vertical Countdown Digital Sync System.

When the collector currents in each of transistors 90a-90n of FIGURE 1 is zero, signal S_c , for example, is in an inactive state. The result is that, during the standby mode, a pass switch 102b of regulator 102 remains nonconductive; consequently, voltage $B+$ is not generated and horizontal output stage 99 remains unenergized.

In carrying out an aspect of the invention, on/off signal 110 is coupled via an arrangement, operating as a signal inverter, that includes transistors Q700, Q701 and Q703, to a junction terminal 200a of an on/off switching arrangement 200. During operation in the power-up mode, a second on/off control signal V_{200a} that is developed at junction terminal 200a is at a high level as a result of signal 110 being at the low level; conversely, during operation in the standby mode signal V_{200a} is at a low level.

On/off switching arrangement 200 includes a zener diode 83 that has its cathode coupled to voltage V_{cc} and its anode coupled via a resistor

R202 to junction terminal 200a that is coupled to the bases of two switching transistors 84 and 85. Junction terminal 200a is coupled via a resistor 86 to ground.

The emitter of switching transistor 84, that is conductive only during a short interval following a user initiated power-up command, referred to herein as the start-up interval, is coupled to bus 10 at a junction between the base of transistor 82 and the emitter of transistor 81. The collector of transistor 84 is coupled back to both collectors of transistors 76 and 77 of current control arrangement 300 at terminal 300c.

The collector of switching transistor 85 is coupled to the bases of transistors 87 and 90 and to voltage V_{cc} via a resistor 88 to turn-on transistors 87 and 90 when switching transistor 85 is nonconductive. The collector of transistor 87 is coupled back at terminal 300b to the base of transistor 76, to the collector of transistor 80 and to the collector of transistor 90b.

During the standby mode, control signal V_{200a} , that is at the low level as a result of signal 110 being at the high level, causes transistor 87 to be in saturation. Consequently, a collector current i_{90b} of transistor 90b that flows into terminal 300b is shunted away from transistor 80 by transistor 87 that is conductive. Therefore, the collector current in each of transistors 76, 77 and 80 is forced to be zero. It follows that when on/off control signal 110 is at the high level, as a result of the user initiated power-off command, no base current flows in transistor 73 of arrangement 300. The emitter current in transistor 73 is, therefore, also zero.

Voltage V_{BR} is, during normal operation power-up mode, a temperature compensated voltage that causes the corresponding collector currents in transistors 90a-90n to be temperature compensated, as described before.

Thus, in accordance with an aspect of the invention, in the standby mode, voltage V_{BR} causes the base current and, hence, the emitter current, in each of transistors 90a-90n, to be zero. Thus, temperature compensated arrangement 300 that generates temperature compensated voltage V_{BR} couples on/off signal 110 to bus 11 to turn off transistors 90a-90n. Because the collector current in transistor 90i is zero, the emitter current in each of transistors 190a-190m is also zero. Also, because the emitter current in each of transistors 76, 77 and 80 is zero, I^2L injector transistors 290a-290j become also nonconductive. The result is that control signal S_c remains at an inactive state that prevents conduction of switch 102b so as to prevent the generation of voltage $B+$. It follows that during the standby mode, supply current i_{PS} that flows in deflection IC 100 and that is proportional to the sum of the emitter currents in transistors 90a-90n,

for example, is reduced relative to its value during the power-up mode. The result is that current loading of standby transformer T0 is, advantageously, reduced during the standby mode.

As described before, when a user initiates the power-up mode, transistor 108, that is coupled to remote receiver 107, become conductive that causes signal 110 to be at the low level. When transistor Q703 becomes nonconductive, due to signal 110 being at the low level, conductive zener diode 83 generates signal V_{200a} . Zener diode 83 is conductive as long as voltage V_{cc} exceeds a predetermined minimum, or threshold, first level. Zener diode 83 prevents initiation of the start-up operation if capacitor 66 is not fully charged above the first level. On/off control signal V_{200a} at terminal 200a that is pulled up to a sufficiently high level by conductive zener 83 causes transistors 85 and 84 to become turned-on. With transistor 85 conducting, transistors 87 and 90 are turned off.

During the start-up interval and immediately after signal V_{200a} causes transistors 84 and 85 to turn on, transistor 84 draws current from the base of transistor 73, which begins to conduct simultaneously with transistor 84. Transistor 85 shunts the base currents of transistors 87 and 90, causing them to turn off. The conduction of transistor 73 causes transistors 90a, 90b and 90i to conduct the corresponding collector currents. Transistor 87 being turned off, allows the conduction of transistor 90b to turn on the feedback network comprising transistors 76, 77 and 80. Conduction of transistor 90i turns on transistors 81 and 82 that cause voltage V_{BR1} at the emitter of transistor 84 to increase. The increase in voltage V_{BR1} causes transistor 84 to become nonconductive. Transistor 73 base current is now supplied by conduction of transistors 76 and 77. In this way, current control arrangement 300 enables the emitter currents in each of transistors 90a-90n and 190a-190m to flow; thereby, deflection IC 100 that may include a horizontal oscillator, not shown in the FIGURES, becomes fully operational. The result is that signals H_r and S_c are generated and deflection switching transistor Q1 is switched on and off at the deflection rate f_H , that initiates the generation of voltage $V+$. As described before, voltage V_{cc} of deflection IC 100 is obtained during the power-up mode from voltage $V+$.

FIGURES 2a and 2b illustrate schematically waveforms useful for explaining the operation of deflection IC 100 of FIGURE 1 during the start-up interval. Similar numbers and symbols in FIGURES 1, 2a and 2b depict similar items or functions.

During portion t_0-t_1 of the start-up interval of FIGURES 2a and 2b, that immediately follows the user initiated power-up command, IC 100 of FIGURE 1 is powered primarily from the charge al-

ready stored in capacitor 66. Because of the loading caused by, for example, transistors 90a-90n, capacitor 66 may discharge prior to voltage $V+$ attaining its normal operational level. The result is that voltage V_{cc} of FIGURE 2b may be reduced at, for example, time t_1 to a level so low that voltage V_{cc} is insufficient to sustain operation in the power-up mode. The discharge of capacitor 66 of FIGURE 1 may occur since deflection IC 100 may draw more current than can be provided by standby voltage V_{SB} via resistor R1, that is relatively large valued. Resistor R1 is designed to be a large resistor so as to reduce loading of transformer T0 during the standby mode and start-up interval.

Should capacitor 66 be discharged during the start-up interval by, for example, current i_{PS} , zener diode 83 will turn off when capacitor 66 voltage falls below the breakdown zener voltage of diode 83. Transistor 85 remains, however, conductive, due to a supply of current through resistors 91 and 92. Deflection IC 100 will continue to operate to generate signals H_r and S_c until, for example, time t_1 of FIGURE 2b when voltage V_{cc} in capacitor 66 of FIGURE 1 falls below a second predetermined level VL2 of FIGURE 2b. The second predetermined level VL2 is a lower holding level of, for example, 4 volts, which is sufficient to supply enough current through resistors 91 and 92 of FIGURE 1 to maintain conduction of transistor 85. Below the lower holding level that occurs at time t_1 of FIGURE 2b, transistor 85 of FIGURE 1 turns off. When transistor 85 turns off, however, transistors 87 and 90 will again saturate, thus turning off transistor 76 which will cause the emitter currents in transistors 90a-90n and 190a-190m to become zero, so as to terminate the start-up operation after time t_1 of FIGURE 2b. With transistors 87 and 90 of FIGURE 1 again saturated, supply current i_{PS} from capacitor 66 will be reduced and the previously described start-up process will be repeated.

Capacitor 66 may, therefore, be recharged as many times as are necessary until power-up operation is obtained, to cause voltage $V+$ to be operative so as to supply voltage V_{cc} . Thus, during such portions of the start-up interval, such as, for example, during interval t_1-t_2 of FIGURE 2b, deflection IC 100 of FIGURE 1 is essentially in an off condition with the load current sources disabled until capacitor 66 recharges to the first predetermined voltage such as level VL1 that occurs at time t_2 of FIGURE 2b.

During interval t_2-t_3 , a second start-up attempt occurs that is similar to that occurring during interval t_0-t_1 . In the example shown, at time t_3 voltage $V+$ of FIGURE 1 becomes sufficiently large so as to begin charging capacitor 66 via diode D2. During interval t_3-t_4 of FIGURE 2b, capacitor 66 of FIGURE 1 is charged up to a level that is controlled by

shunt regulator 131 that occurs at time t_4 of FIGURE 2b. Henceforth, start-up operation ceases and normal operation in a power-up mode begins. It should be understood that a successful start-up attempt that is not terminated may occur immediately after time t_0 of FIGURE 2b when, for example, the amplitude of voltage V_{AC} is sufficiently high.

During the power-up mode that immediately follows the start-up interval, signal 110 is maintained at the low level, thereby maintaining signal V_{200a} at a high level. Transistors 87 and 84 are maintained nonconductive, and transistors 73, 76, 77 and 80 conductive. Consequently, normal operation emitter currents in transistors 90a-90n and 190a-190m, that are controlled by voltage V_{BR} , and normal operation level of supply current i_{PS} are maintained.

Thus, in accordance with a feature of the invention, voltage V_{BR} on PNP bus 11 that is temperature compensated during the power-up mode, operates as a switching signal, during the standby mode. In this way the emitter currents in transistors 90a-90n are, advantageously, switched off, during the standby mode.

Claims

1. A television apparatus selectively operable in a standby mode and a power-up mode, comprising :

a deflection circuit (99) for producing a deflection current (i_y) in a deflection winding (L_y) during operation of said television apparatus in a power-up mode;

a source (66) of a first supply voltage (V_{CC}) that is developed during operation of said television apparatus in each of said power-up and a standby mode;

a control circuit (IC 100) coupled to said deflection circuit (99) for controlling the operation of said deflection circuit during operation in said power-up mode and for preventing the production of said deflection current during operation in said standby mode, said control circuit including at least a first circuit stage (90a) that is coupled during operation in each of said power-up and standby modes to said source (66) of said first supply voltage (V_{CC}) to form a current path in which a first portion of a supply current flows from said source (66) of said first supply voltage (V_{CC}) during operation in said power-up mode;

a source (107) of an on/off control signal (110) that is selectively indicative of operation of said television apparatus in said power-up mode and in said standby mode; characterised by

means (300) coupled to said source (107) of said on/off control signal (110) for generating during operation of said television apparatus a second control signal (V_{BR}) whose value is substantially invariable with temperature, and that is applied to said first circuit stage (90a) to control said first portion (i_{90a}) of said supply current (i_{PS}) in a way that is temperature compensated, said temperature compensated generating means (300) being responsive to said on/off control signal (110) such that during operation of said television apparatus in said standby mode, said on/off control signal (110) causes said temperature compensated second control signal (V_{BR}) to reduce said first portion (i_{90a}) of said supply current (i_{PS}) that flows in said first circuit stage (90a).

2. An apparatus according to Claim 1 characterised by a first plurality of circuit stage (90b-90n) that form corresponding current paths to corresponding different portions of said supply current (i_{PS}) such that said second control signal (V_{BR}) that is coupled to each of said first plurality of circuit stages (90b-90n) separately causes a corresponding reduction of each of said corresponding different current portions in each of said circuit stages (90b-90n).

3. An apparatus according to Claim 1 characterised in that said deflection circuit (99) includes a flyback transformer (T1) for producing a second supply voltage (V_4) from said flyback transformer and wherein said source (66) of said first supply voltage (V_{CC}) develops said first supply voltage from said second supply voltage (V_4) during said power-up mode.

4. An apparatus according to Claim 1 characterised in that said control circuit (IC 100) is coupled to said deflection circuit (99) for producing a deflection rate related signal (H_r) for controlling the timings of said deflection current (i_y) in said deflection winding (L_y).

5. An apparatus according to Claim 4 characterised by controllable means (102) for generating a second supply voltage (B_4) wherein said control circuit (IC 100) further produces a pulse-width modulated control signal (S_c) that is coupled to said second supply voltage generating means (102) for controlling said second supply voltage during said power-up mode and for disabling said second supply voltage (B_4) during said standby mode.

6. An apparatus according to Claim 5 characterised in that said second supply voltage (B_4)

shunt regulator 131 that occurs at time t_4 of FIGURE 2b. Henceforth, start-up operation ceases and normal operation in a power-up mode begins. It should be understood that a successful start-up attempt that is not terminated may occur immediately after time t_6 of FIGURE 2b when, for example, the amplitude of voltage V_{AC} is sufficiently high.

During the power-up mode that immediately follows the start-up interval, signal 110 is maintained at the low level, thereby maintaining signal V_{200a} at a high level. Transistors 87 and 84 are maintained nonconductive, and transistors 73, 76, 77 and 80 conductive. Consequently, normal operation emitter currents in transistors 90a-90n and 190a-190m, that are controlled by voltage V_{BR} , and normal operation level of supply current i_{PS} are maintained.

Thus, in accordance with a feature of the invention, voltage V_{BR} on PNP bus 11 that is temperature compensated during the power-up mode, operates as a switching signal, during the standby mode. In this way the emitter currents in transistors 90a-90n are, advantageously, switched off, during the standby mode.

Claims

1. A television apparatus selectively operable in a standby mode and a power-up mode, comprising:

a deflection circuit (99) for producing a deflection current (i_y) in a deflection winding (L_y) during operation of said television apparatus in a power-up mode;

a source (66) of a first supply voltage (V_{cc}) that is developed during operation of said television apparatus in each of said power-up and a standby mode;

a control circuit (IC 100) coupled to said deflection circuit (99) for controlling the operation of said deflection circuit during operation in said power-up mode and for preventing the production of said deflection current during operation in said standby mode, said control circuit including at least a first circuit stage (90a) that is coupled during operation in each of said power-up and standby modes to said source (66) of said first supply voltage (V_{cc}) to form a current path in which a first portion of a supply current flows from said source (66) of said first supply voltage (V_{cc}) during operation in said power-up mode;

a source (107) of an on/off control signal (110) that is selectively indicative of operation of said television apparatus in said power-up mode and in said standby mode; characterised by

means (300) coupled to said source (107) of said on/off control signal (110) for generating during operation of said television apparatus a second control signal (V_{BR}) whose value is substantially invariable with temperature, and that is applied to said first circuit stage (90a) to control said first portion (i_{90a}) of said supply current (i_{PS}) in a way that is temperature compensated, said temperature compensated generating means (300) being responsive to said on/off control signal (110) such that during operation of said television apparatus in said standby mode, said on/off control signal (110) causes said temperature compensated second control signal (V_{BR}) to reduce said first portion (i_{90a}) of said supply current (i_{PS}) that flows in said first circuit stage (90a).

2. An apparatus according to Claim 1 characterised by a first plurality of circuit stage (90b-90n) that form corresponding current paths to corresponding different portions of said supply current (i_{PS}) such that said second control signal (V_{BR}) that is coupled to each of said first plurality of circuit stages (90b-90n) separately causes a corresponding reduction of each of said corresponding different current portions in each of said circuit stages (90b-90n).

3. An apparatus according to Claim 1 characterised in that said deflection circuit (99) includes a flyback transformer (T1) for producing a second supply voltage (V_4) from said flyback transformer and wherein said source (66) of said first supply voltage (V_{cc}) develops said first supply voltage from said second supply voltage (V_4) during said power-up mode.

4. An apparatus according to Claim 1 characterised in that said control circuit (IC 100) is coupled to said deflection circuit (99) for producing a deflection rate related signal (H_r) for controlling the timings of said deflection current (i_y) in said deflection winding (L_y).

5. An apparatus according to Claim 4 characterised by controllable means (102) for generating a second supply voltage (B_4) wherein said control circuit (IC 100) further produces a pulse-width modulated control signal (S_c) that is coupled to said second supply voltage generating means (102) for controlling said second supply voltage during said power-up mode and for disabling said second supply voltage (B_4) during said standby mode.

6. An apparatus according to Claim 5 characterised in that said second supply voltage (B_4)

is coupled to said deflection circuit (99) to provide a substantial portion of the entire energy requirement of said deflection circuit (99).

7. An apparatus according to Claim 1 characterised in that said first circuit stage comprises a first transistor (90a) having a first main current conducting electrode (emitter) that is coupled to said source (66) of first supply voltage (V_{cc}) and that is energized thereby during said power-up and standby modes such that said first portion (i90a) of said supply current (ips) flows from said source (66) of first supply voltage (V_{cc}) in said first main current conducting electrode during said power-up mode and wherein said second control signal (V_{BR}) is coupled to a control electrode (base) of said first transistor (90a).

8. An apparatus according to Claim 7 characterised in that said second control signal (V_{BR}) causes said first transistor (90a) to operate as a switch that is nonconductive when said on/off control signal (110) is indicative of operation in said standby mode.

9. An apparatus according to Claim 7 characterised in that said control circuit (IC 100) further comprises a first plurality of transistors (90b-90n) having control electrodes (bases) that are coupled to said on/off control signal via a path including a common conductor (for V_{BR}) that causes a corresponding current in each of said first plurality of transistors (90b-90n) to be the current mirror of said current in said first transistor (90a) that is temperature compensated.

10. An apparatus according to Claim 9 characterised in that each transistor of said first plurality of transistors (90b-90n) operates as a current source to produce a corresponding current portion in a corresponding main current conducting electrode thereof only during said power-up mode.

11. An apparatus according to Claim 1 characterised in that said means (300) for generating said second control signal (V_{BR}) comprises a circuit arrangement (290a-290j) that requires an I^2L injection current for operation during said power-up mode, and wherein said means (300) for generating said second control signal (V_{BR}) is coupled to said circuit arrangement (290a-290j) for supplying said I^2L injection current that is temperature compensated, such that said means (300) for generating said second control signal (V_{BR}) prevents said I^2L injection

current from flowing during said standby mode.

12. An apparatus according to Claim 1 characterised in that said means (300) for generating said second control signal (V_{BR}) comprises a source of temperature dependent voltage that is proportional to a voltage established across a first conductive P-N junction structure (base emitter of 80), a first resistance (R60) coupled in parallel with said source of temperature dependent voltage for drawing a current at a value that is in accordance with said voltage across said first P-N junction structure, a second P-N junction structure (base emitter of 77) and second resistance (61) that form with said second P-N junction structure a series arrangement that is coupled in parallel with said first resistance (R60) for conducting a current in said second resistance (R61) that is in accordance with said voltage across said first P-N junction structure (base emitter of 80), said current in said second resistance (R61) having a temperature variation coefficient which is proportional to the negative of the temperature variation coefficient of said current in said first resistance (R60) that substantially compensates for said temperature coefficient of said current in said first resistance (R60) over a wide range of operating temperatures, and a feedback arrangement (73) responsive to the sum of said currents in said first (R60) and second (R61) resistances for developing said second control signal (V_{BR}) to provide a temperature compensated control voltage that is coupled to a control electrode (base) of a first transistor (90a) that is included in said first circuit stage.

13. An apparatus according to Claim 12 characterised in that said feedback arrangement comprises a second transistor (73) having a main current conducting electrode (emitter) that is coupled to said control electrode (base) of said first transistor (90a) and wherein said current in said first transistor (90a), said current in said first resistance (R60) and said current in said second resistance (R61) are combined at a control electrode (base) of said second transistor (73) for developing a voltage thereat that is coupled to said control electrode (base) of said first transistor (90a) via said main current conducting electrode (emitter) of said second transistor (73).

14. An apparatus according to Claim 1 characterised in that said control circuit (IC 100) further comprises a plurality of transistors

(90b-90n) each transistor of said plurality of transistors having a control electrode (base) that is coupled to a current conducting terminal (emitter) of said first circuit stage (90a) such that a corresponding current in each transistor of said plurality of transistors (90a-90n) is the current mirror of said current in said first circuit stage (90a) that causes a corresponding reduction in said corresponding current in each of said transistors of said plurality of transistors during said standby mode.

15. An apparatus according to Claim 1 characterised in that said source of first supply voltage (Vcc) comprises a source (V_{AC}) of AC mains voltage, a voltage step-down transformer (TO) coupled to said source of AC mains voltage, a rectifier (D106) having an input terminal that is coupled to said step-down transformer for generating a standby supply voltage (V_{SB}) by rectifying a voltage that is developed at said step-down transformer that supplies said supply current (ips) during said standby mode.

16. An apparatus according to Claim 15 characterised by a source (104) of a second supply voltage (V4) that is developed during said power-up mode, and means (D2) for selectively coupling said standby supply voltage (V_{SB}) to an input supply terminal (120) of said control circuit (IC 100) during said standby mode and for selectively coupling said second supply voltage (V4) during said power-up mode so as to produce said first supply voltage (Vcc) at said input supply terminal (120) during both said power-up and standby modes.

17. An apparatus according to Claim 16 characterised in that said source (104) of second supply voltage (V4) comprises a winding (W2) of a flyback transformer (T1) coupled to said deflection circuit (99), and a rectifier (D4) coupled to said winding (W2) for providing said second supply voltage (V4) only during said power-up mode.

18. An apparatus according to Claim 15 characterised in that said second control signal (V_{BR}) causes a reduction in a current that flows in said step-down transformer (TO) during said standby mode.

19. An apparatus according to Claim 1 characterised in that said source (109) of said on/off control signal (110) comprises a remote receiver of said television apparatus.

20. An apparatus according to Claim 1 characterised in that said control circuit (IC 100) further includes a circuit portion (131, 200) that is coupled to said first supply voltage (Vcc) and that is energized thereby during both said power-up and standby modes.

21. An apparatus according to Claim 20 characterised in that said circuit portion comprises a shunt regulator (131) that regulates said first supply voltage (Vcc).

22. An apparatus according to Claim 1 characterised in that said control circuit (IC 100) forms an integrated circuit and wherein said first supply voltage (Vcc) is applied to an input supply terminal (120) during both said power-up and standby modes.

Patentansprüche

1. Fernsehgerät, das wahlweise im Bereitschaftsbetrieb und im Normalbetrieb arbeitet, umfassend:

eine Ablenkschaltung (99) zur Erzeugung eines Ablenkstromes (iy) in einer Ablenkwicklung (Ly) im Normalbetrieb des Fernsehgerätes;

eine Quelle (66) für eine erste Versorgungsspannung (Vcc), die sowohl im Normalbetrieb als auch im Bereitschaftsbetrieb des Fernsehgerätes erzeugt wird;

eine mit der Ablenkschaltung (99) verbundene Steuerschaltung (IC 100) zur Steuerung des Betriebs der Ablenkschaltung während des Normalbetriebs und zur Verhinderung der Erzeugung des Ablenkstroms während des Bereitschaftsbetriebes, wobei die Steuerschaltung wenigstens eine erste Schaltungsstufe (90a) enthält, die sowohl im Bereitschaftsbetrieb als auch im Normalbetrieb mit der Quelle (66) für die erste Versorgungsspannung (Vcc) verbunden ist, um einen Stromweg zu bilden, in dem ein erster Teil eines Versorgungsstroms von der Quelle (66) für die erste Versorgungsspannung (Vcc) im Normalbetrieb fließt;

eine Quelle (107) für ein Ein/Aus-Steuersignal (110), zur wahlweisen Anzeige, ob sich das Fernsehgerät im Normal- oder Bereitschaftsbetrieb befindet; gekennzeichnet durch:

mit der Quelle (107) für das Ein/Aus-Steuersignal verbundene Mittel (300) zur Erzeugung eines zweiten Steuersignals (V_{BR}) während des Betriebs des Fernsehgerätes, dessen Wert weitgehend unveränderbar mit der Temperatur ist, und das der ersten Schaltungsstufe (90a) zugeführt wird, um den ersten Teil (I_{90a}) des Versorgungsstroms in einer Weise zu

- steuern, daß eine Temperaturkompensation eintritt, wobei die in der Temperatur kompensierten Mittel (300) auf das Ein/Aus-Steuersignal so ansprechen, daß im Bereitschaftsbetrieb des Fernsehgerätes das Ein/Aus-Steuersignal (110) bewirkt, daß das in der Temperatur kompensierte Steuersignal (V_{BR}) den ersten Teil (i_{90a}) des Versorgungstroms (i_p) vermindert, der in der ersten Schaltungsstufe (90a) fließt.
2. Gerät nach Anspruch 1, gekennzeichnet durch eine erste Vielzahl von Schaltungsstufen (90b - 90a), die entsprechende Stromwege zu entsprechenden unterschiedlichen Teilen des Versorgungstromes (i_p) derart bilden, daß das zweite Steuersignal (V_{BR}), das mit jeder der ersten Vielzahl von Schaltungsstufen (90b - 90n) verbunden ist, getrennt eine entsprechende Verminderung jedes der entsprechenden unterschiedlichen Stromteile in jeder der Schaltungsstufen (90b - 90n) bewirkt.
 3. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Ablenkschaltung (99) einen Zeilenendtransformator (T1) zur Erzeugung einer zweiten Versorgungsspannung (V_4) von dem Zeilenendtransformator enthält, und daß die Quelle (66) für die erste Versorgungsspannung (V_{cc}) die erste Versorgungsspannung während des Normalbetriebes aus der zweiten Versorgungsspannung (V_4) entwickelt.
 4. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Steuerschaltung (IC 100) mit der Ablenkschaltung (99) verbunden ist, um ein auf die Ablenkrate bezogenes Signal (H_r) zu erzeugen, um das Timing des Ablenkstromes (i_y) in der Ablenkwicklung (L_y) zu steuern.
 5. Gerät nach Anspruch 4, gekennzeichnet durch steuerbare Mittel (102) zur Erzeugung einer zweiten Versorgungsspannung (B_4), wobei die Steuerschaltung (IC 100) ferner einimpulsbreitenmoduliertes Steuersignal (Sc) erzeugt, das den Mitteln (102) zur Erzeugung der zweiten Versorgungsspannung zugeführt wird, um die zweite Versorgungsspannung während des Normalbetriebes zu steuern, und um die zweite Versorgungsspannung (B_4) während des Bereitschaftsbetriebs unwirksam zu machen.
 6. Gerät nach Anspruch 5, dadurch gekennzeichnet, daß die zweite Versorgungsspannung (B_4) der Ablenkschaltung (99) zugeführt wird, um einen nennenswerten Teil des gesamten Energiebedarfs der Ablenkschaltung (99) zu liefern.
 7. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die erste Schaltungsstufe einen ersten Transistor (90a) enthält, der eine erste stromführende Hauptelektrode (Emitter) hat, die mit der Quelle (66) für die erste Versorgungsspannung (V_{cc}) verbunden ist, und die dadurch während des Normal- und Bereitschaftsbetriebs so gespeist wird, daß der erste Teil (i_{90a}) des Versorgungstroms (i_p) von der Quelle (66) für die erste Versorgungsspannung (V_{cc}) in der ersten stromführenden Haupt-Elektrode während des Normalbetriebes fließt, und wobei das zweite Steuersignal (V_{BR}) einer Steuerelektrode (Basis) des ersten Transistors (90a) zugeführt wird.
 8. Gerät nach Anspruch 7, dadurch gekennzeichnet, daß das zweite Steuersignal (V_{BR}) bewirkt, daß der erste Transistor (90a) als Schalter arbeitet, der nichtleitend ist, wenn das Ein/Aus-Steuersignal (110) den Bereitschaftsbetrieb anzeigt.
 9. Gerät nach Anspruch 7, dadurch gekennzeichnet, daß die Steuerschaltung (IC 100) ferner eine erste Vielzahl von Transistoren (90b-90n) enthält, deren Steuerelektroden (Basen) das Ein/Aus-Steuersignal über einen gemeinsamen Leiter (für V_{BR}) enthaltenden Weg zugeführt wird, der einen entsprechenden Strom in jedem der ersten Vielzahl von Transistoren (90b-90n) bewirkt, der das Spiegelbild des Stroms in dem ersten Transistor (90a) ist, der in der Temperatur kompensiert ist.
 10. Gerät nach Anspruch 9, dadurch gekennzeichnet, daß jeder Transistor der ersten Vielzahl von Transistoren (90b-90n) als Stromquelle arbeitet, um einen entsprechenden Stromanteil in einer entsprechenden stromführenden Haupt-Elektrode nur während des Normalbetriebes zu erzeugen.
 11. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Mittel (300) zur Erzeugung des zweiten Steuersignals (V_{BR}) eine erste Schaltungsanordnung (290a-290j) umfassen, die einen I^2L -Injektionsstrom während des Normalbetriebes erfordert, und daß die Mittel (300) zur Erzeugung des zweiten Steuersignals (V_{BR}) mit der Schaltungsanordnung (290a-290j) verbunden ist, um den temperaturkompensierten I^2L -Injektionsstrom so zuzuführen, daß die Mittel (300) zur Erzeugung des zweiten Steuersignals (V_{BR}) verhindern, daß der I^2L -Injektionsstrom während des Bereitschaftsbetriebs fließt.

12. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Mittel (300) zur Erzeugung des zweiten Steuersignals (V_{BR}) umfassen: eine Quelle für eine temperaturabhängige Spannung, die proportional zu einer Spannung ist, die über einem ersten leitenden P-N-Übergang (Basis-Emitter von 80), einen ersten Widerstand (R60), der parallel zu der temperaturabhängigen Spannungsquelle errichtet wird, um einem Strom mit einem Wert zu ziehen, der in Übereinstimmung mit der Spannung über dem ersten P-N-Übergang ist, einen zweiten P-N-Übergang (Basis-Emitter von 77), und einen zweiten Widerstand (R61), der mit dem zweiten P-N-Übergang eine Reihenanordnung bildet, die mit dem ersten Widerstand (R60) parallel geschaltet ist, um einen Strom durch den zweiten Widerstand (R61) zu leiten, der gemäß der Spannung über dem ersten P-N-Übergang (Basis-Emitter von 80) ist, wobei der Strom in dem zweiten Widerstand (R61) einen Temperaturänderungskoeffizienten hat, der proportional zum Negativen des Temperaturänderungskoeffizienten des Stromes in den ersten Widerstand (R60) ist, der weitgehend den Temperaturkoeffizienten des Stromes in dem ersten Widerstand (R60) über einen weiten Bereich von Betriebstemperaturen kompensiert, und eine Rückkopplungsanordnung (73), die auf die Summe der Ströme in dem ersten (R60) und zweiten Widerstand (R61) anspricht, um das zweite Steuersignal (V_{BR}) zu erzeugen und eine temperaturkompensierte Steuerspannung vorzusehen, die einer Steuerelektrode (Basis) eines ersten Transistors (90a) zugeführt wird, der in der ersten Schaltungsstufe enthalten ist.

13. Gerät nach Anspruch 12, dadurch gekennzeichnet, daß die Rückkopplungsanordnung einen zweiten Transistor (73) enthält, der eine stromführende Hauptelektrode (Emitter) hat, die mit der Steuerelektrode (Basis) des ersten Transistors (90a) verbunden ist, und daß der Strom in dem ersten Transistor (90a), der Strom in dem ersten Widerstand (R60) und der Strom in dem zweiten Widerstand (R61) an einer Steuerelektrode (Basis) des zweiten Transistors (73) kombiniert wird, um daran eine Spannung zu entwickeln, die der Steuerelektrode (Basis) des ersten Transistors (90a) über die stromführende Hauptelektrode (Emitter) des zweiten Transistors (73) zugeführt wird.

14. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Steuerschaltung (IC 100) ferner eine Vielzahl von Transistoren (90b-90n) umfaßt, von denen jeder Transistor eine Steuerelektrode (Basis) hat, die mit einer stromfüh-

renden Klemme (Emitter) der ersten Schaltungsstufe (90a) so verbunden ist, daß ein entsprechender Strom in jedem Transistor der Vielzahl von Transistoren (90a-90n) das Spiegelbild des Stromes in der ersten Schaltungsstufe (90a) ist, was eine entsprechende Verminderung des entsprechenden Stromes in jedem der Transistoren der Vielzahl von Transistoren während des Bereitschaftsbetriebs bewirkt.

15. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Quelle für die erste Versorgungsspannung (V_{CC}) eine Netzwechsellspannungsquelle (V_{AC}), einen Spannungs-Abwärts-Transformator (TO), der mit der Netzwechsellspannungsquelle verbunden ist, und einen Gleichrichter (D106) umfaßt, dessen Eingangsklemme mit dem Abwärtstransformator verbunden ist, um eine Bereitschaftsversorgungsspannung (V_{SB}) zu erzeugen, indem eine Spannung gleichgerichtet wird, die an dem Abwärtstransformator entwickelt wird, der den Versorgungsstrom (Ips) im Bereitschaftsbetrieb liefert.

16. Gerät nach Anspruch 15, gekennzeichnet durch eine Quelle (104) für eine zweite Versorgungsspannung (V_4), die während des Normalbetriebs entwickelt wird, und durch Mittel (D2) zur wahlweisen Zuführung der Bereitschaftsversorgungsspannung (V_{SB}) zu einer Eingangsversorgungsklemme (120) der Steuerschaltung (IC 100) während des Bereitschaftsbetriebes, und zur wahlweisen Zuführung der zweiten Versorgungsspannung (V_4) während des Normalbetriebes, um so die erste Versorgungsspannung (V_{CC}) an der Eingangsversorgungsklemme (120) sowohl während des Normalbetriebs als auch während des Bereitschaftsbetriebs zu erzeugen.

17. Gerät nach Anspruch 16, dadurch gekennzeichnet, daß die Quelle (104) für die zweite Versorgungsspannung (V_4) eine Wicklung (W_2) eines Zeilenendtransformators (T1), die mit der Ablenkschaltung (99) verbunden ist, und einen Gleichrichter (T4) umfaßt, der mit der Wicklung (W_2) verbunden ist, um die zweite Versorgungsspannung (V_4) nur während des Normalbetriebs zu erzeugen.

18. Gerät nach Anspruch 15, dadurch gekennzeichnet, daß das zweite Steuersignal (V_{BR}) eine Verminderung des Stroms bewirkt, der in dem Abwärtstransformator (TO) während des Bereitschaftsbetriebes fließt.

19. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Quelle (109) für das Ein/Aus-Steuersignal (110) den Empfänger einer Fernbedienung des Fernsehgerätes umfaßt.

20. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Steuerschaltung (IC 100) ferner einen Schaltungsteil (131, 200) enthält, dem die erste Versorgungsspannung (Vcc) zugeführt wird, und der dadurch während des Normalbetriebs und während des Bereitschaftsbetriebs gespeist wird.

21. Gerät nach Anspruch 20, dadurch gekennzeichnet, daß der erste Schaltungsteil einen Nebenschlußregler (131) enthält, der die erste Versorgungsspannung (Vcc) regelt.

22. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Steuerschaltung (IC 100) eine integrierte Schaltung bildet, und daß die erste Versorgungsspannung (Vcc) der Eingangs-Versorgungsklemme (120) sowohl bei Normalbetrieb als auch bei Bereitschaftsbetrieb zugeführt wird.

Revendications

1. Dispositif de télévision capable de fonctionner sélectivement dans un mode d'attente et dans un mode sous tension, comprenant :

un circuit de déviation (99) pour produire un courant de déviation (Iy) dans un enroulement de déviation (Ly) pendant le fonctionnement dudit dispositif de télévision dans un mode sous tension ;

une source (66) d'une première tension d'alimentation (Vcc) qui est développée pendant le fonctionnement dudit dispositif de télévision dans chacun desdits modes d'attente et sous tension ;

un circuit de commande (IC 100) couplé audit circuit de déviation (99) pour commander le fonctionnement dudit circuit de déviation pendant le fonctionnement dans ledit mode sous tension et pour empêcher la production dudit courant de déviation pendant le fonctionnement dans ledit mode d'attente, ledit circuit de commande comprenant au moins un premier étage de circuit (90a) qui est couplé pendant le fonctionnement dans chacun desdits modes d'attente et sous tension à ladite source (66) de ladite première tension d'alimentation (Vcc) pour former un trajet de courant dans lequel une première partie d'un courant d'alimentation circule à partir de ladite source (66) de ladite première tension d'alimentation (Vcc) pendant le fonctionnement dans ledit

mode sous tension ;

une source (107) d'un signal de commande de marche/arrêt (110) qui est sélectivement indicateur du fonctionnement dudit dispositif de télévision dans ledit mode sous tension et dans ledit mode d'attente ; caractérisé par

un moyen (300) couplé à ladite source (107) dudit signal de commande de marche/arrêt (110) pour générer pendant le fonctionnement dudit dispositif de télévision un second signal de commande (VBR) dont la valeur est sensiblement invariable avec la température et qui est appliqué audit premier étage de circuit (90a) pour contrôler ladite première partie (I_{90a}) dudit courant d'alimentation (Ips) d'une façon qui est à compensation thermique, ledit moyen pour générer un signal à compensation thermique étant sensible audit signal de commande de marche/arrêt (110) de telle sorte que, pendant le fonctionnement dudit dispositif de télévision dans ledit mode d'attente, ledit signal de commande de marche/arrêt entraîne ledit second signal de commande à compensation thermique (VBR) à réduire ladite première partie (I_{90a}) dudit courant d'alimentation (Ips) qui circule dans ledit premier étage de circuit (90a).

2. Dispositif selon la revendication 1, caractérisé par une première pluralité d'étages de circuit (90b-90a) qui forme des trajets de courant correspondant aux différentes parties correspondantes dudit courant d'alimentation (Ips) de telle sorte que ledit second signal de commande (VBR) qui est couplé à chaque étage de ladite pluralité d'étages de circuit (90b-90a) provoque séparément une réduction correspondante de chacune desdites différentes parties de courant dans chacun desdits étages de circuit (90b-90a).

3. Dispositif selon la revendication 1, caractérisé en ce que ledit circuit de déviation (99) inclut un transformateur de retour de balayage (TI) pour produire une seconde tension d'alimentation (V4) à partir dudit transformateur de retour et dans lequel ladite source (66) de ladite première tension d'alimentation (Vcc) développe ladite première tension d'alimentation à partir de ladite seconde tension d'alimentation (V4) pendant ledit mode sous tension.

4. Dispositif selon la revendication 1 caractérisé en ce que ledit circuit de commande (IC 100) est couplé audit circuit de déviation (99) pour produire un signal (Hr) relié à la fréquence de déviation pour contrôler les rythmes dudit courant de déviation (Iy) dans ledit enroulement de

déviations (I_y).

5. Dispositif selon la revendication 4 caractérisé par un moyen réglable (102) pour générer une seconde tension d'alimentation (B4) dans lequel ledit circuit de commande (IC 100) produit de plus un signal de commande modulé en largeur d'impulsion (S_c) qui est couplé audit moyen de production de la seconde tension d'alimentation (102) pour commander ladite seconde tension d'alimentation pendant ledit mode sous tension et pour invalider ladite seconde tension d'alimentation (B4) pendant ledit mode d'attente.
6. Dispositif selon la revendication 5 caractérisé en ce que ladite seconde tension d'alimentation (B4) est couplée audit circuit de déviation (99) pour fournir une partie importante de la demande totale d'énergie dudit circuit de déviation (99).
7. Dispositif selon la revendication 1 caractérisé en ce que ledit premier étage de circuit comprend un premier transistor (90a) comportant une première électrode conductrice de courant principal (émetteur) qui est couplée à ladite source (66) de la première tension d'alimentation (V_{cc}) et qui est, de ce fait, excitée pendant lesdits modes sous tension et d'attente de telle sorte que ladite première partie (i90a) dudit courant d'alimentation (ips) circule à partir de ladite source (66) de la première tension d'alimentation (V_{cc}) dans ladite première électrode conductrice de courant principal pendant ledit mode sous tension et dans lequel ledit second signal de commande (V_{BR}) est couplé à une électrode de commande (base) dudit premier transistor (90a).
8. Dispositif selon la revendication 7 caractérisé en ce que ledit second signal de commande (V_{BR}) entraîne ledit premier transistor (90a) à fonctionner comme un commutateur qui est non conducteur lorsque le signal de commande de marche/arrêt (110) est indicateur du fonctionnement dans ledit mode d'attente.
9. Dispositif selon la revendication 7 caractérisé en ce que ledit circuit de commande (IC 100) comprend une première pluralité de transistors (90b-90n) comportant des électrodes de commande (bases) qui sont couplées audit signal de commande de marche/arrêt via un trajet incluant un conducteur commun (pour V_{BR}) qui entraîne un courant correspondant dans chaque transistor de ladite première pluralité de transistors (90b-90n) à devenir le miroir de

courant dudit courant dans ledit transistor (90a) qui est à compensation thermique.

10. Dispositif selon la revendication 9 caractérisé en ce que chaque transistor de ladite première pluralité de transistors (90b-90n) fonctionne comme une source de courant pour produire une partie de courant correspondante dans leur électrode conductrice de courant principal correspondante seulement pendant ledit mode sous tension.
11. Dispositif selon la revendication 1 caractérisé en ce que ledit moyen (300) pour générer ledit second signal de commande (V_{BR}) comprend un agencement de circuit (290a-290j) qui demande un courant d'injection (I^2L) (logique d'injection intégrée) pour un fonctionnement pendant ledit mode sous tension et dans lequel ledit moyen (300) pour générer ledit second signal de commande (V_{BR}) est couplé audit agencement de circuit (290a-290j) pour fournir ledit courant d'injection I^2L qui est à compensation thermique de telle sorte que ledit moyen (300) pour générer ledit second signal de commande (V_{BR}) empêche ledit courant d'injection I^2L de circuler pendant ledit mode d'attente.
12. Dispositif selon la revendication 1 caractérisé en ce que ledit moyen (300) pour générer ledit second signal de commande (V_{BR}) comprend une source de tension dépendante de la température qui est proportionnelle à une tension établie à travers une première structure de jonction P-N conductrice (base émetteur de 80), une première résistance (R 60) couplée en parallèle à ladite source de tension dépendante de la température pour extraire un courant à une valeur qui est en conformité avec ladite tension à travers ladite première structure de jonction P-N, une seconde structure de jonction P-N (base -émetteur de 77) et une seconde résistance (61) qui forment avec ladite seconde structure de jonction P-n, un agencement en série qui est couplé en parallèle à ladite première résistance (R60) pour conduire un courant dans ladite seconde résistance (R 61) qui est en conformité avec ladite tension à travers ladite première structure de jonction P-N (base émetteur de 80), ledit courant dans ladite seconde résistance (R61) ayant un coefficient de variation de température qui est proportionnel à la valeur négative du coefficient de variation de température dudit courant dans ladite première résistance (R 60) qui compense sensiblement ledit coefficient de température dudit courant dans ladite première résistan-

ce (R 60) sur une large gamme de températures de fonctionnement, et un circuit de réaction (73) sensible à la somme desdits courants dans lesdites première (R 60) et seconde (R 61) résistances afin de développer ledit second signal de commande (V_{BR}) pour fournir une tension de commande à compensation thermique qui est couplée à une électrode de commande (base) d'un premier transistor (90a) qui est inclus dans ledit premier étage de circuit.

13. Dispositif selon la revendication 12 caractérisé en ce que ledit circuit de réaction comprend un second transistor (73) comportant une électrode conductrice du courant principal (émetteur) qui est couplée à ladite électrode de commande (base) dudit premier transistor (90a) et dans lequel ledit courant dans ledit premier transistor (90a), ledit courant dans ladite première résistance (R60) et ledit courant dans ladite seconde résistance (R 61) sont combinés au niveau d'une électrode de commande (base) dudit second transistor (73) pour développer à ce niveau une tension qui est couplée à ladite électrode de commande (base) dudit premier transistor (90A) via ladite électrode conductrice du courant principal (émetteur) dudit second transistor (73).

14. Dispositif selon la revendication 1 caractérisé en ce que ledit circuit de commande (IC 100) comprend, de plus, une pluralité de transistors (90b-90n) chaque transistor de ladite pluralité de transistors ayant une électrode de commande (base) qui est couplée à une borne conductrice de courant (émetteur) dudit premier étage de circuit (90a) de telle sorte qu'un courant correspondant dans chaque transistor de ladite pluralité de transistors (90a-90n) est le miroir de courant dudit courant dudit premier étage de circuit (90a) qui provoque une réduction correspondante dudit courant correspondant dans chacun desdits transistors de ladite pluralité de transistors pendant ledit mode d'attente.

15. Dispositif selon la revendication 1 caractérisé en ce que ladite source de la première tension d'alimentation (V_{CC}) comprend une source (V_{AC}) de tension d'alimentation CA (courant alternatif), un transformateur d'abaissement de tension (TO) couplé à ladite source de tension d'alimentation CA, un redresseur (D 106) ayant une borne d'entrée qui est couplée audit transformateur d'abaissement de tension pour produire une tension d'alimentation d'attente (V_{SB}) en redressant une tension qui est développée audit transformateur d'abaissement de tension qui fournit ledit courant d'alimentation

(ips) pendant ledit mode d'attente.

16. Dispositif selon la revendication 15 caractérisé par une source (104) d'une seconde tension d'alimentation (V_4) qui est développée pendant ledit mode sous tension et un moyen (D2) pour coupler sélectivement ladite tension d'alimentation d'attente (V_{SB}) à une borne de connexion d'entrée (120) dudit circuit de commande (IC 100) pendant ledit mode d'attente et pour coupler sélectivement ladite seconde tension d'alimentation (V_4) pendant ledit mode sous tension de façon à produire ladite première tension d'alimentation (V_{CC}) à ladite borne de connexion d'entrée (120) pendant les deux dits modes sous tension et d'attente.

17. Dispositif selon la revendication 16 caractérisé en ce que ladite source (104) de la seconde tension d'alimentation (V_4) comprend un enroulement (W_z) d'un transformateur de retour de balayage (T1) couplé audit circuit de déviation (99) et un redresseur (D4) couplé audit enroulement (W_z) pour fournir ladite seconde tension d'alimentation (V_4) seulement pendant ledit mode sous tension.

18. Dispositif selon la revendication 15 caractérisé en ce que ledit second signal de commande (V_{BR}) entraîne une réduction du courant qui circule dans ledit premier transformateur d'abaissement de tension (TO) pendant ledit mode d'attente.

19. Dispositif selon la revendication 1 caractérisé en ce que ladite source (109) dudit signal de commande de marche/arrêt (110) comprend un récepteur à distance dudit dispositif de télévision.

20. Dispositif selon la revendication 1 caractérisé en ce que ledit circuit de commande (IC 100) inclut, de plus, une partie de circuit (131, 200) qui est couplée à ladite première tension d'alimentation (V_{CC}) et qui est excitée, de ce fait, pendant les deux dits modes sous tension et d'attente.

21. Dispositif selon la revendication 20 caractérisé en ce que ladite partie de circuit comprend un régulateur en dérivation (131) qui régule ladite première tension d'alimentation (V_{CC}).

22. Dispositif selon la revendication 1 caractérisé en ce que ledit circuit de commande (IC 100) forme un circuit intégré et dans lequel ladite première tension d'alimentation (V_{CC}) est appliquée à une borne de connexion d'entrée (120)

pendant les deux dits modes sous tension et d'attente.

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