

DESCRIPTION

LIQUID CRYSTAL DISPLAY DEVICE

5

TECHNICAL FIELD

[0001]

The present invention relates to a liquid crystal display device. More specifically, the present invention relates to a liquid crystal display device that adopts a driving method using a thin film transistor.

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BACKGROUND ART

[0002]

A liquid crystal display (LCD) device is a device which performs display in such a manner that the optical property of light emitted from a light source is controlled by using a liquid crystal layer, and the like, filled between a pair of substrates, and is widely used in various fields by taking advantage of its features, such as thin profile, light weight and low power consumption.

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[0003]

In the liquid crystal display device, an alignment state of liquid crystal molecules is changed by applying a voltage to the liquid crystal layer by using a pair of electrodes formed on the substrates, and thereby a polarization state of the light passing through the liquid crystal layer is changed. In the liquid crystal display device, color filters of a plurality of colors are formed to perform color display. The pair of substrates sandwiching the liquid crystal layer are held by spacers so as to have a uniform gap (cell gap) therebetween and are bonded to each other by a sealing material.

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[0004]

In the liquid crystal display device, subsidiary pixels of three colors of red (R), green (G) and blue (B) are usually formed. A color filter of each color is arranged for each of

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the subsidiary pixels, and color control is performed for each pixel by adjusting light passing through the color filter of each color.

[0005]

5 In recent years, there has been made such a contrivance that, in addition to the RGB, a white (W) subsidiary pixel is arranged in order to increase luminance (see, for example, Patent Literature 1). Further, a method has also been
10 investigated in which the areas of the RGBW subsidiary pixels are made different for each color so as to suitably adjust color balance (see, for example, Patent Literature 2).

[0006]

 In the liquid crystal display device, pixel electrodes are usually arranged in a matrix form, and each of the pixel
15 electrodes is driven through a switch formed by a thin film transistor (TFT). The TFT is a three terminal field-effect transistor, and a drain electrode of each of the TFTs is connected to the pixel electrode corresponding to the TFT. A
 gate electrode of each of the TFTs is connected to a gate bus
20 line of each row of the matrix. A source electrode of each of the TFTs is connected to a source bus line of each column of the matrix. A desired image can be obtained by applying an image signal to the source bus line and by sequentially scanning the gate bus line.

25 [0007]

 Some of the liquid crystal display devices have a multi-gap configuration in which a thickness (cell gap) of the liquid crystal layer is made different for the subsidiary pixel of each color. However, when a size of the cell gap is made
30 different, a value of capacitance associated with the pixel electrode is changed. Therefore, in order to eliminate the difference in the pixel capacitance between the subsidiary pixels, it is necessary to make contrivances such as (a) making storage capacitance different for each of the pixels by
35 equalizing pixel electrode areas or (b) equalizing the storage

capacitance between the pixels by making the pixel electrode areas different from each other (see, for example, Patent Literature 3).

[0008]

5 Further, in the liquid crystal display device, in order to solve a viewing angle dependency problem due to a difference in γ characteristics between the time when the display is viewed in a front direction and the time when the display is viewed in an oblique direction, there is a case where a pixel is divided
10 into a plurality of sub-pixels, and where the γ characteristics of the respective sub-pixels are made close to each other (see, for example, Patent Literature 4). The γ characteristics mean gradation dependency of display luminance. That the γ characteristics are different between the time when the display
15 is viewed in the front direction and the time when the display is viewed in the oblique direction means that a gradation display state is changed according to the observation direction. The viewing angle dependency problem due to the γ characteristics can be eliminated in such a manner that a state
20 having different γ characteristics is formed by applying a different voltage to the liquid crystal layer corresponding to each of the sub-pixels.

[0009]

Further, as a method for forming a spacer, a method has
25 also been tried in which, when color filters are formed in correspondence with RGB subsidiary pixels, the color filters are also similarly formed at a place where the spacer is to be formed, and are laminated to form the spacer (see, for example, Patent Literature 5). In Patent Literature 5, in order to
30 compensate a change in the capacitance of each pixel electrode due to the spacer formed in the subsidiary pixel, a method has been investigated which equalizes a capacitance ratio of each of the respective pixels by changing a size of storage capacitor line.

CITATION LIST

- Patent Literature

[0010]

Patent Literature 1: JP 2001-296523 A

5 Patent Literature 2: JP 2007-25697 A

Patent Literature 3: JP 6-11733 A

Patent Literature 4: JP 2004-62146 A

Patent Literature 5: WO 2008/081624

10 SUMMARY OF INVENTION

- Technical Problem

[0011]

During the investigation of a liquid crystal display device including subsidiary pixels (hereinafter also referred to as picture elements) of a plurality of colors, the present inventors paid attention to a phenomenon in which, when thicknesses (cell gaps) of the liquid crystal layer are different between the picture elements, and when a white window screen is displayed on a halftone background for a long time and then a halftone solid screen is displayed, only the color in the portion corresponding to the white window is seen to be different from the color of the background portion.

[0012]

Figure 50 is a schematic view showing a state when a white window is displayed on the halftone background, and Figure 51 is a schematic view showing a state of the halftone solid display when the white window is eliminated. As shown in Figure 50 and Figure 51, in the state of the halftone solid display, image sticking due to the display before the deletion of the white window occurs in the region in which the white window was displayed.

[0013]

The present inventors made various investigations about the cause of occurrence of such phenomenon and found out that the image sticking occurs in the display because the cell gaps

of the picture elements are different from each other and thereby the voltages applied to the liquid crystal layer are made different from each other, so that the liquid crystal capacitance is made different for each of the picture elements.

5 [0014]

When the liquid crystal capacitance is different for each picture element, the value of the electrostatic capacitance formed by the pixel electrode is also different for each of the picture elements. Figure 52 is a schematic view showing signal
10 waveforms of the drain voltages of two pixel electrodes arranged adjacently to each other.

[0015]

The signal waveforms shown on a left side of Figure 52 are waveforms associated with a picture element having a larger
15 cell gap, and the signal waveforms shown on a right side of Figure 52 are waveforms associated with a picture element having a smaller cell gap. As shown in Figure 52, an effective value of the drain voltage (V_d) is different for each picture element. This is because the magnitude of the pull-in voltage (ΔV_d) is
20 different between the picture elements, and because the polarity of drain voltages ($V_d(+)$, $V_d(-)$) is changed at each timing when the AC driving of the pixel electrode is performed. Since an opposed electrode is not formed for each of the pixels, an opposed voltage is set to a value common to all the pixels.
25 Therefore, a value of the optimum opposed voltage determined by the value of the drain voltage ($V_d(+)$, $V_d(-)$) after pull-in is set to a value different for each of the picture elements, and hence it is difficult that all the picture elements are suitably driven by an opposed voltage common to all the picture
30 elements.

[0016]

Further, according to the investigation of the present inventors, it was found that such variation in the optimum opposed voltage causes image sticking so as to affect the
35 display.

[0017]

The present invention has been made in view of the above described circumstances. An object of the present invention is to provide a liquid crystal display device which hardly
 5 causes image sticking even when the thicknesses of the liquid crystal layer for the picture elements are made different from each other.

- Solution to Problem

10 [0018]

In order to suppress the image sticking, the present inventors have investigated various methods for making the optimum opposed voltage equal between the picture elements, and paid attention to the fact that one of factors required to adjust
 15 the optimum opposed voltage is ΔV_d described above. When the values of ΔV_d of the picture elements are made close to each other, the optimum opposed voltages are also made equal to each other between the picture elements. The value of ΔV_d can be expressed as $\Delta V_d = \alpha \times V_{g^{p-p}}$. As shown in Figure 52 described
 20 above, the value of $V_{g^{p-p}}$ represents a gate voltage change at the time when the TFT is turned off. It is necessary to keep the value of $V_{g^{p-p}}$ at a fixed value to some extent, and hence it is necessary to adjust the value of α in order to change the value of ΔV_d . The value of α is expressed as $\alpha = C_{gd}/C_{gd}$
 25 $+ C_{sd} + C_{cs} + C_{lc}$. Reference character C_{gd} denotes parasitic capacitance between the gate and the drain, reference character C_{gd} denotes parasitic capacitance between the source and the drain, reference character C_{cs} denotes parasitic capacitance between the C_s and the drain, and reference character C_{lc}
 30 denotes liquid crystal capacitance. A total value of $C_{gd} + C_{sd} + C_{cs} + C_{lc}$, which is hereinafter also referred to as C_{pix} , represents the total capacitance (that is, pixel capacitance) connected to the drain of the TFT.

[0019]

35 As a result of an extensive investigation of means for

effectively adjusting the value of α , the present inventors paid attention to a channel region of TFT and found out that the balance of suitable pixel capacitance can be effectively adjusted by making the channel region of TFT different for each
5 of the picture elements. The channel region of TFT means a region in a semiconductor layer, which region forms a passage (channel) that enables current to flow between the source electrode and the drain electrode according to the charges supplied to the gate electrode.

10 [0020]

The size of the channel region of TFT has a large influence on the characteristics of TFT. As the width of the channel region is increased, the current characteristic becomes better, and a change in the size of the channel region exerts an influence
15 on all the capacitances C_{gd} , C_{sd} , C_{cs} , and C_{lc} which are components of C_{pix} .

[0021]

The present inventors found out that the optimum opposed voltage can be easily made equal between the picture elements
20 by connecting a TFT having a larger width of the channel region to a pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer, and thereby the generation of image sticking can be suppressed. As a result, the present inventors came up with an idea that, with such means,
25 the above described problems can be effectively solved, and reached the present invention.

[0022]

That is, the present invention is to provide a liquid crystal display device which includes a pair of substrates, and
30 a liquid crystal layer sandwiched between the pair of substrates, and in which a pixel is formed by picture elements of a plurality of colors, the liquid crystal display device being featured in that one of the pair of substrates includes scanning lines, signal lines, and storage capacitor lines, a thin film
35 transistor connected to each of the scanning line and the signal

line, and a pixel electrode connected to the thin film transistor, in that the other of the pair of substrates includes an opposed electrode, in that the liquid crystal layer includes a region having a larger thickness and a region having a smaller thickness in one pixel, in that the pixel electrode is arranged for each of the picture elements, and in that the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer among the plurality of pixel electrodes arranged in one pixel is connected to the thin film transistor having a larger channel width among the plurality of the thin film transistors arranged in the one pixel.

[0023]

The liquid crystal display device of the present invention includes a pair of substrates, and a liquid crystal layer sandwiched between the pair of substrates, and is configured such that a pixel is formed by picture elements of a plurality of colors. For example, one of the pair of substrates can be used as an array substrate, and the other of the pair of substrates can be used as a color filter substrate. The picture elements of the plurality of colors can be realized by color filters respectively arranged in correspondence with picture elements, and various display colors can be expressed by adjusting the balance of the respective colors.

[0024]

One of the pair of substrates includes scanning lines (hereinafter also referred to as gate bus lines), signal lines (hereinafter also referred to as source bus lines), storage capacitor lines (hereinafter also referred to as Cs bus lines), a thin film transistor (TFT) connected to each of the scanning lines and each of the signal lines, and a pixel electrode connected to the thin film transistor. The drain electrode of each of the TFTs is connected to the pixel electrode corresponding to the TFT. The gate electrode of each of the TFTs is connected to the gate bus line of each row. The source electrode of each of the TFTs is connected to the source bus

line of each column. A desired image can be obtained by supplying an image signal to the source bus line and by applying a voltage to the gate bus line at a predetermined timing.

[0025]

5 In the above-described configuration, it is necessary that the scanning line, the signal line, the storage capacitor line, the thin film transistor, and the pixel electrode are arranged respectively via insulating films, or the like, and at certain intervals so as to be electrically isolated from each
10 other. Further, the pixel electrode and the opposed electrode are arranged to be separated from each other via the liquid crystal layer. Therefore, a certain amount of electrostatic capacitance is formed between each of the lines and each of the electrodes, and between the electrodes. Specifically, the
15 scanning line and the pixel electrode form gate-drain capacitance (C_{gd}), the signal line and the pixel electrode form source-drain capacitance (C_{sd}), the storage capacitor line and the pixel electrode form a storage capacitance (C_{cs}), and the pixel electrode and the opposed electrode form liquid crystal
20 capacitance (C_{lc}).

[0026]

The other of the pair of substrates includes the opposed electrode. Since an electric field is formed between the pixel electrode and the opposed electrode, and since each of the pixel
25 electrodes is individually controlled by the thin film transistor, the orientation of the liquid crystal can be controlled for each of the picture elements, and thereby the whole screen can be precisely controlled.

[0027]

30 The liquid crystal layer has a region having a larger thickness and a region having a smaller thickness in one pixel. The light-control characteristics can be made different between the regions by making a thickness (cell gap) of the liquid crystal layer different for each region.

35 [0028]

The pixel electrode is arranged for each of the picture elements, and the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer among the plurality of pixel electrodes arranged in one pixel is connected to the thin film transistor having a larger channel width among the plurality of the thin film transistors arranged in the one pixel. The channel width does not mean the interval between the source electrode and the drain electrode (hereinafter also referred to as channel length) in plan view of a thin film transistor, but means the width of the region formed by the source electrode and the drain electrode which face each other. There is a correlation between the channel width and the value of pixel capacitance, and there is a correlation between the value of pixel capacitance and the value of cell gap. When a TFT having a larger channel width is connected to a pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer, and when a TFT having a smaller channel width is connected to a pixel electrode that overlaps a region having a larger thickness of the liquid crystal layer, the variation of the optimum opposed voltage between the picture elements can be suppressed on the basis of the characteristics of the TFTs.

[0029]

The configuration of the liquid crystal display device of the present invention is not especially limited as long as it essentially includes such components. Preferable embodiments of the liquid crystal display device of the present invention are mentioned in more detail below.

[0030]

It is preferred that the overlapping area of the scanning line and the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer is different from the overlapping area of the scanning line and the pixel electrode that overlaps a region having a larger thickness of the liquid crystal layer. Thereby, the value of the gate-drain

capacitance (C_{gd}) formed between the scanning line and the pixel electrode can be changed, and hence more suitable adjustment can be performed.

[0031]

5 It is preferred that the overlapping area of the signal line and the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer is different from the overlapping area of the signal line and the pixel electrode that overlaps a region having a larger thickness of the liquid
10 crystal layer. Thereby, the value of the source-drain capacitance (C_{sd}) formed between the signal line and the pixel electrode can be changed, and hence more suitable adjustment can be performed.

[0032]

15 It is preferred that the overlapping area of the storage capacitor line and the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer is different from the overlapping area of the storage capacitor line and the pixel electrode that overlaps a region having a
20 larger thickness of the liquid crystal layer. Thereby, the value of the storage capacitance (C_{cs}) formed between the storage capacitor line and the pixel electrode can be changed, and hence more suitable adjustment can be performed.

[0033]

25 It is preferred that the area of the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer is different from the area of the pixel electrode that overlaps a region having a larger thickness of the liquid crystal layer. Thereby, the value of the electrostatic
30 capacitance (C_{pix}) formed by the pixel electrode can be changed, and hence more suitable adjustment can be performed.

[0034]

 It is preferred that the scanning line and the pixel electrode form the gate-drain capacitance (C_{gd}), that the
35 signal line and the pixel electrode form the source-drain

capacitance (C_{sd}), that the storage capacitor line and the pixel electrode form the storage capacitance (C_{cs}), that the pixel electrode and the opposed electrode form the liquid crystal capacitance (C_{lc}), that the ratio of the gate-drain capacitance to the total of the gate-drain capacitance, the source-drain capacitance, the storage capacitance, and the liquid crystal capacitance (the value of this ratio of the gate-drain capacitance is hereinafter set as α) is different for each of the picture elements of the plurality of colors, and that, among the ratios of the gate-drain capacitance respectively obtained for the picture elements of the plurality of colors, the difference between the largest ratio of the gate-drain capacitance and the smallest ratio of the gate-drain capacitance is 10% or less of the smallest ratio of the gate-drain capacitance.

[0035]

It is preferred that the values of α of the picture elements in this case are close to each other. Further, when the values of α are set in the above-described range, the difference between the optimum opposed voltages of the respective picture elements can be eliminated so that the image sticking can be sufficiently suppressed.

[0036]

It is preferred that, in the one picture element, the value of the response coefficient (" $C_{pix(min)}/C_{pix(max)}$ ") obtained by calculating a ratio of the maximum value of the total of the gate-drain capacitance, the source-drain capacitance, and the storage capacitance, and the liquid crystal capacitance, with respect to the minimum value of the total of the gate-drain capacitance, the source-drain capacitance, and the storage capacitance, and the liquid crystal capacitance is different for each of the picture elements of the plurality of colors, and that, among the response coefficients respectively obtained for the picture elements of the plurality of colors, the difference between the largest response coefficient and the

smallest response coefficient is 5% or less of the smallest response coefficient.

[0037]

5 It is preferred that the pixel electrode is configured by a plurality of sub-pixel electrodes divided from each other in one picture element, that the thin film transistors are connected to the sub-pixel electrodes respectively, that the storage capacitor lines overlap the sub-pixel electrodes respectively, and that the liquid crystal display device
10 includes a driving circuit which inverts the polarity of the voltage of the storage capacitor line at regular time intervals. In the following, the method, in which one picture element is controlled by using a plurality of sub-pixel electrodes in this way, is also referred to as a multi-driving method. When a
15 plurality of sub-pixel electrodes are arranged in the same picture element and are respectively driven by different effective voltages, a state where different γ characteristics are mixed is formed, so that the visual angle dependency based on the γ characteristics can be eliminated. Further, an
20 increase in the number of extra lines can be prevented by driving the sub-pixel electrodes by the multi-driving method using the change in the voltage of the storage capacitor line.

[0038]

25 It is preferred that the ratio of the storage capacitance with respect to the total of the gate-drain capacitance, the source-drain capacitance, and the storage capacitance, and the liquid crystal capacitance (the value of this ratio of the storage capacitance is hereinafter set as K) is different for each of the picture elements of the plurality of colors, and
30 that, among the ratios of the storage capacitance respectively obtained for the picture elements of the plurality of colors, the difference between the largest ratio of the storage capacitance and the smallest ratio of the storage capacitance is 1.0% or less of the smallest ratio of the storage capacitance.

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- Advantageous Effects of Invention

[0039]

With the liquid crystal display device of the present invention, the variation in the optimum opposed voltage is adjusted between the picture elements, and hence the generation of image sticking can be suppressed.

BRIEF DESCRIPTION OF DRAWINGS

[0040]

- 10 [Figure 1] Figure 1 is a schematic plan view showing an arrangement configuration of pixel electrodes, TFTs and various lines of a liquid crystal display device of Embodiment 1.
- [Figure 2] Figure 2 is a schematic plan view when color filters in Embodiment 1 are arranged in a stripe shape.
- 15 [Figure 3] Figure 3 is a schematic plan view when the color filters in Embodiment 1 are arranged in a two-by-two matrix shape.
- [Figure 4] Figure 4 is an equivalent circuit diagram in the liquid crystal display device of Embodiment 1.
- 20 [Figure 5] Figure 5 is a schematic cross-sectional view of one example (Example 1) of the liquid crystal display device of Embodiment 1 wherein three color picture elements of red, green, and blue are used..
- [Figure 6] Figure 6 is a schematic cross-sectional view of one example (Example 1) of the liquid crystal display device of Embodiment 1 wherein four color picture elements of red, green, blue, and yellow are used.
- 25 [Figure 7] Figure 7 is a schematic plan view showing a first example of TFT in which a size of channel width is adjusted.
- 30 [Figure 8] Figure 8 is a schematic plan view showing a second example of TFT in which the size of channel width is adjusted.
- [Figure 9] Figure 9 is a schematic plan view (enlarged view) showing the second example of TFT in which the size of channel width is adjusted.
- 35 [Figure 10] Figure 10 is a schematic plan view showing a third

example of TFT in which the size of channel width is adjusted.

[Figure 11] Figure 11 is a schematic plan view (enlarged view) showing the third example of TFT in which the size of channel width is adjusted.

5 [Figure 12] Figure 12 is a schematic cross-sectional view of a liquid crystal display device of Example 2.

[Figure 13] Figure 13 is a schematic cross-sectional view of a liquid crystal display device of Example 3.

10 [Figure 14] Figure 14 is a schematic cross-sectional view of a liquid crystal display device of Example 4.

[Figure 15] Figure 15 is a schematic cross-sectional view of a liquid crystal display device of Example 5.

[Figure 16] Figure 16 is a schematic cross-sectional view of the liquid crystal display device of Example 5.

15 [Figure 17] Figure 17 is a schematic cross-sectional view of a liquid crystal display device of Example 6.

[Figure 18] Figure 18 is a schematic cross-sectional view of the liquid crystal display device of Example 6.

20 [Figure 19] Figure 19 is a schematic cross-sectional view of the liquid crystal display device of Example 6.

[Figure 20] Figure 20 is a schematic cross-sectional view of the liquid crystal display device of Example 6.

25 [Figure 21] Figure 21 is a schematic plan view of TFT showing an example in which the size of channel width is actually adjusted in Example 1.

[Figure 22] Figure 22 is a graph showing a relationship between the channel size ratio and the cell thickness ratio.

30 [Figure 23] Figure 23 is a schematic plan view showing a region in which the gate bus line and the drain electrode overlap each other in Embodiment 1.

[Figure 24] Figure 24 is a schematic plan view showing a region in which the gate bus line and the drain electrode overlap each other in Embodiment 1.

35 [Figure 25] Figure 25 is a schematic plan view showing a region in which the gate bus line and the drain electrode overlap each

other in Embodiment 1..

[Figure 26] Figure 26 shows an example of TFT in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted in the example of TFT shown in Figure 23, and shows a form in which the dimension d1 of the TFT shown in Figure 23 is changed.

[Figure 27] Figure 27 shows an example of TFT in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted in the example of TFT shown in Figure 23, and shows a form in which the dimension d1 of the TFT shown in Figure 23 is changed.

[Figure 28] Figure 28 shows an example of TFT in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted in the example of TFT shown in Figure 23, and shows a form in which the dimension d2 of the TFT shown in Figure 23 is changed.

[Figure 29] Figure 29 shows an example of TFT in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted in the example of TFT shown in Figure 23, and shows a form in which the dimension d2 of the TFT shown in Figure 23 is changed.

[Figure 30] Figure 30 shows an example of TFT in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted in the example of TFT shown in Figure 24, and shows a form in which the dimension d3 of the TFT shown in Figure 24 is changed.

[Figure 31] Figure 31 shows an example of TFT in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted in the example of TFT shown in Figure 24, and shows a form in which the dimension d4 of the TFT shown in Figure 24 is changed.

[Figure 32] Figure 32 shows an example of TFT in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted in the example of TFT shown in Figure 24, and shows a form in which the dimension d4 of the TFT shown in

Figure 24 is changed.

[Figure 33] Figure 33 is a schematic plan view showing a region in which the gate bus line and the pixel electrode overlap each other in Embodiment 1, and showing a form in which a normal gate bus line and a normal pixel electrode overlap each other.

[Figure 34] Figure 34 is a schematic plan view showing a region in which the gate bus line and the pixel electrode overlap each other in Embodiment 1, and showing an example in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted.

[Figure 35] Figure 35 is a schematic plan view showing a region in which the gate bus line and the pixel electrode overlap each other in Embodiment 1, and showing an example in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted.

[Figure 36] Figure 36 is a graph showing a relationship between the frame period and the applied voltage arrival rate.

[Figure 37] Figure 37 is a schematic view showing a display state when the influence of the difference in the response coefficient on the display was investigated.

[Figure 38] Figure 38 is a graph showing a suitable range of the response coefficient expressed by " $C_{\text{pix}}(\text{min}) / C_{\text{pix}}(\text{max})$."

[Figure 39] Figure 39 is a schematic plan view showing an arrangement configuration of pixel electrodes, TFTs and various lines of a liquid crystal display device of Embodiment 2.

[Figure 40] Figure 40 is an equivalent circuit diagram in the liquid crystal display device of Embodiment 2.

[Figure 41] Figure 41 shows signal waveforms when a multi-pixel drive is performed.

[Figure 42] Figure 42 is a schematic plan view showing a range in which the Cs bus line and the drain electrode having an expanded region in a part overlap each other in Embodiment 2.

[Figure 43] Figure 43 is a schematic plan view showing an example when the Cs capacitance is adjusted by the overlapping area of the pixel electrode and the Cs bus line.

[Figure 44] Figure 44 is a schematic plan view showing an example when the Cs capacitance is adjusted by the overlapping area of the pixel electrode and the Cs bus line.

5 [Figure 45] Figure 45 is a schematic plan view showing an example when the Cs capacitance is adjusted by the overlapping area of the pixel electrode and the Cs bus line.

[Figure 46] Figure 46 is a schematic plan view showing an example when the Cs capacitance is adjusted by the overlapping area of the pixel electrode and the Cs bus line.

10 [Figure 47] Figure 47 is a waveform chart showing the Cs amplitude when a multi-drive is performed.

[Figure 48] Figure 48 is a schematic plan view showing a form in which picture elements of three colors are used in Embodiment 3.

15 [Figure 49] Figure 49 is a schematic plan view showing a form in which picture elements of four colors are used in Embodiment 3.

[Figure 50] Figure 50 is a schematic view showing a state in which a white window is displayed on a halftone background.

20 [Figure 51] Figure 51 is a schematic view showing a state of a halftone solid display after the white window is eliminated.

[Figure 52] Figure 52 is a schematic view showing signal waveforms of the drain voltages of two pixel electrodes arranged adjacently to each other.

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DESCRIPTION OF EMBODIMENTS

[0041]

The present invention will be mentioned in more detail referring to the drawings in the following embodiments, but is
30 not limited to these embodiments.

[0042]

Embodiment 1

Figure 1 is a schematic plan view showing an arrangement configuration of pixel electrodes, TFTs and various lines of
35 a liquid crystal display device of Embodiment 1. As shown in

Figure 1, one pixel electrode is arranged for one picture element in Embodiment 1. Also, one pixel is configured by a plurality of picture elements, and hence each of the picture elements is individually controlled to control each pixel, and to further control the whole display of the liquid crystal display device.

[0043]

A liquid crystal display device of Embodiment 1 includes gate bus lines 11 extending in the row direction (lateral direction), and source bus lines 12 extending in the column direction (longitudinal direction). Further, the liquid crystal display device includes a TFT 14 connected to both of the gate bus line 11 and the source bus line 12. The TFT 14 is also connected to a pixel electrode 15. Further, the liquid crystal display device includes a Cs bus line 13 which overlaps at least a part of the pixel electrode 15. For example, as shown in Figure 1, the Cs bus line 13 is formed to extend in the row direction so as to cross the center portion of the pixel electrode 15.

[0044]

In Embodiment 1, a kind of color filter is arranged for one picture element. Examples of the kinds, the number and the arrangement order of colors of the picture elements configuring a pixel include, but are not limited in particular to, combinations, such as RGB, RGBY and RGBW. The color of a picture element is determined by a color filter. Examples of arrangement forms of color filters include a stripe arrangement, as shown in Figure 2, in which color filters are formed to extend in the longitudinal direction regardless of the boundary of the pixel electrode, and a two-by-two matrix arrangement having four colors, as shown in Figure 3, in which two color filters are arranged in each of the row direction and the column direction.

[0045]

Figure 4 is an equivalent circuit diagram in the liquid

crystal display device of Embodiment 1. In Embodiment 1, a circuit pattern is formed for each picture element (subsidiary pixel), and hence circuit patterns for two picture elements are illustrated in Figure 4.

5 [0046]

A liquid crystal capacitance C_{lc} is formed by the pixel electrode and the opposed electrode which are arranged to face each other via the liquid crystal layer. The value of C_{lc} is dependent on an effective voltage (V) applied to the liquid
10 crystal layer by the pair of electrodes. A storage capacitance C_{cs} is formed by the pixel electrode and the C_s bus line (storage capacitor line) which are arranged to face each other via an insulating layer. A gate-drain capacitance C_{gd} is formed by the pixel electrode and the gate bus line (scanning line) which
15 are arranged to face each other via an insulating layer. A source-drain capacitance C_{sd} is formed by the pixel electrode and the source bus line (signal line) which are arranged to face each other via an insulating layer.

[0047]

20 The TFT (thin film transistor) includes a semiconductor layer made of silicon, and the like, and three electrodes of a gate electrode, a source electrode, and a drain electrode. The pixel electrode is connected to the drain electrode of the TFT. The gate electrode of the TFT is connected to the gate
25 bus line, and the source electrode of the TFT is connected to the source bus line.

[0048]

A scanning signal supplied to the gate bus line in a pulse-like manner at a predetermined timing is applied to each
30 of the TFTs at a predetermined timing (by line-sequential writing, every other line writing, two-line simultaneous writing, or the like). Then, an image signal supplied from the source bus line is applied to the pixel electrode connected to the TFT which is turned on for a predetermined time period by
35 the input of the scanning signal.

[0049]

The image signal having a predetermined level, which is written in the liquid crystal layer for each of the picture elements, is held, for a predetermined time period, between the pixel electrode with the image signal applied thereto and the opposed electrode facing the pixel electrode. After the image signal is applied, the image signal held between the pixel electrode and the opposed electrode may leak, but in order to prevent this leakage, the storage capacitance C_{cs} is formed in parallel with the liquid crystal capacitance C_{lc} formed between the pixel electrode and the opposed electrode.

[0050]

Each of Figure 5 and Figure 6 is a schematic cross-sectional view of one example (Example 1) of the liquid crystal display device of Embodiment 1. Figure 5 shows a case where three color picture elements of red, green, and blue are used, whereas Figure 6 shows a case where four color picture elements of red, green, blue, and yellow are used.

[0051]

As shown in Figure 5 and Figure 6, the liquid crystal layer 1 of the liquid crystal display device of Example 1 is placed between a pair of substrates, that is, an active matrix substrate 2 and a color filter substrate 3. The active matrix substrate 2 has a pixel electrode 41, and the color filter substrate 3 has an opposed electrode 42. Further, the color filter substrate 3 has color filters 31 of a plurality of colors, and one pixel includes three or four colors. In the example shown in Figure 5, three color filters of red 31R, green 31G, and blue 31B are used. In the example shown in Figure 6, four color filters red 31R, green 31G, blue 31B, and yellow 31Y are used.

[0052]

As shown in Figure 5 and Figure 6, the cell gaps (thicknesses of the liquid crystal layer) of the picture elements are different from each other in Example 1. In the

examples shown in Figure 5 and Figure 6, the thickness (cell gap) of the liquid crystal layer 1 corresponding to the blue picture element is formed thinner than the thicknesses (cell gaps) of the liquid crystal layer 1 corresponding to the other picture elements. Thereby, a better viewing angle characteristic can be achieved in comparison with the case where the thickness of the liquid crystal layer is the same for all the picture elements.

[0053]

10 In Example 1, a voltage applied to the inside of the liquid crystal layer 1 through the electrodes 41 and 42 of the pair of substrates is different for each picture element. This is because the thickness of the liquid crystal layer 1 corresponding to the blue picture element is set thinner than the thicknesses of the liquid crystal layer 1 corresponding to the other picture elements in Example 1. A liquid crystal capacitance formed in the blue picture element is larger than those formed in the other picture elements. Thus, in the case of forming a multi-gap configuration, an optimum opposed voltage is different for each picture element.

[0054]

25 In Example 1, the balance between the values of $\alpha = C_{gd}/(C_{gd} + C_{sd} + C_{cs} + C_{lc})$ of the picture elements is adjusted using the channel width of the TFT. Specifically, a TFT having a smaller cell gap is arranged for the pixel electrode having a larger area. Therefore, the channel width of the TFT arranged for the blue picture element is larger than the channel width of the TFT arranged for the red picture element, and is larger than the channel width of the TFT arranged for the green picture element.

[0055]

35 Thereby, it is possible to easily adjust, for each of the picture elements, the balance of the gate-drain capacitance (C_{gd}) formed between the gate bus line and the pixel electrode, the source-drain capacitance (C_{sd}) formed between the source

bus line and the pixel electrode, the storage capacitance (Ccs) formed between the Cs bus line and the pixel electrode, and the liquid crystal capacitance (Clc) formed between the pixel electrode and the opposed electrode.

5 [0056]

Figure 7 to Figure 11 are schematic plan views respectively showing examples of means for making the channel width d (d1 to d8) of the TFT different between the picture elements in Example 1. As shown in Figure 7 to Figure 11, a TFT 14 is connected to each of a gate bus line 11 and a source bus line 12. The TFT 14 includes, as components, a semiconductor layer formed of silicon, and the like, a source electrode 22 extended from a part of the source bus line 12, a drain electrode 23 that supplies an image signal from the source bus line 12 to the pixel electrode via the semiconductor layer, and a gate electrode that is a region of the gate bus line 11, which region overlaps the semiconductor layer.

15 [0057]

The drain electrode 23 is extended toward the center of the picture element, and is formed to have a certain spread. A contact hole 24 is formed through the insulating layer formed on a portion 23a having the fixed spread, and the drain electrode 23 and the pixel electrode are electrically connected to each other via the contact hole 24.

20 [0058]

The portion 23a of the drain electrode 23, which portion has the certain spread, can form a storage capacitance together with the Cs bus line arranged under the portion 23a via the insulating layer.

25 [0059]

The semiconductor layer provided in the TFT 14 overlaps both of the source electrode 22 and the drain electrode 23. The region of the semiconductor layer, which region overlaps the source electrode 22, is a source region, and the region of the semiconductor layer, which region overlaps the drain electrode

23, is a drain region. Further, the region of the semiconductor layer, which region does not overlap both of the source electrode 22 and the drain electrode 23, and which region is located between the source electrode 22 and the drain electrode 23 in plan view, is a channel region 21. Therefore, the semiconductor layer 21 has three regions of the source region, the channel region 21, and the drain region.

[0060]

The channel region 21, which overlaps the gate bus line 11, enables an image signal to be supplied from the source electrode 22 to the drain electrode 23 only when a scanning signal is inputted into the gate bus line 11. Since the length (distance between the source electrode 22 and the drain electrode 23) of the channel region 21 is determined to be an appropriate value to some extent, it is not preferred to change the length of the channel region 21 for each of the picture elements, but the width d of the channel region 21 can be adjusted. When the width d of the channel region 21 with respect to the length of the channel region 21 is expanded, the conductivity of the TFT 14 can be further improved. Therefore, in Example 1, the channel width d in the blue picture element is formed to be larger than the channel width d in the red and green picture elements.

[0061]

Thereby, the value of the gate-drain capacitance (C_{gd}) formed between the gate bus line and the pixel electrode is changed, and hence, by the use of this change, the values of the optimum opposed voltages in the picture elements are respectively adjusted so as to become close to each other.

[0062]

Figure 7 is a schematic plan view showing a first example of TFT in which the size of channel width is adjusted. The channel region 21 of the TFT in Figure 7 is formed between the drain electrode 23 and the source electrode 22, and has the channel width of d_1 . The value of α can be adjusted by changing

the size of d_1 for each of the picture elements.

[0063]

Figure 8 and Figure 9 are schematic plan views showing a second example of TFT in which the size of channel width is adjusted. The channel width d_2 of the TFT 14 in Figure 8 is formed not only between the drain electrode 23 and the source electrode 22 but also between the drain electrode 23 and a part of the source bus line 12, and has the channel width of d_2 . In this case, as shown in Figure 9, the channel width d_2 of the TFT 14 becomes the length of the sum of the length d_3 of the portion facing the source bus line 12 and the length d_4 of the portion facing the source electrode 22. The value of α can be adjusted by changing the size of d_2 for each of the picture elements.

15 [0064]

Figure 10 and Figure 11 are schematic plan views showing a third example of TFT in which the size of channel width is adjusted. In the TFT 14 shown in Figure 10, the source electrode 22 extended from a part of the source bus line 12 is branched in the middle so as to have a shape surrounding the distal end of the drain electrode 23. In this case, as shown in Figure 11, the channel width d_5 of the TFT 14 becomes the length of the sum of the lengths d_6 and d_8 of the portions in parallel with the gate bus line 11, and the length d_7 of the portion in parallel with the source bus line 12. The value of α can be adjusted by changing the size of d_5 for each of the picture elements.

[0065]

In Example 1, it is preferred that the values of α of the picture elements are close to each other. Specifically, it is preferred that the ratio of the values of α of the picture elements, which ratio is expressed as: "(maximum value of α - minimum value of α) / (minimum of value of α)," is 10% or less. When the values of α of the picture elements are set close to each other, the variation in ΔV_d which is the pull-in voltage

is suppressed, and thereby the optimum opposed voltages between the picture elements are made close to each other. Thereby, the possibility of occurrence of image sticking can be greatly reduced. The value of α is obtained by the expression: $\alpha =$
 5 Cgd/Cpix(Cgd + Csd + Ccs + Clc). For this reason, the parameters included in the expression need to be adjusted, in order to adjust the balance between the values of α of the picture elements. The balance between the values of α of the picture elements can be effectively adjusted by adjusting the channel
 10 width.

[0066]

The following will describe in detail a plurality of combination for making cell gaps different between picture elements referring to examples.

15 [0067]

Example 2

Figure 12 is a schematic cross-sectional view of a liquid crystal display device of Example 2. As shown in Figure 12, three color filters of red (R), green (G) and blue (B) are used
 20 in Example 2. The arrangement order of the colors is not limited in particular. In Example 2, the cell gap of the red (R) picture element is larger than the cell gaps of the green (G) picture element and of the blue (B) picture element. The cell gap of the green (G) picture element is the same as the cell gap of
 25 the blue (B) picture element.

[0068]

Example 3

Figure 13 is a schematic cross-sectional view of a liquid crystal display device of Example 3. As shown in Figure 13,
 30 three color filters of red (R), green (G) and blue (B) are used in Example 3. The arrangement order of the colors is not limited in particular. In Example 3, the cell gap of the red (R) picture element is larger than the cell gap of the green (G) picture element, and the cell gap of the green (G) picture element is
 35 larger than the cell gap of the blue (B) picture element.

[0069]

Example 4

Figure 14 is a schematic cross-sectional view of a liquid crystal display device of Example 4. As shown in Figure 14, four color filters of red (R), green (G), blue (B) and yellow (Y) are used in Example 4. The arrangement order of the colors is not limited in particular. In Example 4, the cell gap of the green (G) picture element is the same as the cell gap of the yellow (Y) picture element, and the cell gap of the red (R) picture element is the same as the cell gap of the blue (B) picture element. The cell gaps of the green (G) and yellow (Y) picture elements are larger than the cell gaps of the red (R) and blue (B) picture elements.

[0070]

Example 5

Each of Figure 15 and Figure 16 is a schematic cross-sectional view of a liquid crystal display device of Example 5. As shown in Figure 15 and Figure 16, four color filters of red (R), green (G), blue (B) and yellow (Y) are used in Example 5. The arrangement order of the colors is not limited in particular. In Example 5, the cell gap of the green (G) picture element is the same as the cell gap of the yellow (Y) picture element. The cell gap of the red (R) picture element is smaller than any of the cell gap of the green (G) picture element and the cell gap of the yellow (Y) picture element. Further, the cell gap of the blue (B) picture element is smaller than any of the cell gap of the green (G) picture element and the cell gap of the yellow (Y) picture element.

[0071]

In the relationship between the cell gaps of the red and blue picture elements, a form is assumed in which one of the cell gaps of the red and blue picture elements is larger than the other. When the cell gap of the red picture element is larger than the cell gap of the blue picture element, the color filters are configured as shown in Figure 15, while when the

cell gap of the blue picture element is larger than the cell gap of the red picture element, the color filters are configured as shown in Figure 16.

[0072]

5 Example 6

Each of Figure 17 to Figure 20 is a schematic cross-sectional view of a liquid crystal display device of Example 6. As shown in Figure 17 to Figure 20, four color filters of red (R), green (G), blue (B) and yellow (Y) are used
10 in Example 6. The arrangement order of the colors is not limited in particular. In Example 6, the cell gap of the red (R) picture element is smaller than any of the cell gap of the green (G) picture element and the cell gap of the yellow (Y) picture element. Also, the cell gap of the blue (B) picture element
15 is smaller than any of the cell gap of the green (G) picture element and the cell gap of the yellow (Y) picture element. In the relationship between the cell gaps of the green and yellow picture elements, a form is assumed in which one of the cell gaps of the green and yellow picture elements is larger than
20 the other. Also, in the relationship between the cell gaps of the red and blue picture elements, a form is assumed in which one of the cell gaps of the red and blue picture elements is larger than the other. Figure 17 shows a form in which the cell gaps of the picture elements are set as yellow > green > blue
25 > red, and Figure 18 shows a form in which the cell gaps of the picture elements are set as green > yellow > blue > red. Figure 19 shows a form in which the cell gaps of the picture elements are set as yellow > green > red > blue, and Figure 20 shows a form in which the cell gaps of the picture elements are set as
30 green > yellow > red > blue.

[0073]

In the following, there will be described an example in which, in the liquid crystal display device of Example 1, the value of α is adjusted by actually adjusting the channel width.
35 Figure 21 is a schematic plan view showing an example in which

the channel width of the TFT in Example 1 is actually adjusted.
[0074]

As shown in Figure 21, the TFT 14 includes the source electrode 22 extended from a part of the source bus line 12, a gate electrode 25 extended from a part of the gate bus line 11, and the drain electrode 23 connected to the pixel electrode. The TFT 14 includes a semiconductor layer at a position at which the TFT 14 overlaps the gate electrode 25. A part of the semiconductor layer overlaps a part of each of the source electrodes 22 and the drain electrodes 23. Further, the other part of the semiconductor layer, which part overlaps neither the source electrode 22 nor the drain electrode 23, and which part is sandwiched between the source electrode 22 and the drain electrode 23 is the channel region 21. Here, the widths of the respective channel regions 21 of the semiconductor layer are set to be different, but the distance between the source electrode 22 and the drain electrode 23 is set to be the same.
[0075]

In the example shown in Figure 21, the drain electrode 23 has a linear shape extended in the direction in parallel with the source bus line 12. Further, the source electrode 22 has, in plan view, an opening opened toward the side opposite to the side of the gate bus line 11, and has a shape configured to surround the distal end of the drain electrode 23.

[0076]

The width of the drain electrode 23 is denoted by reference character c , and the interval between the drain electrode 23 and the source electrode 22 in the direction in parallel with the gate bus line 11 is denoted by reference character d . The distance between the drain electrode 23 and the source electrode 22 in the direction in parallel with the source bus line 12 is denoted by reference character e . The length of the portion of the source electrode 22, which portion faces the drain electrode 23 and which portion is in parallel with the gate bus line 11, is denoted by reference character

a. The length obtained by subtracting the length of the portion of the source electrode 22 which portion is in parallel with the source bus line 12 from the length of the portion of the gate electrode 25, which portion is in parallel with the source bus line 12, is denoted by reference character b.

[0077]

In the liquid crystal display device of Example 1, in the case where, in three color picture elements having multi-gap configuration, the cell gaps of the picture elements were set as "blue" > "red = green," the deviation between the values of α of the picture elements could be suppressed to 0.81% by adjusting the values of a to e between the picture elements as shown in Table 1 described below. Further, ΔV_d in the blue picture element was 1.619 V, and ΔV_d in each of the red and green picture elements was 1.606 V. The difference between the maximum and minimum values of ΔV_d was 13 mV. Therefore, according to the above-described design, it was possible to obtain a liquid crystal display device in which the generation of image sticking is suppressed by sufficiently adjusting the optimum opposed voltages between the picture elements. Note that the ratio of the cell gap of each of the picture elements was set as "blue": "red": "green" = 1.1:1.0:1.0.

[0078]

[Table 1]

	Picture element B (μm)	Picture elements R and G (μm)
a	15.00	16.50
b	6.0	6.0
c	4.0	4.0
d	4.0	4.0
e	4.0	4.0

[0079]

The following Table 2 is a table showing permissible ranges of the deviation of the value of α when the difference of the value of ΔV_d is assumed to be less than 100 mV in the liquid crystal display device of the present invention. It is

seen that, when the difference between the values of ΔV_d is 100 mV or less, the image sticking can be easily improved, and that, when the difference between the values of ΔV_d is 50 mV or less, the image sticking can be more surely improved.

5 [0080]
[Table 2]

ΔV_d (V)	V_{gpp} (V)	α	Deviation of α (%)
1	41	0.02439	10.0
1.1	41	0.02683	
1.5	41	0.03659	6.7
1.6	41	0.03902	
2.0	41	0.04878	5.0
2.1	41	0.05122	
3.0	41	0.07317	3.3
3.1	41	0.07561	

[0081]

As shown in Table 2 described above, the deviation of the value of α was 10.0% at the time when the value of ΔV_d was set to 1.0 V, and when the difference between the values of ΔV_d was set to 100 mV. The deviation of the value of α was 6.7% at the time when the value of ΔV_d was set to 1.5 V, and when the difference between the values of ΔV_d was set to 100 mV. The deviation of the value of α was 5.0% at the time when the value of ΔV_d was set to 2.0 V, and when the difference between the values of ΔV_d was set to 100 mV. The deviation of the value of α was 3.3% at the time when the value of ΔV_d was set to 3.0 V, and when the difference between the values of ΔV_d was set to 100 mV.

[0082]

It was found to be preferred that, in a normal liquid crystal display device, the value of ΔV_d is set in the range of 1.5 to 3.0 V, and that, under this condition, the deviation of the value of α is set in the range of 7.0% or less. Further, it is conceivable that the value of ΔV_d may be set as $\Delta V_d = 1$ V or less in future, and it was found to be preferred that, in this case, the deviation of the value of α is set in the

range of 10.0% or less.

[0083]

Note that, in the case where a normal liquid crystal display device, in which the cell gap and the channel width of each of picture elements were set to be the same, was investigated as a comparison example, the deviation of the value of α was 8.0% (between picture elements R), and ΔV_d was 183 mV (between picture elements R).

[0084]

Further, when a relationship between the channel size and the cell thickness ratio in the liquid crystal display device of the present invention was investigated, data as shown in Table 3 and Figure 22 were obtained. Figure 22 is a graph showing a relationship between the channel size ratio and the cell thickness ratio.

[0085]

[Table 3]

Channel size ratio	Cell thickness ratio
0.800	1.176
0.873	1.118
0.927	1.059
1.000	1.000
1.073	0.941
1.164	0.882
1.273	0.824

[0086]

The variation of the value of α is suppressed between the picture elements by changing the values of a to e of the TFT channel according to Table 3 and along the straight line shown in Figure 22, so that a liquid crystal display device with little image sticking can be obtained.

[0087]

Further, the difference in the lengths of the source electrode and the drain electrode between the TFTs shown in Figure 6 to Figure 8 actually also influences the overlapping area of the gate bus line and the drain electrode as shown in

Figure 23 to Figure 25. Each of Figure 23 to Figure 25 is a schematic plan view showing a region in which the gate bus line and the drain electrode overlap each other in Embodiment 1. Since, as the overlapping area of the gate bus line 11 and the drain electrode 23 is increased, the value of the gate-drain capacitance (Cgd) is more changed, the balance between all the values of α of the picture elements can be adjusted also by adjusting the overlapping area of the gate bus line 11 and the drain electrode 23 in addition to the adjustment of the channel length.

[0088]

As described above, in Embodiment 1, the balance between the values of $\alpha = C_{gd}/(C_{gd} + C_{sd} + C_{cs} + C_{lc})$ of the picture elements is adjusted. As can be seen from the above-described expression, it is effective to adjust the gate-drain capacitance Cgd in order to adjust the balance between the values of α of the picture elements.

[0089]

Actually, the difference in the overlapping area of the drain electrode and the gate bus line in the TFT also influences the gate-drain capacitance (Cgd) formed between the gate bus line and the drain electrode. Since, as the overlapping area of the gate bus line and the drain electrode is increased, the value of the gate-drain capacitance (Cgd) is increased, the balance between the values of α of the picture elements can be adjusted also by adjusting the overlapping area of the gate bus line and the drain electrode.

[0090]

Each of Figure 26 to Figure 29 shows an example of TFT in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted in the example of TFT shown in Figure 23. Each of Figure 26 and Figure 27 shows a form in which the channel width d1 of the TFT shown in Figure 23 is changed. In Figure 26, a projecting section is provided in a planar shape in a part of the overlapping region of the drain

electrode 23 and the gate bus line 11. In Figure 27, the channel width d1 as a whole is increased. Each of Figure 28 and Figure 29 shows a form in which the dimension d2 of the TFT shown in Figure 23 is changed. In Figure 28, the length of d2 is increased. In Figure 29, the shape of the drain electrode 23 is maintained as it is, but a projecting section is provided in a planar shape in a part of the gate bus line 11, so that the overlapping region of the drain electrode 23 and the gate bus line 11 is increased.

10 [0091]

Each of Figure 30 to Figure 32 shows an example of TFT in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted in the example of TFT shown in Figure 24. Figure 30 shows a form in which the dimension d3 of the TFT shown in Figure 24 is changed. In Figure 31, the width d3 as a whole is increased. Each of Figure 31 and Figure 32 shows a form in which the dimension d4 of the TFT shown in Figure 24 is changed. In Figure 31, the length of d4 is increased. In Figure 32, the shape of the drain electrode 23 is maintained as it is, but a projecting section is provided in a planar shape in a part of the gate bus line 11, so that the overlapping region of the drain electrode 23 and the gate bus line 11 is increased.

[0092]

25 The gate-drain capacitance (Cgd) formed between the gate bus line and the drain electrode is also formed in the region in which the gate bus line and the pixel electrode directly overlap each other. Since, as the overlapping area of the gate bus line and the pixel electrode is increased, the value of the gate-drain capacitance (Cgd) is increased, the balance between the values of α of the picture elements can be adjusted also by adjusting the overlapping area of the gate bus line and the pixel electrode.

[0093]

35 Each of Figure 33 to Figure 35 is a schematic plan view

showing a region in which the gate bus line and the pixel electrode overlap each other in Embodiment 1. Figure 33 shows a form in which a normal gate-bus line and a normal pixel electrode overlap each other, and in which the end portion of the pixel electrode 15 is linearly formed, and the gate bus line 11 is extended in parallel with the end portion of the pixel electrode 15. Each of Figure 34 and Figure 35 shows an example in which the size of the overlapping area of the gate bus line and the drain electrode is adjusted. In Figure 34, a projecting section is provided in a planar shape in a part of the pixel electrode 15 in the overlapping region of the pixel electrode 15 and the gate bus line 11. Therefore, as a result, the overlapping region of the pixel electrode 15 and the gate bus line 11 is expanded. In Figure 35, a recessed section (cut-out section) is provided in a planar shape in a part of the pixel electrode 15 in the overlapping region of the pixel electrode 15 and the gate bus line 11. Therefore, as a result, the overlapping region of the pixel electrode 15 and the gate bus line 11 is narrowed.

[0094]

In this way, when the overlapping area of the drain electrode and the gate bus line, and the overlapping area of the pixel electrode and the gate bus line are adjusted, the value of each electrostatic capacitance formed in association with the pixel electrode can be adjusted for each of the picture elements, and thereby the value of the opposed voltage can be more optimized for each of the picture elements.

[0095]

In Embodiment 1, it is preferred that the value of "Cpix(min)/Cpix(max)" (hereinafter also referred to as response coefficient) is set to be the same between the picture elements. Reference character Cpix(min) denotes pixel capacitance at the time of black display, and reference character Cpix(max) denotes pixel capacitance at the time of white display. The response coefficient denoted as

"Cpix(min)/Cpix(max)" is one of the indicators of the response characteristics of liquid crystal. When the values of the response coefficient are different between the picture elements, the response characteristic becomes different for each of the colors, and hence desired chromaticness may not be obtained.
[0096]

The response coefficient "Cpix(min)/Cpix(max)" can be adjusted by performing, as described above, the adjustment of the TFT channel width, the adjustment of the overlapping area of the gate bus line and the drain electrode, the adjustment of the overlapping area of the pixel electrode and the gate bus line, the adjustment of the overlapping area of the pixel electrode and the Cs bus line, and the like.
[0097]

Figure 36 is a graph showing a relationship between the frame period and the applied voltage arrival rate. Figure 37 is a schematic view showing a display state when the influence of the difference in the response coefficient on the display was investigated. As shown in Figure 36, in a liquid crystal display device currently in use, the liquid crystal cannot respond within one frame, and hence the liquid crystal display device is designed to obtain desired transmissivity through two stages. For example, as shown in Figure 37, when a display is performed such that a white quadrangle is displayed on the black background and then the white quadrangle is moved from the right to the left, the picture elements located at the left end of the quadrangle are made to newly respond in each frame. As a result, only the picture element having a small response coefficient is slow in response, and thereby the intensity of the colors of the other picture elements becomes large so that the chromaticness is changed.

[0098]

To cope with this, the change in the chromaticness can be suppressed by making the values of response coefficients of the picture elements close to each other. Figure 38 is a graph

showing a suitable range of the response coefficient expressed by "Cpix(min)/Cpix(max)." The value of the response coefficient at the time when the arrival rate is 0.9 is 0.78, and the preferred range of the response coefficient is in a range of 0.78 ± 0.04 in which the arrival rate difference is within 5%.

[0099]

Embodiment 2

Figure 39 is a schematic plan view showing an arrangement configuration of pixel electrodes, TFTs, and various lines of a liquid crystal display device of Embodiment 2. As shown in Figure 39, in Embodiment 2, two pixel electrodes (hereinafter also referred to as sub-pixel electrodes) are arranged for one picture element. Further, one pixel is configured by a plurality of picture elements, and each of the picture elements is individually controlled to control each pixel and to further control the whole display of the liquid crystal display device.

[0100]

The liquid crystal display device of Embodiment 2 includes the gate bus line 11 extended in the row direction (lateral direction), and the source bus line 12 extended in the column direction (longitudinal direction). Further, the liquid crystal display device includes a first TFT 14a and a second TFT 14b each of which are connected to both the gate bus line 11 and the source bus line 12. The first TFT 14a is connected to a first sub-pixel electrode 15a, and the second TFT 14b is connected to a second sub-pixel electrode 15b. Further, the liquid crystal display device of Embodiment 2 includes a first Cs bus line 13a which overlaps at least a part of the first sub-pixel electrode 15a, and a second Cs bus line 13b which overlaps at least a part of the second sub-pixel electrode 15b. As shown in Figure 39, each of the first Cs bus line 13a and the second Cs bus line 13b is extended in the row direction so as to cross the center of each of the sub-pixel electrodes 15a and 15b.

[0101]

In Embodiment 2, a kind of color filter is arranged for one picture element. Examples of the kinds, the number and the arrangement order of colors of the picture elements configuring a pixel include, but are not limited in particular to, combinations, such as RGB, RGBY and RGBW. The color of a picture element is determined by a color filter. Examples of arrangement forms of color filters include a stripe arrangement, as shown in Figure 2, in which color filters are formed to be extended in the longitudinal direction regardless of the boundary of the pixel electrode, and a two-by-two matrix arrangement, as shown in Figure 3, in which two of four color filters are arranged in each of the row direction and the column direction.

15 [0102]

In Embodiment 2, each of the two sub-pixel electrodes forms sub-pixel capacitance having a different capacitance value. Examples of the method for making the sub-pixel capacitance different for each of the sub-pixel electrodes include (1) a method of supplying a signal voltage from each of different source bus lines, and (2) a method of adjusting the signal voltage by changing the voltage of the Cs bus line. The TFTs are connected to the sub-pixel electrodes respectively. Each of the TFTs is connected to the same gate bus line, and hence the two sub-pixels are simultaneously controlled at the timing at which a scanning signal is supplied to the gate bus line.

[0103]

Figure 40 is an equivalent circuit diagram in the liquid crystal display device of Embodiment 2. In Embodiment 2, a circuit pattern is formed for each of the sub-pixels, and the circuit patterns of the two sub-pixels are shown in Figure 40. The sub-pixel electrodes respectively form Clc1 and Clc2 between themselves and the opposed electrode via the liquid crystal layer. The sub-pixel electrodes respectively form

Ccs1 and Ccs2b between themselves and the Cs bus line. Further, each of the sub-pixel electrodes is connected to the drain electrode of each of the TFTs, and the driving of each of the sub-pixels is controlled by each of the TFTs.

5 [0104]

The liquid crystal capacitance Clc is formed by the pixel electrode and the opposed electrode which are arranged to face each other via the liquid crystal layer. The value of Clc is dependent on the effective voltage (V) applied to the liquid
10 crystal layer by the pair of electrodes. The storage capacitance Ccs is formed by the pixel electrode and the Cs bus line (storage capacitor line) which are arranged to face each other via an insulating layer. The gate-drain capacitance Cgd is formed by the pixel electrode and the gate bus line (scanning
15 line) which are arranged to face each other via an insulating layer. The source-drain capacitance Csd is formed by the pixel electrode and the source bus line (signal line) which are arranged to face each other via an insulating layer.

[0105]

20 The method for driving each of the sub-pixel electrodes by using the TFTs, and the basic configuration in Embodiment 2 are the same as those in Embodiment 1.

[0106]

In the following, a method for performing the multi-pixel
25 drive by changing the voltage of the Cs bus line will be described in detail. Figure 41 shows signal waveforms when the multi-pixel drive is performed.

[0107]

When a voltage Vg is changed from VgL to VgH at the time
30 of T1, the first TFT 14a and the second TFT 14b are simultaneously switched to conductive state (on-state), so that a voltage Vs is transmitted to each of the first and second sub-pixel electrodes 15a and 15b from the source bus line 12, and is charged to the first and second sub-pixel electrodes 15a and 15b.

35 Similarly, the first and second Cs bus lines 13a and 13b

respectively overlapping the first and second sub-pixel electrodes 15a and 15b are also charged by the voltage supplied from the source bus line 12.

[0108]

5 Next, when the voltage V_g of the gate bus line 11 is changed from V_{gH} to V_{gL} at the time of T_2 , the first TFT 14a and the second TFT 14b are simultaneously switched to non-conductive state (off-state), the first and second sub-pixel electrodes 15a and 15b, and the first and second Cs bus lines 13a and 13b
10 are all electrically insulated from the source bus line 12. Note that, immediately after this change, each of the voltages V_{lc1} and V_{lc2} of the first and second sub-pixel electrodes 15a and 15b is reduced by substantially a same voltage ΔV_d as follows, due to the pull-in phenomenon caused by the influence of the
15 parasitic capacitance, and the like, associated with the first TFT 14a and the second TFT 14b.

$$V_{lc1} = V_s - \Delta V_d$$

$$V_{lc2} = V_s - \Delta V_d$$

Further, at this time, the voltage V_{cs1} and V_{cs2} of the first
20 and second Cs bus lines 13a and 13b become as follows.

$$V_{cs1} = V_{com} - V_{ad}$$

$$V_{cs2} = V_{com} + V_{ad}$$

[0109]

At the time of T_3 , the voltage V_{cs1} of the first Cs bus
25 line 13a is changed from $V_{com} - V_{ad}$ to $V_{com} + V_{ad}$, and the voltage V_{cs2} of the second Cs bus line 13b is changed from $V_{com} + V_{ad}$ to $V_{com} - V_{ad}$. According to these voltage changes in the first Cs bus line 13a and the second Cs bus line 13b, the voltages V_{lc1} and V_{lc2} of the first and second sub-pixel electrodes 15a
30 and 15b are changed as follows.

$$V_{lc1} = V_s - \Delta V_d + 2 \times V_{ad} \times C_{cs1} / (C_{lc1} + C_{cs1})$$

$$V_{lc2} = V_s - \Delta V_d - 2 \times V_{ad} \times C_{cs2} / (C_{lc2} + C_{cs2})$$

[0110]

At the time of T_4 , V_{cs1} is changed from $V_{com} + V_{ad}$ to V_{com}
35 - V_{ad} , and V_{cs2} is changed from $V_{com} - V_{ad}$ to $V_{com} + V_{ad}$. Before

the time T4, the voltages Vlc1 and Vlc2 are respectively expressed as follows.

$$Vlc1 = V_s - \Delta V_d + 2 \times V_{ad} \times C_{cs1} / (Clc1 + C_{cs1})$$

$$Vlc2 = V_s - \Delta V_d - 2 \times V_{ad} \times C_{cs2} / (Clc2 + C_{cs2})$$

- 5 At the time of T4, also, the voltages Vlc1 and Vlc2 are respectively changed to the voltages expressed as follows.

$$Vlc1 = V_s - \Delta V_d$$

$$Vlc2 = V_s - \Delta V_d$$

[0111]

- 10 At the time of T5, Vcs1 is changed from Vcom - Vad to Vcom + Vad, and Vcs2 is changed from Vcom + Vad to Vcom - Vad. Before the time of T5, the voltages Vlc1 and Vlc2 expressed as follows.

$$Vlc1 = V_s - \Delta V_d$$

$$Vlc2 = V_s - \Delta V_d$$

- 15 At the time of T5, also, the voltages Vlc1 and Vlc2 are respectively changed to the voltages expressed as follows

$$Vlc1 = V_s - \Delta V_d + 2 \times V_{ad} \times C_{cs1} / (Clc1 + C_{cs1})$$

$$Vlc2 = V_s - \Delta V_d - 2 \times V_{ad} \times C_{cs2} / (Clc2 + C_{cs2})$$

[0112]

- 20 For each interval of an integer multiple of horizontal writing time 1H, the voltages Vcs1, Vcs2, Vlc1, and Vlc2 respectively repeat the changes caused at the time of T4 and T5. Whether the repeating interval of the changes caused at the time of T4 and T5 is set to be equal to the horizontal writing time 1H, or set to twice, 3 times, or more of the horizontal writing time 1H, may be suitably determined in view of the driving method (for example, polarity inversion drive) and displaying conditions (flickering, roughness of display, and the like) of the liquid crystal display device. This repetition
- 25 is continued until the time equivalent to T1 is subsequently reached. Therefore, the effective values of voltages Vlca and Vlcb of the sub-pixel electrodes become as follows, respectively.

$$Vlca = V_s - \Delta V_d + V_{ad} \times C_{cs1} / (Clc1 + C_{cs1})$$

- 35 $Vlcb = V_s - \Delta V_d - V_{ad} \times C_{cs2} / (Clc2 + C_{cs2})$

[0113]

Therefore, the effective voltages V1 and V2, which are respectively applied to the liquid crystal layer by the first and second sub-pixel electrodes 15a and 15b, are set to values different from each other and expressed as follows.

$$V1 = Vlc1 - Vcom$$

$$V2 = Vlc2 - Vcom$$

That is, the effective voltages V1 and V2 are expressed as follows.

$$V1 = Vs - \Delta Vd + Vad \times Ccs1 / (Clc1 + Ccs1) - Vcom$$

$$V2 = Vs - \Delta Vd - Vad \times Ccs2 / (Clc2 + Ccs2) - Vcom$$

[0114]

Under the above-described premises, the adjustment of the optimum opposed voltages between the respective picture elements in Embodiment 2 will be described in detail below.

[0115]

In Embodiment 2, similarly to Embodiment 1, the balance between the values of $\alpha = Cgd / (Cgd + Csd + Ccs + Clc)$ of the picture elements is adjusted by using the channel width of TFT.

Further, the balance between the values of $\alpha = Cgd / (Cgd + Csd + Ccs + Clc)$ of the picture elements is also supplementarily adjusted by using the gate-drain overlapping area. As the methods for adjusting the balance between the values of α in Embodiment 2, methods similar to the methods described in Embodiment 1 can be used.

[0116]

In Embodiment 2, it is preferred that K-values are set to be equal to each other between the sub-pixels. When the K-values are set to be equal to each other, the values of the electrostatic capacitance formed by the respective sub-pixel electrodes are made uniform, and the adjustment between the sub-pixels is more suitably performed. Thereby, it is possible to further reduce the possibility that the value of α is varied between the picture elements. The K-value is expressed as $K = Ccs / Cpix(Cgd + Csd + Ccs + Clc)$. Therefore, the adjustment

of C_{cs} is effective to adjust the balance between the K -values of the picture elements.

[0117]

Figure 42 is a schematic plan view showing a range in which the expanded portions of the C_s bus line and of the drain electrode overlap each other in Embodiment 2. As shown in Figure 42, the C_s bus line 13 has an expanded region in a part thereof, and the drain electrode 23 also has an expanded region in a part thereof. These expanded regions are isolated from each other via an insulating layer, but overlap each other in plan view so as to form the storage capacitance C_{cs} . The value of storage capacitance C_{cs} depends on the overlapping area of these expanded regions, and hence the storage capacitance C_{cs} having a suitable capacitance value can be formed by adjusting the size of the expanded region for each of the sub-pixels and by adjusting the overlapping degree between the expanded regions. Note that, in Figure 42, the expanded portion of the C_s bus line 13 is larger than the expanded portion 23a of the drain electrode 23 on both longitudinal and lateral sides.

[0118]

The longitudinal length and the lateral length of the expanded portion 23a of the drain electrode 23 are denoted by reference characters of d and f , respectively. Further, the longitudinal length and the lateral length of the expanded portion of the C_s bus line 13 are denoted by reference characters of e and g , respectively.

[0119]

On the same one side of the expanded portions, the distance between the longitudinal side of the expanded portion of the C_s bus line 13 and the longitudinal side of the expanded portion 23a of the drain electrode 23 is set to a . That is, the expanded portion 23a of the drain electrode 23 is formed on the laterally inner side of the expanded portion of the C_s bus line 13 by the distance a from each of the longitudinal sides of the expanded portion of the C_s bus line 13. Therefore, the

expression $g = f + 2a$ is established.

[0120]

On the same one side of the expanded portions, the distance between the lateral side of the expanded portion of the Cs bus line 13 and the lateral side of the expanded portion of the drain electrode 23 is set to b . That is, the expanded portion of the drain electrode 23 is formed on the longitudinally inner side of the expanded portion of the Cs bus line 13 by the distance b from each of the lateral sides of the expanded portion of the Cs bus line 13. Therefore, the expression $e = d + 2b$ is established.

[0121]

In such case, when, in the four color picture elements having different cell gaps, the pitch widths were set as "red = blue" < "green = yellow," the deviation between the K-values (maximum value - minimum value) of the picture elements could be suppressed to 0.10% by respectively adjusting the values of a to g between the picture elements as shown in Table 4 described below. Note that the ratio of the cell gaps of the respective picture elements was set as "red":"blue":"green":"yellow" = 1:1:1.4:1.4.

[0122]

[Table 4]

	Picture elements R and B (μm)	Picture elements G and Y (μm)
a	17.0	14.0
b	3.0	2.0
c	226.0	154.25
d	29.0	36.0
e	35.0	40.0
f	157.0	91.25
g	191.0	119.25

25 [0123]

Each of Figure 43 to Figure 46 is a schematic plan view showing an example when the storage capacitance C_s is adjusted by the overlapping area of the pixel electrode and the C_s bus line. Figure 43 shows a form in which the upper side of the

pixel electrode 15 overlaps a part of the Cs bus line 13. The value of the storage capacitance C_{cs} can be adjusted by adjusting the values of a and b in Figure 43. Figure 44 shows a form in which the Cs bus line 13 crosses the center of the pixel electrode 15, and in which the whole in the width direction of the Cs bus line 13 overlaps the pixel electrode 15. The value of the storage capacitance C_{cs} can be adjusted by adjusting the values of c and d in Figure 44. Figure 45 shows a form in which the upper side of the pixel electrode 15 overlaps the Cs bus line 13, and in which an extending section of the Cs bus line 13 is added along with the left side of the pixel electrode 15. The value of the storage capacitance C_{cs} can be adjusted by adjusting the values of a to d in Figure 45. Figure 46 shows a form in which the upper side of the pixel electrode 15 overlaps the Cs bus line 13, and in which an extending section of the Cs bus line 13 is added so as to cross the center of the pixel electrode 15. The value of C_{cs} can be adjusted by adjusting the values of e to f in Figure 46.

[0124]

The values of the storage capacitance C_{cs} between the sub-pixels are made close to each other by performing these adjustments between the sub-pixels, so that the K-values within a suitable range can be obtained.

[0125]

Figure 47 is a waveform chart showing the amplitude of the voltage of the CS bus line 13 when the multi-drive is performed. The voltage value ΔV_{cs} in Figure 47 is expressed as $\Delta V_{cs} = K \times V_{cs}^{p-p}$. It is preferred that the magnitude of the pull-in voltage is uniform between the sub-pixels and specifically is 10 mV or less. Thereby, the optimum opposed voltages of the sub-pixels can be made close to each other. Since the value of V_{cs}^{p-p} is substantially fixed, it is preferred that the value of ΔV_{cs} is adjusted by adjusting the value of K.

[0126]

Table 5 described below is a table showing a permissible range of deviation of the value of K when the value of ΔV_{cs} is assumed to be 10 mV or less. In the conventional liquid crystal display device in which the areas of the picture elements are not made different from each other, the value of K is set in the range of 0.43 to 0.54, and hence the investigation was performed on the basis of this range.

[0127]

[Table 5]

K	Deviation of K (%)	V _{cs}	ΔV_{cs}	Deviation of ΔV_{cs} (mV)
0.54	0.74	1.92	1.04	7.7
0.544		1.92	1.04	
0.43	0.93	2.41	1.04	9.6
0.434		2.41	1.04	

[0128]

As shown in Table 5 described above, when the value of K was set to 0.54 and when the deviation of the value of K was set to 0.74%, the deviation of the value of ΔV_{cs} could be suppressed to 7.7 mV. Further, when the value of K was set to 0.43 and when the deviation of the value of K was set to 0.93%, the deviation of the value of ΔV_{cs} could be suppressed to 9.6 mV. Therefore, the target range of the value of K is 1.0% or less.

[0129]

Embodiment 3

Each of Figure 48 and Figure 49 is a schematic plan view showing an arrangement configuration of color filters in Embodiment 3.

In Embodiment 3, three color picture elements of red, green and blue, or four color picture elements of red, green, blue and yellow are used, and one pixel is configured by a combination of these picture elements. In Embodiment 3, the areas of the picture elements are different from each other.

[0130]

Figure 48 is a schematic plan view showing a form in which picture elements of three colors are used in Embodiment 3, wherein the area of the picture element green (G) among the picture elements is larger than the area of the picture element red (R) and the area of the picture element blue (B). Difference in the area between the picture elements leads to difference in the value of pixel capacitance. Based on this, the optimum opposed voltage between the picture elements can be adjusted. In addition, higher transmissivity can be achieved by increasing the ratio of green and thereby making the pitch widths of red, green, and blue different from each other in comparison with the case where the ratios of the colors are the same.

[0131]

Figure 49 is a schematic plan view showing a form in which picture elements of four colors are used in Embodiment 3, wherein any of the area of the picture element red (R) and the area of the picture element blue (B) among the picture elements is larger than any of the area of the picture element green (G) and the area of the picture element yellow (Y). Difference in the area between the picture elements leads to difference in the value of pixel capacitance. Based on this, the optimum opposed voltage between the picture elements can be adjusted. In addition, wider color reproducibility can be achieved by increasing the ratio of red and blue whereas decreasing the ratio of green and yellow, and thereby making the pitch widths of red, green, blue, and yellow different from each other in comparison with the case where the ratios of the colors are the same.

[0132]

In Embodiment 3, the optimum opposed voltage is adjusted between the picture elements by using the channel width of the TFT, and the optimum opposed voltage is further adjusted by adjusting the picture element area between the picture elements. Thereby, it is possible to obtain a liquid crystal display

device in which the variation of the value of α is further suppressed between the picture elements and thereby the image sticking is reduced.

[0133]

- 5 The present application claims priority to Patent Application No. 2010-019563 filed in Japan on January 29, 2010 under the Paris Convention and provisions of national law in a designated State, the entire contents of which are hereby incorporated by reference.

10

REFERENCE SIGNS LIST

[0134]

- 1: Liquid crystal layer
- 2: Active matrix substrate
- 15 3: Color filter substrate
- 11: Gate bus line (scanning line)
- 12: Source bus line (signal line)
- 13: Cs bus line (storage capacitor line)
- 13a: First Cs bus line
- 20 13b: Second Cs bus line
- 14: TFT (Thin film transistor)
- 14a: First TFT
- 14b: Second TFT
- 15: Pixel electrode
- 25 15a: First sub-pixel electrode
- 15b: Second sub-pixel electrode
- 21: Channel region
- 22: Source electrode
- 23: Drain electrode
- 30 23a: Expanded section of drain electrode
- 24: Contact hole
- 25: Gate electrode
- 31: Color filter
- 31R: Color filter (red)
- 35 31G: Color filter (green)

31B: Color filter (blue)
31Y: Color filter (yellow)
41: Pixel electrode
42: Opposed electrode

CLAIMS

Claim 1. A liquid crystal display device which includes a pair of substrates, and a liquid crystal layer sandwiched between the pair of substrates, and is configured such that a pixel is formed by picture elements of a plurality of colors, wherein one of the pair of substrates includes scanning lines, signal lines, and storage capacitor lines, a thin film transistor connected to each of the scanning line and the signal line, and a pixel electrode connected to the thin film transistor;

the other of the pair of substrates includes an opposed electrode;

the liquid crystal layer includes a region having a larger thickness and a region having a smaller thickness in one pixel, whereby each of the regions corresponds to any of the picture elements (or the pixel electrodes);

the pixel electrode is arranged for each of the picture elements; and

the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer among the plurality of pixel electrodes arranged in one pixel is connected to the thin film transistor with a larger channel width among the plurality of thin film transistors arranged in the one pixel;

wherein the overlapping area of the signal line and the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer is different from the overlapping area of the signal line and the pixel electrode that overlaps a region having a larger thickness of the liquid crystal layer.

Claim 2. The liquid crystal display device according to claim 1,

wherein the overlapping area of the scanning line and the

pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer is different from the overlapping area of the scanning line and the pixel electrode that overlaps a region having a larger thickness of the liquid
5 crystal layer.

Claim 3. The liquid crystal display device according to claims 1 or 2,

10 wherein the overlapping area of the storage capacitor line and the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer is different from the overlapping area of the storage capacitor line and the pixel electrode that overlaps a region having a larger thickness of
15 the liquid crystal layer.

Claim 4. The liquid crystal display device according to any one of claims 1 to 3,

20 wherein an area of the pixel electrode that overlaps a region having a smaller thickness of the liquid crystal layer is different from an area of the pixel electrode that overlaps a region having a larger thickness of the liquid crystal layer.

Claim 5. The liquid crystal display device according to
25 any one of claims 1 to 4,

wherein the scanning line and the pixel electrode form gate-drain capacitance;

the signal line and the pixel electrode form source-drain capacitance;

30 the storage capacitor line and the pixel electrode form storage capacitance;

the pixel electrode and the opposed electrode form liquid crystal capacitance;

35 a ratio of the gate-drain capacitance to a total of the gate-drain capacitance, the source-drain capacitance, the

storage capacitance, and the liquid crystal capacitance is different for each of the picture elements of the plurality of colors; and

5 a difference between a largest ratio of the gate-drain capacitance and a smallest ratio of the gate-drain capacitance, among the ratios of the gate-drain capacitance respectively obtained for the picture elements of the plurality of colors, is 10% or less of the smallest ratio of the gate-drain capacitance.

10

Claim 6. The liquid crystal display device according to any one of claims 1 to 5,

wherein the scanning line and the pixel electrode form gate-drain capacitance;

15 the signal line and the pixel electrode form source-drain capacitance;

the storage capacitor line and the pixel electrode form storage capacitance;

20 the pixel electrode and the opposed electrode form liquid crystal capacitance;

wherein a value of a response coefficient obtained by calculating, in the one picture element, a ratio of the maximum value of the total of the gate-drain capacitance, the source-drain capacitance, the storage capacitance, and the liquid crystal capacitance, with respect to the minimum value of the total of the gate-drain capacitance, the source-drain capacitance, the storage capacitance, and the liquid crystal capacitance is different for each of the picture elements of the plurality of colors; and

30 the difference between the largest response coefficient and the smallest response coefficient, among the response coefficients respectively obtained for the picture elements of the plurality of colors, is 5% or less of the smallest response coefficient.

35

Claim 7. The liquid crystal display device according to any one of claims 1 to 6,

wherein the pixel electrode is configured by a plurality of sub-pixel electrodes divided from each other in one picture element;

the thin film transistors are connected to the sub-pixel electrodes respectively;

the storage capacitor lines overlap the sub-pixel electrodes respectively; and

the liquid crystal display device includes a driving circuit which inverts a polarity of a voltage of the storage capacitor line at regular time intervals.

Claim 8. The liquid crystal display device according to claim 7,

wherein the scanning line and the pixel electrode form gate-drain capacitance;

the signal line and the pixel electrode form source-drain capacitance;

the storage capacitor line and the pixel electrode form storage capacitance;

the pixel electrode and the opposed electrode form liquid crystal capacitance;

wherein a ratio of the storage capacitance with respect to the total of the gate-drain capacitance, the source-drain capacitance, the storage capacitance, and the liquid crystal capacitance is different for each of the picture elements of the plurality of colors; and

the difference between the largest ratio of the storage capacitance and the smallest ratio of the storage capacitance, among the ratios of the storage capacitance respectively obtained for the picture elements of the plurality of colors, is 1.0% or less of the smallest ratio of the storage capacitance.