WHAT IS CLAIMED IS:

1. An operating method of a memory device including a plurality of banks, the operating method comprising:

receiving a write command, and data and an address corresponding to the write command;

decoding the write command; and

responsive to a result of the decoding indicating that the write command corresponds to a multiple write command, together writing the same data in two or more banks using an internal address generating operation that is based on the received address, wherein the two or more banks are selected from a subset of the plurality of banks that are less than a total number of the plurality of banks.

2. The operating method of claim 1, further comprising, responsive to the result of the decoding indicating that the write command corresponds to a standard write command, writing the data in one bank indicated by the received address.

3. The operating method of claim 1 or claim 2, wherein the memory device communicates the write command with a memory controller using command/address signals including fields CA0, CA1, CA2, CA3, CA4, and CA5 based on a low power double data rate (LPDDR) communication interface.

4. The operating method of claim 3, wherein the write command comprises a first portion of a first write command synchronized with a rising edge of a clock signal and a second portion of the first write command synchronized with a falling edge of the clock signal, and

wherein the multiple write command is determined by decoding information about at least one of the fields CA0, CA1, CA2, CA3, CA4, and CA5 of the first portion of the first write command synchronized with the rising edge of the clock signal.

5. The operating method of claim 4, wherein the multiple write command is determined by further decoding information about at least one of the fields CA0, CA1, CA2,

CA3, CA4, and CA5 of the second portion of the first write command synchronized with the falling edge of the clock signal.

6. The operating method of claim 5, wherein, responsive to the CA3 field of the second portion of the first write command synchronized with the falling edge of the clock signal having a first logic value, the write command is determined as the multiple write command, and

wherein, responsive to the CA3 field of the second portion of the first write command having a second logic value, the write command is determined as a command other than the multiple write command.

7. The operating method of any one of claims 4 to 6, wherein the write command further comprises a second Column Access Strobe (CAS) command synchronized with a subsequent cycle of the clock signal after the first write command, and

wherein the two or more banks in which the same data is written are based on at least one of a plurality of fields included in the second CAS command.

8. The operating method of any one of claims 1 to 7, wherein the memory device further comprises an address generator configured to store a plurality of internal addresses corresponding to the received address, and

wherein the operating method further comprises generating two or more internal addresses for selecting the two or more banks, based on a value of the received address.

9. The operating method of any one of claims 1 to 8, wherein the two or more banks are selected based on at least one don’t care bit of a bank address included in the received address.

10. The operating method of claim 9, wherein a location of the at least one don’t care bit of the bank address is configured to vary based on at least one field of the write command.

11. The operating method of any one of claims 1 to 10, wherein, in response to the multiple write command, the same data is written at a same column position of the two or more banks.

12. An operating method of a memory controller for controlling a memory device including a plurality of banks, the operating method comprising:

receiving an initialization request for the memory device from a host;

in response to the initialization request, generating a multiple write command to together write same initialization data in two or more banks of the memory device using an internal address generating operation that is based on an address received, wherein the two or more banks of the memory device are selected from a subset of the plurality of banks that are less than a total number of the plurality of banks;

transferring the multiple write command to the memory device; and

transferring, to the memory device, a standard write command and the address indicating a position of a bank of the memory device in which data are to be written,

wherein the multiple write command and the standard write command transferred to the memory device respectively comprise a plurality of fields,

wherein a first combination of the plurality of fields of the multiple write command is different than a second combination of the plurality of fields of the standard write command.

13. The operating method of claim 12, wherein the initialization data is set in the memory device, and

wherein the multiple write command is transferred to the memory device without transferring the initialization data.

14. The operating method of claim 12 or claim 13, further comprising transferring a clock signal synchronized with the multiple write command,

wherein the write command comprises a first portion of a first write command synchronized with a rising edge of the clock signal and a second portion of the first write command synchronized with a falling edge of the clock signal.

15. The operating method of claim 14, wherein the memory controller communicates the first write command with the memory device using command/address

signals including fields CA0, CA1, CA2, CA3, CA4, and CA5 based on a low power double data rate (LPDDR) communication interface, and

wherein an operation of the multiple write command is based on fields CA0, CA1, CA2, CA3, and CA4 of the first portion of the first write command synchronized with the rising edge of the clock signal and field CA3 of the second portion of the first write command synchronized with the falling edge of the clock signal.

16. The operating method of claim 14 or claim 15, wherein the multiple write command further comprises a second Column Access Strobe (CAS) command synchronized with a subsequent cycle of the clock signal after the first write command, and

wherein at least one field of the second CAS command comprises information about the two or more banks of the memory device in which the same initialization data is together written.

17. The operating method of any one of claims 12 to 16, further comprising:

receiving a plurality of data and a plurality of addresses according to one or more write requests from the host;

checking the received plurality of data and the received plurality of addresses to determine whether a same data is requested to be written in the two or more banks of the memory device;

transferring the multiple write command to the memory device, based on a result of the determination; and

transferring bank addresses, indicating the two or more banks corresponding to the multiple write command, to the memory device according to the received plurality of addresses.

18. A memory device comprising:

a memory cell array including a plurality of banks;

a command decoder configured to decode a write command and an address received from a memory controller to control a write operation on the plurality of banks; and

a bank controller block configured to select one or more of the plurality of banks in which data is to be written,

wherein, responsive to the command decoder decoding the write command as a standard write command, the data is written in one bank of the plurality of banks indicated by the address received from the memory controller, and

wherein, responsive to the command decoder decoding the write command as a multiple write command, the data is together written in two or more banks of the plurality of banks of the memory cell array through an internal bank selecting operation to generate an internal address that is based on the address received, wherein the two or more banks are selected from a subset of the plurality of banks that are less than a total number of the plurality of banks.

19. The memory device of claim 18, further comprising an internal address generator configured to generate the internal address for selecting the two or more banks, based on the address received from the memory controller.

20. The memory device of claim 18 or claim 19, further comprising a storage circuit configured to store initialization data,

wherein, in an initialization operation of an electronic system including the memory device, the memory device receives the multiple write command from the memory controller, and

wherein, in response to the multiple write command, the initialization data is accessed from the storage circuit and is written simultaneously in the two or more banks of the plurality of banks of the memory cell array.