[0026] FIG. 11A and FIG. 11B illustrate a refresh operation of a memory device including one plane.

[0027] FIG. 12 is a diagram for specifically describing the refresh operation according to an embodiment of the present disclosure.

[0028] FIG. 13 is a diagram for specifically describing the refresh operation according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0029] Various embodiments of the present invention are described below in more detail with reference to the accompanying drawings. We note, however, that the present invention may be embodied in different forms and variations, and should not be construed as being limited to the embodiments set forth herein. Rather, the described embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the present invention to those skilled in the art to which this invention pertains. Throughout the disclosure, like reference numerals refer to like parts throughout the various figures and embodiments of the present invention. It is noted that reference to "an embodiment" does not necessarily mean only one embodiment, and different references to "an embodiment" are not necessarily to the same embodiment(s).

[0030] It will be further understood that when an element is referred to as being "connected to", or "coupled to" another element, it may be directly on, connected to, or coupled to the other element, or one or

more intervening elements may be present. In addition, it will also be understood that when an element is referred to as being "between" two elements, it may be the only element between the two elements, or one or more intervening elements may also be present.

[0031] It will be further understood that the terms "comprises," "comprising," "includes," and "including" when used in this specification, specify the presence of the stated elements and do not preclude the presence or addition of one or more other elements. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0032] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the present invention.

[0033] A data storage device and an operating method thereof are described below with reference to the accompanying drawings through various embodiments.

[0034] FIG. 1 is a block diagram illustrating an exemplary configuration of a memory system 10 including a data storage device 200 according to an embodiment of the present disclosure.

[0035] Referring to FIG. 1, the memory system 10 may include a host device 100 and the data storage device 200.

[0036] The host device 100 may include devices such as a mobile phone, an MP3 player, a laptop computer, a desktop computer, a game player, a TV and an in-vehicle infotainment system, but the host device 100 is not specifically limited any of these devices or systems.

[0037] The host device 100 may include a host controller 120 for controlling the general operations of the host device 100. While not shown in FIG. 1, the host device 100 may include an interface for interfacing with the data storage device 200. The host controller 120 may transmit various commands to the data storage device 200. For example, the host controller 120 may transmit commands, such as a read command and a program command, to the data storage device 200. The host controller 120 may transmit information on an address to read or program to the data storage device 200.

[0038] In the present embodiment, the host controller 120 may transmit a refresh scan command RS CMD and a refresh operation command RO CMD to the data storage device 200.

[0039] The refresh scan command RS CMD may be a command for checking whether it is necessary to perform a refresh operation for a nonvolatile memory device 210 of the data storage device 200 and the degree of urgency. If the refresh scan command RS CMD is transmitted from the host device 100, a device controller 220 of the data storage device 200 may perform a refresh scan operation of checking the number of failed bits, a read count and an erase count for each of the plurality of memory blocks (one of which is shown) in the nonvolatile memory device 210. For of convenience, a passive refresh scan operation performed in the data storage device 200 in response to the refresh scan command RS CMD transmitted from the host device 100 will be referred to as a first refresh scan operation, and a passive refresh operation performed based on a first refresh scan result will be

referred to as a first refresh operation.

[0040] The host controller 120 may receive a refresh scan result RS Response transmitted from the data storage device 200, and may transmit the refresh operation command RO CMD to the data storage device 200 based on the refresh scan result RS Response. The host controller 120 may transmit the refresh operation command RO CMD when the data storage device 200 is not used by a user or when a refresh request is inputted from the user, based on the refresh scan result RS Response transmitted from the data storage device 200.

[0041] The data storage device 200 may store data to be accessed by the host device 100. The data storage device 200 may be configured as any one of various kinds of storage devices depending on a transmission protocol with the host device 100. For example, the data storage device 200 may be configured as any one of a solid state drive, a multimedia card in the form of an MMC, an eMMC, an RS-MMC and a micro-MMC, a secure digital card in the form of an SD, a mini-SD and a micro-SD, a universal serial bus (USB) storage device, a universal flash storage (UFS) device, a Personal Computer Memory Card International Association (PCMCIA) card type storage device, a peripheral component interconnection (PCI) card type storage device, a PCI express (PCI-E) card type storage device, a compact flash (CF) card, a smart media card, a memory stick, and the like.

[0042] The data storage device 200 may be manufactured as any one of various package types. For example, the data storage device 200 may be manufactured as any one of a package-on-package (POP),

a system-in-package (SIP), a system-on-chip (SOC), a multi-chip package (MCP), a chip-on-board (COB), a wafer-level fabricated package (WFP) and a wafer-level stack package (WSP).

[0043] The data storage device 200 may include the nonvolatile memory device 210 and the device controller 220.

[0044] The nonvolatile memory device 210 may operate as the storage medium of the data storage device 200. The nonvolatile memory device 210 may be configured by any one of various types of nonvolatile memory devices such as a NAND flash memory device, a NOR flash memory device, a ferroelectric random access memory (FRAM) using a ferroelectric capacitor, a magnetic random access memory (MRAM) using a tunneling magneto-resistive (TMR) layer, a phase change random access memory (PRAM) using a chalcogenide alloy, and a resistive random access memory (RERAM) using a transition metal compound, depending on memory cells.

[0045] The nonvolatile memory device 210 may include a memory cell array (not shown) which has a plurality of memory cells respectively disposed at regions where a plurality of bit lines and a plurality of word lines intersect with each other. The memory cell array may include a plurality of memory blocks, and each of the plurality of memory blocks may include a plurality of pages.

[0046] Each memory cell of the memory cell array may be a single level cell (SLC) storing one bit, a multi-level cell (MLC) capable of storing 2-bit data, a triple level cell (TLC) capable of storing 3-bit data or a quad level cell (QLC) capable of storing 4-bit data. The memory

cell array may include single level cells, multi-level cells, triple level cells and/or quad level cells. For example, the memory cell array may include memory cells of a 2-dimensional horizontal structure or memory cells of a 3-dimensional vertical structure.

[0047] A read operation and a program operation for the nonvolatile memory device 210 may be performed on a unit such as a page, and an erase operation may be performed on a unit such as a memory block.

[0048] The device controller 220 may include a host interface 221, a processor 223, a RAM 225, an error correction code (ECC) circuit 227 and a memory interface 229.

[0049] The host interface 221 may interface the host device 100 and the data storage device 200. For example, the host interface 221 may communicate with the host device 100 by using any one among standard transmission protocols such as universal serial bus (USB), universal flash storage (UFS), multimedia card (MMC), parallel advanced technology attachment (PATA), serial advanced technology attachment (SATA), small computer system interface (SCSI), serial attached SCSI (SAS), peripheral component interconnection (PCI) and PCI express (PCI-E) protocols.

[0050] The processor 223 may be configured by a micro control unit (MCU) or a central processing unit (CPU). The processor 223 may process the command received from the host device 100. In order to process the command received from the host device 100, the processor 223 may drive an instruction or algorithm of a code type, that is, a

software, loaded in the RAM 225, and may control internal function blocks and the nonvolatile memory device 210.

[0051] The RAM 225 may be configured by a random access memory such as a dynamic random access memory (DRAM) or a static random access memory (SRAM). The RAM 225 may store a software to be driven by the processor 223. Also, the RAM 225 may store data necessary for the driving of the software (for example, metadata). Namely, the RAM 225 may operate as the working memory of the processor 223.

[0052] The RAM 225 may temporarily store data to be transmitted from the host device 100 to the nonvolatile memory device 210 or data to be transmitted from the nonvolatile memory device 210 to the host device 100. In other words, the RAM 225 may operate as a data buffer memory or a data cache memory.

[0053] The ECC circuit 227 may perform an ECC encoding operation of generating the parity data of data to be transmitted from the host device 100 to the nonvolatile memory device 210. The ECC circuit 227 may perform an ECC decoding operation of detecting and correcting an error for the data read out from the nonvolatile memory device 210, based on corresponding parity data. When the number of error bits in the data read out from the nonvolatile memory device 210 is equal to or less than a set or predetermined number of bits (for example, error correction capability), the ECC circuit 227 may correct the detected error bits.

[0054] The memory interface 229 may control the nonvolatile

memory device 210 according to the control of the processor 223. The memory interface 229 may also be referred to as a memory controller. The memory interface 229 may provide control signals to the nonvolatile memory device 210. The control signals may include a command, an address and the like, for controlling the nonvolatile memory device 210. The memory interface 229 may provide data to the nonvolatile memory device 210 or may be provided with data from the nonvolatile memory device 210. The memory interface 229 may be coupled with the nonvolatile memory device 210 through a channel CH including one or more signal lines.

[0055] The processor 223 may perform refresh operations such as garbage collection, wear leveling and read reclaim to improve the operation performance of the nonvolatile memory device 210. For convenience, an active refresh scan operation of determining, by the device controller 220 of the data storage device 200, whether it is necessary to perform a refresh operation will be referred to as a second refresh scan operation, and an active refresh operation to be performed based on a second refresh scan result will be referred to as a second refresh operation.

[0056] That is to say, the processor 223 of the device controller 220 of the data storage device 200 according to the present embodiment may perform the passive refresh scan operation and the passive refresh operation in response to the refresh scan command RS CMD and the refresh operation command RO CMD transmitted from the host device 100 or perform the active refresh scan operation and the active

refresh operation according to a set or predetermined condition in the absence of the refresh scan command RS CMD and the refresh operation command RO CMD respectively.

[0057] In the present embodiment, a read reclaim operation and a wear leveling operation among refresh operations will be described as examples, but the same principle may be applied to other kinds of refresh operations.

[0058] The memory cells of the nonvolatile memory device 210 may wear out as a result of erase operations and program operations being performed repeatedly. Worn-out memory cells may cause failures in the memory device 210 (for example, physical defects). Wear-leveling is an operation of leveling the program-erase counts of respective memory blocks, that is, an operation of causing all the memory blocks in the nonvolatile memory device 210 to have similar wear levels, to prevent any memory block from being worn out faster than the other memory blocks. Wear-leveling may be performed by moving the data stored in a memory block of which the program-erase count has reached a set or predetermined threshold count, to a memory block which has a program-erase count lower than the threshold count.

[0059] The data stored in each of the memory blocks of the nonvolatile memory device 210 may be influenced by read disturbance each time a read operation is performed for each of the memory blocks, and may be damaged as a result, particularly in the case where the read operation is performed excessively. The device controller 220 may manage read count of each memory block, and may recover the

damaged data of a corresponding memory block by performing read reclaim for the memory block of which the read count has reached a set or predetermined threshold count. Read reclaim may be performed by detecting and correcting an error by reading the data stored in a memory block of which read count has reached the set or predetermined threshold count and by storing the error-corrected data in another memory block.

[0060] The processor 223 may use different threshold counts in the first refresh scan operation that is performed according to the request of the host device 100 and the second refresh scan operation that is performed as determined by the processor 223. For example, the processor 223 may use a first threshold count in the first refresh scan operation and may use a second threshold count in the second refresh scan operation. The first threshold count may be less than the second threshold count.

[0061] The first refresh scan result may include a failed bit count, a read count and a program-erase count for each memory block. The first threshold count may include a first threshold failed bit count, a first threshold read count and a first threshold program-erase count.

[0062] The processor 223 may determine whether it is necessary to perform the first refresh operation and the degree of urgency, for each memory block, based on a comparison result of the first refresh scan result for each memory block of the nonvolatile memory device 210 and the first threshold count, and may transmit a determination result to the host device 100, as a refresh scan result for the nonvolatile

memory device 210. The determination result may be indicative of a normal state, a low state or a high state, but it is to be noted that the determination result is not specifically limited thereto. The normal state may be a state in which a refresh operation for the nonvolatile memory device 210 is not necessary. The low state may be a state in which a refresh operation for the nonvolatile memory device 210 is necessary but need not be performed urgently. The high state may mean a state in which a refresh operation for the nonvolatile memory device 210 is necessary and need be performed urgently.

[0063] The host device 100 may transmit or not transmit the refresh operation command RO CMD to the processor 223 based on the refresh scan result transmitted from the processor 223.

[0064] As described above, the processor 223 performs by its own determination a refresh operation, that is, the second refresh operation, for the nonvolatile memory device 210 even without a request from the host device 100. The processor 223 may continuously perform the second refresh scan operation for the nonvolatile memory device 210. The second refresh scan operation may include an operation of checking a read count or a program-erase count for each of the memory blocks of the nonvolatile memory device 210. The second refresh scan result may include a read count and a program-erase count for each memory block. The second threshold count may include a second threshold read count and a second threshold program-erase count.

[0065] The processor 223 may determine whether a memory block

of which the read count or the program-erase count is greater than the second threshold count exists among the memory blocks of the nonvolatile memory device 210. If such a memory block does not exist, the processor 223 may not perform a refresh operation for the nonvolatile memory device 210. If at least one such memory block exists, the processor 223 may perform a refresh operation for the nonvolatile memory device 210.

[0066] FIG. 2 is a flow chart describing a method for operating the data storage device 200 in accordance with an embodiment. In explaining the method for operating the data storage device 200 in accordance with the embodiment, with reference to FIG. 2, reference also may be made to FIG. 1.

[0067] The method for operating the data storage device 200 in accordance with the embodiment may include a first refresh operation (Refresh Operation 1) RO1 that is passively performed according to the request of the host device 100 and a second refresh operation (Refresh Operation 2) RO2 that is actively performed based on a reference set or predetermined in the data storage device 200.

[0068] Steps S201 to S213 of FIG. 2 represent the first refresh operation RO1.

[0069] At step S201, the host controller 120 of the host device 100 may transmit a refresh scan command RS CMD to the data storage device 200. The host device 100 may transmit the refresh scan command RS CMD to the data storage device 200 when the data storage device 200 is in a standby state in which a user does not use

the data storage device 200 or if a refresh operation request for a memory is inputted from the user, but it is to be noted that the embodiment is not specifically limited thereto.

[0070] At step S203, the processor 223 of the device controller 220 of the data storage device 200 may perform a first refresh scan operation for the plurality of memory blocks (not shown) in the nonvolatile memory device 210. The first refresh scan operation may include checking the count of failed bits in the data stored in each memory block, a read count for each memory block and a program-erase count for each memory block.

[0071] At step S205, the processor 223 may compare a first refresh scan result with a set or predetermined first threshold count. The first refresh scan result may include a failed bit count, a read count and a program-erase count for each memory block. The set or predetermined first threshold count may include a first threshold failed bit count, a first threshold read count and a first threshold program-erase count.

[0072] The processor 223 may compare a failed bit count, a read count and a program-erase count for each of all the memory blocks in the nonvolatile memory device 210 with the first threshold failed bit count, the first threshold read count and the first threshold program-erase count, respectively.

[0073] At step S207, the processor 223 may determine whether it is necessary to perform a first refresh operation and the degree of urgency, for each memory block, based on a comparison result of the

first refresh scan result of each memory block and the first threshold count. Whether it is necessary to perform a first refresh operation may mean whether it is necessary to perform a first refresh operation for a corresponding memory block. The degree of urgency of the first refresh operation may mean a point of time at which the first refresh operation is to be performed for the corresponding memory block.

[0074] For example, if a memory block of which first refresh scan result is greater than the first threshold count does not exist among the memory blocks of the nonvolatile memory device 210, the processor 223 may determine a normal state in which it is not necessary to perform the first refresh operation. If memory blocks of which first refresh scan results are greater than the first threshold count, among the memory blocks of the nonvolatile memory device 210 are less than a first percentage, the processor 223 may determine a low state in which it is necessary to perform the first refresh operation but need not be performed in an urgent basis. If memory blocks of which first refresh scan results are greater than the first threshold count, among the memory blocks of the nonvolatile memory device 210 are equal to or greater the first percentage and less than a second percentage, the processor 223 may determine a high state in which it is necessary to perform the first refresh operation and need be performed in an urgent basis. For example, the first percentage may be 5% of the memory blocks in the nonvolatile memory device 210 and the second percentage may be 10% of the memory blocks in the nonvolatile memory device 210, but it is to be noted that the

embodiment is not specifically limited thereto.

[0075] At step S209, the processor 223 may transmit a first refresh scan result to the host device 100. The processor 223 may transmit the first refresh scan result to the host device 100, as the normal state, the low state or the high state.

[0076] At step S211, the host device 100 may transmit or not transmit a first refresh operation command RO CMD to the processor 223 based on the first refresh scan result transmitted from the processor 223. If the normal state is received from the processor 223, the host device 100 may not transmit the first refresh operation command RO CMD to the processor 223. If the low state or the high state is received from the processor 223, the host device 100 may transmit the first refresh operation command RO CMD to the processor 223.

[0077] The host device 100 may transmit the first refresh operation command RO CMD to the data storage device 200 immediately when the first refresh scan result is received from the processor 223. Alternatively, the host device 100 may not transmit the first refresh operation command RO CMD to the data storage device 200 immediately when the first refresh scan result is received from the processor 223, and may transmit the first refresh operation command RO CMD to the data storage device 200 at an appropriate point of time. The appropriate point of time may be a point of time at which the data storage device 200 is not used by a user or a point of time at which a refresh operation is requested by the user's manipulation, but it is to

be noted that the embodiment is not specifically limited thereto.

[0078] At step S213, if the first refresh operation command RO CMD is transmitted from the host device 100, the processor 223 may perform the first refresh operation for the nonvolatile memory device 210.

[0079] Steps S215 to S221 of FIG. 2 represent the second refresh operation RO2.

[0080] At step S215, the processor 223 of the device controller 220 of the data storage device 200 may perform a second refresh scan operation for the memory blocks of the nonvolatile memory device 210. The second refresh scan operation may be a scan operation for the memory blocks that is performed by the determination of the processor 223 regardless of the refresh scan command RS CMD transmitted from the host device 100. The second refresh scan operation may include an operation of checking a read count or a program-erase count for each of the memory blocks of the nonvolatile memory device 210.

[0081] At step S217, the processor 223 may compare read counts or program-erase counts for the memory blocks of the nonvolatile memory device 210 with a set or predetermined second threshold count (for example, a second threshold read count or a second threshold program-erase count). The second threshold count used at the present step may be greater than the first threshold count used at the step S205 of the first refresh operation RO1.

[0082] At step S219, the processor 223 may determine whether a memory block of which read count or program-erase count is greater

than the second threshold count exists among the memory blocks of the nonvolatile memory device 210. If a memory block of which read count or program-erase count is greater than the second threshold count does not exist, the process may proceed to the step S215. If a memory block of which read count or program-erase count is greater than the second threshold count exists, the process may proceed to step S221.

[0083] At step S221, the processor 223 may perform a second refresh operation for the nonvolatile memory device 210 regardless of the refresh operation command RO CMD transmitted from the host device 100. For example, if a memory block of which read count is greater than the second threshold read count exists, the processor 223 may perform read reclaim as the second refresh operation for the nonvolatile memory device 210. If a memory block of which program-erase count is greater than the second threshold program-erase count exists, the processor 223 may perform wear leveling as the second refresh operation for the nonvolatile memory device 210.

[0084] In the present embodiment, the first refresh operation according to the request of the host device 100 may be performed based on the percentage of memory blocks of which read counts and/or program-erase counts are greater than the first threshold count, among the memory blocks in the nonvolatile memory device 210. Conversely, the second refresh operation according to the determination of the data storage device 200 may be performed when there exists at least one memory block of which read count and/or

program-erase count is greater than the second threshold count, among the memory blocks in the nonvolatile memory device 210.

[0085] Since the first threshold count used in the first refresh operation to be performed according to the request of the host device 100 is less than the second threshold count used in the second refresh operation to be performed by the determination of the data storage device 200, a refresh operation may be performed in advance, such as when a user is not using the data storage device 200 or when a refresh is requested from the user. As a result, it is possible to prevent the operation performance of the data storage device 200 from degrading while the data storage device 200 is used by the user.

[0086] Also, since a refresh operation for the nonvolatile memory device 210 may be performed at an appropriate time, the reliability of the data storage device 200 may be improved.

[0087] FIG. 3 is a diagram illustrating an example of a data processing system including a solid state drive (SSD) according to an embodiment. Referring to FIG. 3, a data processing system 2000 may include a host apparatus 2100 and an SSD 2200.

[0088] The SSD 2200 may include a controller 2210, a buffer memory device 2220, non-volatile memory devices 2231 to 223n, a power supply 2240, a signal connector 2250, and a power connector 2260.

[0089] The controller 2210 may control an overall operation of the SSD 2220.

[0090] The buffer memory device 2220 may temporarily store data

to be stored in the nonvolatile memory devices 2231 to 223n. The buffer memory device 2220 may temporarily store data read from the nonvolatile memory devices 2231 to 223n. The data temporarily stored in the buffer memory device 2220 may be transmitted to the host apparatus 2100 or the nonvolatile memory devices 2231 to 223n according to control of the controller 2210.

[0091] The nonvolatile memory devices 2231 to 223n may be used as a storage medium of the SSD 2200. The nonvolatile memory devices 2231 to 223n may be coupled to the controller 2210 through a plurality of channels CH1 to CHn. One or more nonvolatile memory devices may be coupled to one channel. The nonvolatile memory devices coupled to the one channel may be coupled to the same signal bus and the same data bus.

[0092] The power supply 2240 may provide power PWR input through the power connector 2260 to the inside of the SSD 2200. The power supply 2240 may include an auxiliary power supply 2241. The auxiliary power supply 2241 may supply the power so that the SSD 2200 is normally terminated even when sudden power-off occurs. The auxiliary power supply 2241 may include large capacity capacitors capable of charging the power PWR.

[0093] The controller 2210 may exchange a signal SGL with the host apparatus 2100 through the signal connector 2250. The signal SGL may include a command, an address, data, and the like. The signal connector 2250 may be configured as any of various types of connectors according to an interfacing method between the host

apparatus 2100 and the SSD 2200.

[0094] FIG. 4 is a diagram illustrating an example of the controller 2210 of FIG. 3. Referring to FIG. 4, the controller 2210 may include a host interface 2211, a control component 2212, a random access memory (RAM) 2213, an error correction code (ECC) component 2214, and a memory interface 2215.

[0095] The host interface 2211 may perform interfacing between the host apparatus 2100 and the SSD 2200 according to a protocol of the host apparatus 2100. For example, the host interface 2211 may communicate with the host apparatus 2100 through any one among a secure digital protocol, a universal serial bus (USB) protocol, a multimedia card (MMC) protocol, an embedded MMC (eMMC) protocol, a personal computer memory card international association (PCMCIA) protocol, a parallel advanced technology attachment (PATA) protocol, a serial advanced technology attachment (SATA) protocol, a small computer system interface (SCSI) protocol, a serial attached SCSI (SAS) protocol, a peripheral component interconnection (PCI) protocol, a PCI Express (PCI-E) protocol, and a universal flash storage (UFS) protocol. The host interface 2211 may perform a disc emulation function that the host apparatus 2100 recognizes the SSD 2200 as a general-purpose data storage apparatus, for example, a hard disc drive HDD.

[0096] The control component 2212 may analyze and process the signal SGL input from the host apparatus 2100. The control component 2212 may control operations of internal functional blocks according to

firmware and/or software for driving the SDD 2200. The RAM 2213 may be operated as a working memory for driving the firmware or software.

[0097] The ECC component 2214 may generate parity data for the data to be transferred to the nonvolatile memory devices 2231 to 223n. The generated parity data may be stored in the nonvolatile memory devices 2231 to 223n together with the data. The ECC component 2214 may detect errors for data read from the nonvolatile memory devices 2231 to 223n based on the parity data. When detected errors are within a correctable range, the ECC component 2214 may correct the detected errors.

[0098] The memory interface 2215 may provide a control signal such as a command and an address to the nonvolatile memory devices 2231 to 223n according to control of the control component 2212. The memory interface 2215 may exchange data with the nonvolatile memory devices 2231 to 223n according to control of the control component 2212. For example, the memory interface 2215 may provide data stored in the buffer memory device 2220 to the nonvolatile memory devices 2231 to 223n or provide data read from the nonvolatile memory devices 2231 to 223n to the buffer memory device 2220.

[0099] FIG. 5 is a diagram illustrating an example of a data processing system including a data storage apparatus according to an embodiment. Referring to FIG. 5, a data processing system 3000 may include a host apparatus 3100 and a data storage apparatus 3200.

[00100] The host apparatus 3100 may be configured in a board form such as a printed circuit board (PCB). Although not shown in FIG. 5, the host apparatus 3100 may include internal functional blocks configured to perform functions of the host apparatus 3100.

[00101] The host apparatus 3100 may include a connection terminal 3110 such as a socket, a slot, or a connector. The data storage apparatus 3200 may be mounted on the connection terminal 3110.

[00102] The data storage apparatus 3200 may be configured in a board form such as a PCB. The data storage apparatus 3200 may be embodied as a memory module or a memory card. The data storage apparatus 3200 may include a controller 3210, a buffer memory device 3220, nonvolatile memory devices 3231 to 3232, a power management integrated circuit (PMIC) 3240, and a connection terminal 3250.

[00103] The controller 3210 may control an overall operation of the data storage apparatus 3200. The controller 3210 may be configured to have the same configuration as the controller 2210 illustrated in FIG. 4.

[00104] The buffer memory device 3220 may temporarily store data to be stored in the nonvolatile memory devices 3231 and 3232. The buffer memory device 3220 may temporarily store data read from the nonvolatile memory devices 3231 and 3232. The data temporarily stored in the buffer memory device 3220 may be transmitted to the host apparatus 3100 or the nonvolatile memory devices 3231 and 3232 according to control of the controller 3210.

[00105] The nonvolatile memory devices 3231 and 3232 may be used

as a storage medium of the data storage apparatus 3200.

[00106] The PMIC 3240 may provide power input through the connection terminal 3250 to the inside of the data storage apparatus 3200. The PMIC 3240 may manage the power of the data storage apparatus 3200 according to control of the controller 3210.

[00107] The connection terminal 3250 may be coupled to the connection terminal 3110 of the host apparatus 3100. A signal such as a command, an address, and data and power may be transmitted between the host apparatus 3100 and the data storage apparatus 3200 through the connection terminal 3250. The connection terminal 3250 may be configured in various forms according to an interfacing method between the host apparatus 3100 and the data storage apparatus 3200. The connection terminal 3250 may be arranged in any one side of the data storage apparatus 3200.

[00108] FIG. 6 is a diagram illustrating an example of a data processing system including a data storage apparatus according to an embodiment. Referring to FIG. 6, a data processing system 4000 may include a host apparatus 4100 and a data storage apparatus 4200.

[00109] The host apparatus 4100 may be configured in a board form such as a PCB. Although not shown in FIG. 6, the host apparatus 4100 may include internal functional blocks configured to perform functions of the host apparatus 4100.

[00110] The data storage apparatus 4200 may be configured in a surface mounting package form. The data storage apparatus 4200 may be mounted on the host apparatus 4100 through a solder ball

4250. The data storage apparatus 4200 may include a controller 4210, a buffer memory device 4220, and a nonvolatile memory device 4230.

[00111] The controller 4210 may control an overall operation of the data storage apparatus 4200. The controller 4210 may be configured to have the same configuration as the controller 2210 illustrated in FIG. 4.

[00112] The buffer memory device 4220 may temporarily store data to be stored in the nonvolatile memory device 4230. The buffer memory device 4220 may temporarily store data read from the nonvolatile memory device 4230. The data temporarily stored in the buffer memory device 4220 may be transmitted to the host apparatus 4100 or the nonvolatile memory device 4230 through control of the controller 4210.

[00113] The nonvolatile memory device 4230 may be used as a storage medium of the data storage apparatus 4200.

[00114] FIG. 7 is a diagram illustrating an example of a network system 5000 including a data storage apparatus according to an embodiment. Referring to FIG. 7, the network system 5000 may include a server system 5300 and a plurality of client systems 5410 to 5430 which are coupled through a network 5500.

[00115] The server system 5300 may serve data in response to requests of the plurality of client systems 5410 to 5430. For example, the server system 5300 may store data provided from the plurality of client systems 5410 to 5430. In another example, the server system 5300 may provide data to the plurality of client systems 5410 to 5430.

[00116] The server system 5300 may include a host apparatus 5100 and a data storage apparatus 5200. The data storage apparatus 5200 may be configured of the data storage apparatus 10 of FIG. 1, the data storage apparatus 2200 of FIG. 3, the data storage apparatus 3200 of FIG. 5, or the data storage apparatus 4200 of FIG. 6.

[00117] FIG. 8 is a block diagram illustrating an example of a nonvolatile memory device in a data storage apparatus according to an embodiment. Referring to FIG. 8, a nonvolatile memory device 100 may include a memory cell array 1100, a row decoder 1200, a column decoder 1400, a data read/write block 1300, a voltage generator 1500, and a control logic 1600.

[00118] The memory cell array 1100 may include memory cells MC arranged in regions in which word lines WL1 to WLm and bit lines BL1 to BLn intersect.

[00119] The row decoder 1200 may be coupled to the memory cell array 1100 through the word lines WL1 to WLm. The row decoder 1200 may operate through control of the control logic 1600. The row decoder 1200 may decode an address provided from an external apparatus (not shown). The row decoder 1200 may select and drive the word lines WL1 to WLm based on a decoding result. For example, the row decoder 1200 may provide a word line voltage provided from the voltage generator 1500 to the word lines WL1 to WLm.

[00120] The data read/write block 1300 may be coupled to the memory cell array 1100 through the bit lines BL1 to BLn. The data read/write block 1300 may include read/write circuits RW1 to RWn

corresponding to the bit lines BL1 to BLn. The data read/write block 1300 may operate according to control of the control logic 1600. The data read/write block 1300 may operate as a write driver or a sense amplifier according to an operation mode. For example, the data read/write block 1300 may operate as the write driver configured to store data provided from an external apparatus in the memory cell array 1100 in a write operation. In another example, the data read/write block 1300 may operate as the sense amplifier configured to read data from the memory cell array 1100 in a read operation.

[00121] The column decoder 1400 may operate though control of the control logic 1600. The column decoder 1400 may decode an address provided from an external apparatus (not shown). The column decoder 1400 may couple the read/write circuits RW1 to RWn of the data read/write block 1300 corresponding to the bit lines BL1 to BLn and data input/output (I/O) lines (or data I/O buffers) based on a decoding result.

[00122] The voltage generator 1500 may generate voltages used for an internal operation of the nonvolatile memory device 1000. The voltages generated through the voltage generator 1500 may be applied to the memory cells of the memory cell array 1100. For example, a program voltage generated in a program operation may be applied to word lines of memory cells in which the program operation is to be performed. In another example, an erase voltage generated in an erase operation may be applied to well regions of memory cells in which the erase operation is to be performed. In another example, a read

voltage generated in a read operation may be applied to word lines of memory cells in which the read operation is to be performed.

[00123] The control logic 1600 may control an overall operation of the nonvolatile memory device 1000 based on a control signal provided from an external apparatus. For example, the control logic 1600 may control an operation of the nonvolatile memory device 100 such as a read operation, a write operation, an erase operation of the nonvolatile memory device 1000.

[00124] Hereinafter, another embodiment of the present disclosure will be described. Specifically, a storage system performing a self refresh operation and an auto refresh operation will be described in detail with reference to FIGS. 9 through 13.

[00125] FIG. 9 is a diagram for describing a storage system according to an embodiment of the present disclosure.

[00126] Referring to FIG. 9, The storage system 600 may be an embodiment of the data storage device described with reference to FIG. 1. The storage system 600 may include a memory device 800 in which data is stored and a memory controller 900 that may control the memory device 800 in response to a request from a host 500.

[00127] The memory device 800 may operate in response to control of the memory controller 900. The memory device 800 may include a plurality of memory blocks that store data. The memory blocks may include a plurality of memory cells. The memory device 900 may be

configured of a NAND flash memory, a vertical NAND flash memory, a NOR flash memory, a resistive random access memory (RRAM), a phase change memory (PRAM), a magneto resistive random access memory (MRAM), a ferroelectric random access memory (FRAM), a spin transfer torque random access memory (STT-RAM), or the like. In the present specification, it is assumed that the memory device 1100 is a NAND flash memory.

[00128] The memory controller 900 may control the memory device 800 in response to a request from the host 500 and may perform a background operation of managing the memory device 800 without the request of the host 500. For example, the memory controller 900 may perform a background operation such as wear leveling and garbage collection.

[00129] The memory controller 900 may execute firmware such as a flash translation layer (FTL) for controlling communication between the host 500 and the memory device 800. The flash translation layer may receive data and a logical block address from the host 500 and may convert the logical block address into a physical block address. To this end, the memory controller 900 may store and manage a logical-physical address mapping table of the logical block address and the physical address.

[00130] The memory controller 900 may control the memory device 800 to perform a program operation, a read operation, an erase operation, or the like according to a request of the host 500. During the program operation, the memory controller 900 may provide a program command, the physical block address, and data to the memory device 800. During the read operation, the memory controller 900 may provide a read command and the physical block address to the memory device 800. During the erase operation, the memory controller 900 may provide an erase command and the physical block address to the memory device 800.

[00131] The memory controller 900 may include a buffer memory (not shown) for exchanging data between the host 500 and the memory device 800. The buffer memory may be included inside the memory controller 900 or may be disposed outside the memory controller 900. For example, the memory controller 900 may temporarily store data input from the host 500 in the buffer memory, and then transmit the data that is temporarily stored in the buffer memory to the memory device 800. In addition, the buffer memory may be used as an operation memory and a cache memory of the memory controller 900, and may store codes or commands executed by the memory controller 900. For example, the buffer memory may

be implemented by a dynamic random access memory (DRAM) such as a double data rate synchronous dynamic random access memory (DDR SDRAM), a DDR4 SDRAM, a low power double data rate4 (LPDDR4) SDRAM, a graphics double data rate (GDDR) SDRAM, a low power DDR (LPDDR), or Rambus dynamic random access memory (DRAM), or a static random access memory (SRAM).

[00132] In the present embodiment, the memory controller 900 may include a refresh controller 910 to perform a self refresh operation or an auto refresh operation to maintain the data stored in the memory device 800. That is, the memory controller 900 may output various refresh commands so that the memory device 800 may perform the refresh operation, and at this time, the refresh controller 910 may be used.

[00133] A configuration of the memory controller 900 capable of controlling the above-described refresh operation will be specifically described as follows.

[00134] FIG. 10 is a diagram for specifically describing a refresh controller according to an embodiment of the present disclosure.

[00135] Referring to FIG. 10, the refresh controller 910 may include an auto refresh controller 911 and a self refresh controller 912.

[00136] The auto refresh controller 911 may output an auto refresh

command CMD_AR that causes the memory device 800 to perform a refresh operation for the selected memory block. In other words, the auto refresh command CMD_AR may be a command for performing a refresh operation for one selected target block.

[00137] Therefore, the memory device 800 may end the refresh operation after performing the refresh operation for the target block that is a refresh target block in response to the auto refresh command CMD_AR. Here, the target block may be expressed as a victim block, but in the following embodiment, the refresh target block is defined as a target block.

[00138] The auto refresh controller 911 may be activated when performing the background operation or when the memory device 800 is in an idle status. To this end, the auto refresh controller 911 may include a status determiner 911-1 for determining a status of the memory device 800. For example, the status determiner 911-1 may output a status check signal to the memory device 800. When the status signal received from the memory device 800 indicates that all the status signals are idle status, the status determiner 911-1 may generate an auto refresh enable signal for performing the auto refresh operation. The auto refresh controller 911-1 may output the auto refresh command CMD_AR to the memory device 800 when the status

determiner 911-1 generates the auto refresh enable signal.

[00139] The self refresh controller 912 may output a self refresh command CMD_SR and a refresh end command CMD_FIN. The self refresh command CMD_SR may be a command that causes the memory device 800 to perform a refresh operation while selecting the memory blocks by itself without an additional refresh command, and the refresh end command CMD_FIN may be a command for ending the self refresh operation performed by the memory device 800. For example, after performing the refresh operation for the target block in response to the self refresh command CMD_SR, the memory device 800 may newly select a next target block even though an additional refresh command is not received from the memory controller 900, and may performed a refresh operation for the newly selected target block by itself. That is, the memory device 1100 may continuously perform the refresh operation while changing the target block until receiving the refresh end command CMD_FIN from a self refresh controller 912. The self refresh controller 912 may output the refresh end command CMD_FIN when a normal operation request is received from the host 500 of FIG. 9 or when another background operation is to be performed.

[00140] The self refresh controller 912 may also be activated when the memory device 800 is in the idle status and thus may share the

status determiner included in the auto refresh controller 911.

[00141] For example, when a background operation other than the refresh operation is not performed, the refresh controller 910 may activate the self refresh controller 912. When the other background operation is performed, a time during which the refresh operation is performed is short, and thus the refresh controller 910 may activate the auto refresh controller 911.

[00142] In an embodiment, the memory device 800 may further include a history register (not shown). In response to the refresh end command CMD FIN, the memory device 800 may store information about a memory block in which the refresh operation is performed in the history register. In an embodiment, in response to the input of the self refresh command CMD SR, the memory device may determine a memory block to perform the next refresh operation by using information about the memory block included in the history register. For example, the self refresh operation may be performed in order of increasing address of the memory block included in the memory device 800. Alternatively, the self refresh operation may be performed in order of decreasing address of the memory block included in the memory device 800. Alternatively, the self refresh operation may be performed in a preset order. In this case, the memory device 800 may

store the preset order in advance.

[00143] FIG. 11A and FIG. 11B illustrate a refresh operation of a memory device including one plane.

[00144] FIG. 11A shows a refresh operation performed in the same plane, and FIG. 11B shows a position where data is stored before and after the refresh operation.

[00145] Referring to FIG. 11A, the memory cell array 1100 may include a plane, and the plane may include a plurality of memory blocks. In FIG. 11A, first to sixth memory blocks BLK1 to BLK6 are included in the plane, but the number of memory blocks included in the plane is not limited thereto. Each of the first to sixth memory blocks BLK1 to BLK6 may include a plurality of pages, and each of the pages may include a plurality of memory cells.

[00146] In FIG. 11A, it is assumed that the first to fifth memory blocks BLK1 to BLK5 are memory blocks for storing data, and the sixth memory block BLK6 is a memory block allocated for performing a refresh operation. That is, the sixth memory block BLK6 allocated for performing the refresh operation may be a buffer block. Therefore, the sixth memory block BLK6 may maintain the erase status before the refresh operation is performed and after the refresh operation is performed.

[00147] When the fourth memory block BLK4 among the first to fifth memory blocks BLK1 to BLK5 is the target block (or victim block), the data stored in the fourth memory block BLK4 may be a fourth refresh data REF_Data4.

[00148] The fourth refresh data stored in the fourth memory block BLK4 is transferred to the temporary buffer circuit 1300(①). In one embodiment, the temporary buffer circuit 1300 may be the data read/write block of FIG. 8. Then the memory device performs a program operation for storing data stored in the temporary buffer circuit 1300 in the sixth memory block BLK6 (②). Transferring the data from the fourth memory block to the temporary buffer circuit 1300 may be accomplished by a plurality of read operations for the fourth memory block. Storing the data in the sixth memory block BLK6 may be accomplished by a plurality of program operations. In one embodiment, Transferring the data from the fourth memory block to the temporary buffer circuit 1300 and storing the data in the sixth memory block BLK6 may be performed page by page.

[00149] When all the data stored in the fourth memory block BLK4 are transmitted to the sixth memory block BLK6, the memory device performs an erase operation for the fourth memory block BLK4. When the fourth memory block BLK4 is erased, data stored in the sixth

memory block BLK6 is transferred to the temporary buffer circuit 1300(③). Then the memory device performs a program operation for storing data stored in the temporary buffer circuit 1300 in the fourth memory block BLK4 after data in the fourth memory block BLK4 has been erased (④). Transferring the data from the sixth memory block to the temporary buffer circuit 1300 may be accomplished by a plurality of read operations for the sixth memory block. Storing the data in the fourth memory block BLK4 may be accomplished by a plurality of program operations. In one embodiment, Transferring the data from the sixth memory block to the temporary buffer circuit 1300 and storing the data in the fourth memory block BLK4 may be performed page by page.

[00150] As a result, the refresh operation according to the present disclosure may be performed inside the memory device without data input and output between the memory device and the memory controller. Therefore, the memory controller does not generate or update mapping data for reprogramming the data programmed to the target block. Thus, cost for generating and managing the mapping data during the refresh operation does not occur.

[00151] FIG. 12 is a diagram for specifically describing the refresh operation according to an embodiment of the present disclosure.

[00152] Referring to FIG. 12, since the refresh operation according to

the first embodiment described above is an auto refresh operation, when the refresh operation of a selected target block is completed, the refresh operation may be ended without performing the refresh operation of the next block.

[00153] Therefore, the auto refresh operation may be performed as follows.

[00154] When an auto refresh command is received from a memory controller (S901), a memory device may read data of a target block to a temporary buffer circuit (S902). When the memory device is a non-volatile memory device, the read operation may be performed in a page unit of data included in the target block.

[00155] Next to step S902, the data stored in the temporary buffer circuit may be programmed to a buffer block (S903).

[00156] When the data is programmed to the buffer block (S903), an erase operation of the target block may be performed (S904).

[00157] Next to step S904, the data of the buffer block is read to the temporary buffer circuit and temporarily stored (S905), and the data of the temporary buffer circuit may be reprogrammed to the target block (S906).

[00158] When the data is reprogrammed to the target block, an erase operation of the buffer block may be performed for the refresh

operation of the next target block (S907), and a next target block address may be updated (S908).

[00159] When the next target block address is updated, the refresh operation by the auto refresh command may be ended.

[00160] FIG. 13 is a diagram for specifically describing the refresh operation according to an embodiment of the present disclosure.

[00161] Referring to FIG. 13, when a self refresh command is received to the memory device (S1101), the memory device may perform a refresh operation for a target block. The refresh operation for the target block may be performed equally to steps S902 to S908 described above with reference to FIG. 12.

[00162] When the refresh operation of the target block is ended, the memory device may determine whether a refresh end command is received (S1103).

[00163] When the refresh end command is not received (N), the memory device may repeat steps S902 to S908 while changing the address of the target block.When the refresh end command is received (Y), the memory device may end the self refresh operation.

[00164] The above embodiments of the present disclosure are illustrative, but the present invention is not limited to the disclosed embodiments. Various alternatives and equivalents are possible and are not limited by the embodiments described herein. Nor is the

present disclosure limited to any specific type of semiconductor device. Other additions, subtractions, or modifications apparent to those skilled in the art in view of the present disclosure are intended to fall within the scope of the appended claims.

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