

Abstract

A memory cell according to the present invention (1) includes a memory gate structure (2), a first select gate structure (3), and a second select gate structure (4). In the memory gate structure (2), a lower memory gate insulating film (10), a charge storage layer (EC), an upper memory gate insulating film (11), and a metal memory gate electrode (MG) are stacked in this order. The first select gate structure (3) includes a metal first select gate electrode (DG) along a first sidewall spacer (8a) provided on a sidewall of the memory gate structure (2). The second select gate structure (4) includes a metal second select gate electrode (SG) along a second sidewall spacer (8b) provided on another sidewall of the memory gate structure (2). With this configuration, the metal memory gate electrode (MG), the metal first select gate electrode (DG), and the metal second select gate electrode (SG) can be formed of a metallic material the same as that of a metal logic gate electrode (LG1). Thus, the memory cell can be formed through a series of manufacturing processes of forming the metal logic gate electrode (LG1) made of a metallic material on a semiconductor substrate.