CLAIMS

1. A semiconductor structure, comprising:

a plurality of first active columns, arranged in an array along a first direction and a second direction; wherein both the first direction and the second direction are perpendicular to an extension direction of the first active column, and the first direction is intersected with the second direction;

a plurality of first electrodes, located in first grooves arranged at intervals; wherein each of the first electrodes covers a side wall of one of the first active columns, and each of the first grooves surrounds a surface of each of the first active columns;

a plurality of first dielectric layers; wherein each of the first dielectric layers covers a side wall of one of the first electrodes and a bottom of a gap between two adjacent first electrodes; and

second electrodes covering surfaces of the plurality of first dielectric layers;

wherein the semiconductor structure further comprises:

a substrate; wherein a second oxide layer is formed on a surface of the substrate;

a plurality of oxide columns located on the second oxide layer; wherein each of the first active columns is located on a top surface of a corresponding oxide column; and

a first sacrificial layer located in a gap between the plurality of the oxide columns;

wherein the first dielectric layer covers the side wall of the first electrode and a top surface of the first sacrificial layer.

2. The semiconductor structure of claim 1, wherein the semiconductor structure further comprises:

a plurality of second active columns located on the first active columns; wherein an orthographic projection of each of the second active columns is overlapped with an orthographic projection of a corresponding first active column on a plane where of the first direction and the second direction are located;

a plurality of third electrodes located in third grooves arranged at intervals; wherein each of the third electrodes covers a side wall of one of the second active columns, each of the third grooves surrounds a surface of each of the second active columns, and the third electrode and the first electrode are connected with each other;

a plurality of second dielectric layers; wherein each of the second dielectric layers covers a side wall of one of the third electrodes, and the second dielectric layer and the first dielectric layer are connected with each other; and

fourth electrodes covering the plurality of second dielectric layers, wherein the fourth electrode and the second electrode are connected with each other.

3. The semiconductor structure of claim 1, wherein the semiconductor structure further comprises:

a plurality of third active columns, wherein each of the third active columns is located on a top surface of a corresponding first active column; and

a plurality of transistors, wherein each of the transistors has a channel structure located in the third active column and having an extension direction perpendicular to the plane where the first direction and the second direction are located.

4. The semiconductor structure of claim 3, wherein the transistor comprises:

a gate structure arranged at least around one side of the third active column; and

a source and a drain respectively arranged at two opposite ends of the third active column.

5. The semiconductor structure of claim 3, wherein the semiconductor structure further comprises:

a plurality of bit lines, located above the transistor and in electrical contact with tops of the third active columns.

6. A memory, comprising at least one semiconductor structure of any one of claims 1 to 5.

7. A method for manufacturing a semiconductor structure, comprising:

providing a substrate, and forming a plurality of first semiconductor columns arranged in an array along a first direction and a second direction on the substrate; wherein both the first direction and the second direction are perpendicular to an extension direction of the first semiconductor column, and the first direction is intersected with the second direction;

performing an oxidizing treatment on the plurality of first semiconductor columns to form oxide layers on surfaces of the first semiconductor columns;

filling a first sacrificial material in a gap between the oxide layers;

removing part of the oxide layer to obtain a first active column and a first groove;

forming a first electrode in the first groove;

removing part of the first sacrificial material in the gap between the oxide layers to form a second groove;

forming a first dielectric layer covering a side wall and a bottom of the second groove; and

forming a second electrode in the second groove formed with the first dielectric layer.

8. The method for manufacturing a semiconductor structure of claim 7, wherein the formation of the plurality of first semiconductor columns arranged in an array along the first direction and the second direction comprises:

etching the substrate to form a plurality of first trenches arranged at intervals along the first direction and a plurality of second trenches arranged at intervals along the second direction on the substrate, and

performing an enlarging treatment on a bottom of the first trench and/or a bottom of the second trench, to make each of the first semiconductor columns to comprise a first part and a second part located on the first part; wherein a maximum diameter width of the first part is less than a minimum diameter width of the second part.

9. The method for manufacturing a semiconductor structure of claim 8, wherein the formation of the oxide layers on the surfaces of the first semiconductor columns comprises:

performing the oxidizing treatment on the first semiconductor columns, to completely oxidize the first part into an oxide column, to oxidize a exposed surface of the second part into a first oxide layer, and to oxidize a surface of the substrate into a second oxide layer.

10. The method for manufacturing a semiconductor structure of claim 9, wherein the filling of the first sacrificial material in the gap between the oxide layers comprises:

filling the first sacrificial material in a gap between the plurality of oxide columns and a gap between the first oxide layers;

removing the first sacrificial material in the gap between the first oxide layers to form the second groove, and retaining the first sacrificial material in the gap of the plurality of the oxide columns to form a first sacrificial layer.

11. The method for manufacturing a semiconductor structure of claim 7, further comprising:

after the second electrode is formed, forming a plurality of second semiconductor columns arranged in an array along the first direction and the second direction on the first active columns;

performing an oxidizing treatment on the second semiconductor columns, to oxidize exposed surfaces of the second semiconductor columns into third oxide layers;

filling a second sacrificial material in a gap between the third oxide layers;

removing the third oxide layer to obtain a second active column and form a third groove;

forming a third electrode in the third groove;

removing the second sacrificial material to form a fourth groove;

forming a second dielectric layer on a side wall of the fourth groove; and

forming a fourth electrode in the fourth groove formed with the second dielectric layer; wherein the first electrode and the third electrode are connected with each other, the first dielectric layer and the second dielectric layer are connected with each other, and the second electrode and the fourth electrode are connected with each other.

12. The method for manufacturing a semiconductor structure of claim 11, wherein the formation of the plurality of second semiconductor columns arranged in the array along the first direction and the second direction on the first active columns comprises:

forming a second semiconductor substrate on the first active columns;

forming a plurality of third trenches arranged at intervals spaced along the first direction and a plurality of fourth trenches spaced along the second direction in the second semiconductor substrate, so as to form the plurality of second semiconductor columns arranged in the array along the first direction and the second direction on the first active

columns.

13. The method for manufacturing a semiconductor structure of claim 12, wherein the formation of the second semiconductor substrate on the first active columns comprises:

forming the second semiconductor substrate on the first active columns via an epitaxial growth technology.

14. The method for manufacturing a semiconductor structure of claim 7, further comprising:

forming a plurality of third active columns arranged in an array along the first direction and the second direction on the first active columns; wherein each of the third active columns is located on a top surface of a corresponding first active column;

forming a gate structure covering at least one side of the third active column; and

forming a source and a drain respectively at two opposite ends of the third active column.

15. The method for manufacturing a semiconductor structure of claim 14, further comprising:

forming a plurality of bit lines on the third active columns and in electrical contact with tops of the third active columns.