

ABSTRACT

A memory device includes a first semiconductor layer including a first cell region and a second cell region over the first cell region, and a second semiconductor layer under the first semiconductor layer in a substantially vertical direction and including a page buffer circuit which includes a first page buffer set associated with odd data and a second page buffer set associated with even data, the first cell region includes first memory cells, a first odd bit line transmitting odd data of the first memory cells, and a first even bit line transmitting even data of the first memory cells, the second cell region includes second memory cells, a second odd bit line transmitting odd data of the second memory cells, and a second even bit line transmitting even data of the second memory cells.

FIG. 4A