frequency band of operation of the quad-band device. A typical RF system requires multiple IPDs and other high frequency circuits in one or more semiconductor packages to perform the necessary electrical functions. Conductive layer 130c can be a ground plane for the IPD structure.

FIG. 4 shows a schematic representation of one implementation of the IPDs from FIG. 3g. Capacitor 140 represents the MIM capacitor; resistor 142 represents resistive layer 125; inductor 144 represents conductive layers 134e-134h. Conductive layer 138a is electrically connected to conductive layer 136~~4~~b; conductive layer 130b is electrically connected to conductive layer 136~~4~~c; conductive layer 136~~4~~i is electrically connected to conductive layer 138b.

The MIM capacitor has a given Q factor, which is a measure of efficiency as the ratio of capacitive reactance to resistance at a given frequency. The MIM capacitor must have a high Q factor for optimal RF performance. The insulating layer 126 formed over the first smooth surface of conductive layer 124 reduces the ESR of the MIM capacitor and hotspot problems caused by particles and hill-locks between the dielectric and conductive layers. Conductive layer 124 also reduces ~~high~~ hill-lock issues because of self-annealing. By decreasing ESR, the Q factor of the MIM capacitor is increased. In addition, the thick bottom-side conductive layer formed over the second smooth conductive layer 124 minimizes particles and hill-locks between the conductive layer and resistive layer, which increases the ESD protection level and reduces the ESR and increases Q factor for the MIM capacitor.

FIG. 5 illustrates an alternate process of forming an IPD structure using a smooth conductive layer and bottom-side conductive layer. Similar to FIGs. 3a-3b, a temporary or

sacrificial bottom-side substrate or carrier contains silicon, polymer, polymer composite, metal, ceramic, glass, glass epoxy, beryllium oxide, tape, or other suitable low-cost, rigid material or bulk semiconductor material for structural support. An interface layer 152 is applied over the bottom-side carrier. The interface layer 152 can be temporary bonding film or etch-stop layer to protect later-formed layers when removing of the temporary bottom-side carrier. The temporary bonding film can be heat or light releasable material. The etch-stop layer can be SiO2, Si3N4, SiON, organic film, polymer, or metal film with wet etching selectivity. The interface layer 152 is deposited using lamination, PVD, CVD, printing, spin coating, spray coating, sintering, or thermal oxidation.

A smooth conductive layer 154 is formed over interface layer 152 by patterning with PVD, CVD, or other suitable deposition process. In one embodiment, conductive layer 1~~2~~54 is a resistive layer including TaxSiy or other metal silicides, TaN, NiCr, Ti, TiN, TiW or doped poly-silicon having a resistivity between 5 and 100 ohm/sq. Conductive layer 1~~2~~54 can also be other conductive material exhibiting hill-lock issue during subsequent processing. Conductive layer 154 has opposing first and second smooth surfaces for later formation of a MIM capacitor.

A resistive layer 155 is patterned and deposited over interface layer 152 using PVD, CVD, or other suitable deposition process. Resistive layer 155 is Ta2Si or other metal silicides, TaN, NiCr, Ti, TiN, TiW or doped poly-silicon having a resistivity between 5 and 100 ohm/sq. Conductive layer 154 and resistive layer 155 can be formed during the same deposition and patterning process.

An insulating or dielectric layer 156 is formed over

represent one type of interconnect structure that can be formed over conductive pillars 166. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

The structures described in FIG. 5 constitute a plurality of passive circuit elements or IPDs. In one embodiment, conductive layer 160b, insulating layer 156, conductive layer 154, and conductive layer 168b is a MIM capacitor. Resistive layer 155 is a resistor element in the passive circuit. The individual sections of conductive layer 168e-168h can be wound or coiled in plan-view to produce or exhibit the desired properties of an inductor.

The MIM capacitor has a given Q factor, which is a measure of efficiency as the ratio of capacitive reactance to resistance at a given frequency. The MIM capacitor must have a high Q factor for optimal RF performance. The insulating layer 156 formed over the first smooth surface of conductive layer 154 reduces the ESR of the MIM capacitor and hotspot problems caused by particles and hill-locks between the dielectric and conductive layers. Conductive layer 154 also reduces ~~high~~hill-lock issues because of self-annealing. By decreasing ESR, the Q factor of the MIM capacitor is increased. In addition, the thick bottom-side conductive layer formed over the second smooth conductive layer 154 minimizes particles and hill-locks between the conductive layer and resistive layer, which increases the ESD protection level and reduces the ESR and increases Q factor for the MIM capacitor.

FIG. 6 illustrates another process of forming an IPD structure using a smooth conductive layer and bottom-side conductive layer. A temporary or sacrificial bottom-side substrate or carrier contains silicon, polymer, polymer

180b-180e can be wound or coiled in plan-view to produce or exhibit the desired properties of an inductor.

The MIM capacitor has a given Q factor, which is a measure of efficiency as the ratio of capacitive reactance to resistance at a given frequency. The MIM capacitor must have a high Q factor for optimal RF performance. The insulating layer 192 formed over the first smooth surface of conductive layer 188 reduces the ESR of the MIM capacitor and hotspot problems caused by particles and hill-locks between the dielectric and conductive layers. Conductive layer 188 also reduces ~~high~~hill-lock issues because of self-annealing. By decreasing ESR, the Q factor of the MIM capacitor is increased. In addition, the thick bottom-side conductive layer formed over the second smooth conductive layer 188 minimizes particles and hill-locks between the conductive layer and resistive layer, which increases the ESD protection level and reduces the ESR and increases Q factor for the MIM capacitor.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A semiconductor device, comprising:

an interface layer~~;~~

~~a smooth conductive layer disposed over the interface layer;~~

~~a first insulating layer disposed over a first surface of the smooth conductive layer;~~

~~a first conductive layer disposed over the first insulating layer and the interface layer, the first conductive layer contacting the first insulating layer;~~

~~a second insulating layer disposed over the second insulating layer and the first conductive layer; and~~

~~a second conductive layer disposed below the first conductive layer and contacting a second surface of the smooth conductive layer, the second surface of the smooth conductive layer opposite the first surface of the smooth conductive layer~~ disposed entirely at a first level of the semiconductor device;

a smooth conductive layer disposed entirely at a second level of the semiconductor device over the interface layer, wherein the second level of the semiconductor device is different from the first level of the semiconductor device;

a first insulating layer disposed over a first smooth surface of the smooth conductive layer;

a second insulating layer disposed over the first insulating layer and in direct contact with the first smooth surface of the smooth conductive layer;

a first conductive layer disposed through a first opening in the second insulating layer to directly contact the first insulating layer;

a third insulating layer disposed over the second insulating layer and the first conductive layer; and

a second conductive layer disposed through a second opening in the interface layer to directly contact a second smooth surface of the smooth conductive layer opposite the first smooth surface.

2. The semiconductor device of claim 1, further ~~comprising:~~

~~a third insulating layer disposed over the first insulating layer and the first surface of the smooth conductive layer, the third insulating layer exposing the first insulating layer and the interface layer; and~~including

a fourth insulating layer disposed below the second conductive layer and the interface layer.

3. The semiconductor device of claim 2, further ~~comprising~~ including a third conductive layer disposed below the second conductive layer and contacting the second conductive layer.

4. The semiconductor device of claim 1, ~~wherein the second conductive layer, smooth conductive layer, first insulating layer, and first conductive layer constitute~~ further including a metal-insulator-metal (MIM) capacitor comprising the second conductive layer, smooth conductive layer, first insulating layer, and first conductive layer.

5. The semiconductor device of claim 4, wherein the smooth conductive layer reduces particles and hill-locks between the first insulating layer and smooth conductive layer which increases breakdown voltage and electrostatic discharge protection for the MIM capacitor.

6. The semiconductor device of claim 4, wherein the smooth conductive layer and the second conductive layer form a bottom electrode of the MIM capacitor and increase a Q factor of the MIM capacitor.

7. The semiconductor device of claim 1, wherein a portion of the second conductive layer ~~includes an inductor~~ is coiled to exhibit an inductive property.

8. A semiconductor device, comprising:

a smooth conductive layer including opposing first and second entirely flat surfaces;

a first insulating layer disposed over ~~a~~the first entirely flat surface of the smooth conductive layer;

a second insulating layer disposed over the first insulating layer and in direct contact with the first entirely flat surface of the smooth conductive layer;

a first conductive layer disposed over the first insulating layer and in an opening in the second insulating layer over the first insulating layer;

~~a second insulating layer disposed over the first insulating layer and the first conductive layer;~~ and

a second conductive layer disposed over the opening in the second insulating layer and directly on the second entirely flat surface ~~below a second surface of the smooth conductive layer that is opposite the first surface~~ of the smooth conductive layer.

9. The semiconductor device of claim 8, further ~~comprising~~ including a third insulating layer disposed ~~below~~over the second conductive layer.

10. The semiconductor device of claim 8, ~~wherein the second conductive layer, the smooth conductive layer, the first insulating layer, and the first conductive layer constitute~~ further including a metal-insulator-metal (MIM) capacitor comprising the second conductive layer, smooth conductive layer, first insulating layer, and first conductive layer.

11. The semiconductor device of claim 10, wherein the smooth conductive layer reduces particles and hill-locks between the first insulating layer and the smooth conductive layer which increases breakdown voltage and electrostatic discharge protection for the MIM capacitor.

12. The semiconductor device of claim 10, wherein the smooth conductive layer and the second conductive layer form ~~a bottom~~ an electrode of the MIM capacitor and increase a Q factor of the MIM capacitor.

13. A semiconductor device, comprising:

a first conductive layer;

a first insulating layer disposed over a ~~first~~smooth surface of the first conductive layer;

a second insulating layer disposed ~~over~~on the ~~first~~smooth surface of the first conductive layer and the first insulating layer;

a second conductive layer disposed ~~over the first insulating layer~~ in an opening in the second insulating layer

extending to the first insulating layer with the first insulating layer separating the second conductive layer from the first conductive layer; and

a third conductive layer ~~disposed below a second surface of the first conductive layer that is opposite the first surface of the first conductive layer~~including a first portion disposed on a second surface of the first conductive layer opposite the smooth surface of the first conductive layer and a second portion disposed over the second insulating layer and coiled to exhibit an inductive property.

14. The semiconductor device of claim 13, further ~~comprising~~including:

a third insulating layer disposed over the second insulating layer and the second conductive layer; and

a fourth insulating layer disposed below the third conductive layer.

15. The semiconductor device of claim 13, wherein the ~~second insulating layer exposes the first insulating layer~~ smooth surface of the first conductive layer is entirely flat.

16. The semiconductor device of claim 13, further ~~comprising~~ including a fourth conductive layer disposed ~~below the third conductive layer and contacting~~ over the third conductive layer.

17. The semiconductor device of claim 13, ~~wherein the third conductive layer, the first conductive layer, the first insulating layer, and the second conductive layer constitute~~ further including a metal-insulator-metal (MIM) capacitor comprising the first portion of the third conductive layer, first conductive layer, first insulating layer, and second conductive layer.

18. The semiconductor device of claim 17, wherein the first conductive layer reduces particles and hill-locks between the first insulating layer and first conductive layer which increases breakdown voltage and electrostatic discharge protection for the MIM capacitor.

19. The semiconductor device of claim 17, wherein the first conductive layer and first portion of the third conductive layer form ~~a bottom~~ an

electrode of the MIM capacitor ~~and increase a Q factor of the MIM capacitor~~.

20. The semiconductor device of claim 14, ~~wherein the third or the fourth insulating layer provides structural support~~ further including a conductive pillar disposed in the third insulating layer or fourth insulating layer.

21. A semiconductor device, comprising:

a ~~smooth~~ first conductive layer;

a first insulating layer disposed over a first entirely flat surface of the ~~smooth~~ first conductive layer;

~~a first conductive layer disposed over the first insulating layer;~~

a second insulating layer disposed over the first conductive layer; ~~and~~

a second conductive layer disposed ~~below a second surface of the smooth conductive layer that is opposite the first surface of the smooth conductive layer~~ over the second insulating layer and in an opening in the second insulating layer extending to the first insulating layer; and

a third conductive layer disposed on a second entirely flat surface of the first conductive layer opposite the first entirely flat surface of the first conductive layer and aligned with the opening in the second insulating layer and electrically connected to the second conductive layer.

22. The semiconductor device of claim 21, further ~~comprising~~including :

a third insulating layer disposed over the ~~first insulating layer and the first surface of the smooth conductive layer, the~~

~~third insulating layer exposing the first~~second insulating layer; and

a fourth insulating layer disposed ~~below~~ over the ~~second~~ third conductive layer.

23. The semiconductor device of claim 21, further ~~comprising a third conductive layer disposed below the second~~ including a fourth conductive layer ~~and contacting the second~~ disposed over the third conductive layer.

24. The semiconductor device of claim 21, ~~wherein the second conductive layer, the smooth conductive layer, the first~~

~~insulating layer, and the first conductive layer constitute~~ further including a metal-insulator-metal (MIM) capacitor comprising the third conductive layer, first conductive layer, first insulating layer, and second conductive layer.

25. The semiconductor device of claim 24, wherein the ~~smooth~~first conductive layer reduces particles and hill-locks between the first insulating layer and the ~~smooth~~ first conductive layer which increases breakdown voltage and electrostatic discharge protection for the MIM capacitor.

26. The semiconductor device of claim 24, wherein the ~~smooth~~ first conductive layer and the ~~second~~ third conductive layer form an ~~bottom~~ electrode of the MIM capacitor and increase a Q factor of the MIM capacitor.

27. The semiconductor device of claim 21, further ~~comprising~~ including a resistive layer disposed between the third ~~insulating~~ conductive layer and ~~the fourth insulating~~ second conductive layer.

28. The semiconductor device of claim 21, wherein a portion of the third conductive layer is coiled to exhibit an inductive property.