A SYSTEM AND METHOD FOR GENERATING MASK LAYOUTS

ABSTRACT

A system and method are disclosed for integrating mask layout tools to automate the generation of mask layouts for fabricating an integrated circuit corresponding to an input netlist and a timing specification. The mask layout is generated by the disclosed method including the steps of automatically sizing transistors specified in the netlist, clustering the sized transistors into cells, generating a cell library, and placing-and-routing the cells to generate the mask layout. The system includes associated memory and stored programs, including a plurality of mask layout tools; and a processor operated by an automatic mask layout generation program for sequentially applying the plurality of mask layout tools to generate the mask layout from the input data. The plurality of mask layout tools includes: a transistor sizing tool for sizing transistors and to generate a netlist; a cell library generation tool for generating a cell library from the netlist; a place-and-route tool for generating the mask layout; and optionally a clustering tool for clustering the netlist generated by the transistor sizing tool into a plurality of cells.

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