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Methods and Apparatus for Estimating Time of Arrival of a Pulse in a Train of Pulses in a Ranging System

Field of the Invention

The present invention relates to methods and an apparatus for estimating time of arrival of a pulse in a train of pulses in a ranging system.

Background of the Invention

A pulse-based UWB transceiver system may be used to measure the distance between a target and a transceiver by measuring the time delay between transmitting a signal and receiving it back again. A conventional method of determining the time of arrival of the received signal is to use a sampling clock to sample the receiver output at known time intervals and to count the number of time intervals which occur before the signal is received back after it is transmitted. The TOA is estimated from the counted number of time intervals elapsing between transmission and reception. In systems where the signal comprises a pulse code, the TOA is defined as the phase shift of the pulse code. The maximum delay must not be greater than the pulse code length. However, due to the discrete time sampling and the absence of amplitude correlation among adjacent samples, it is difficult to recover the delay finer than the sampling period. The larger the sampling period, the greater the possible estimation error.

There is a need for an improved apparatus and method of estimating time of arrival of a pulse in a train of pulses in a ranging system which is economical and not complex in its construction and implementation.

Summary of the Invention

In broad terms, the invention provides an apparatus and method of estimating the time of arrival of a pulse in a train of pulses in a ranging system

in which an integrator stage is used to record the time difference between the estimated time of arrival obtained by a sampling method and the actual time of arrival to provide a fine estimate of the time of arrival of the pulses.

According to a first aspect of the present invention there is provided a method of estimating time of arrival of a pulse in a train of pulses in a ranging system, the method comprising the steps of:

- estimating a first value for the time of arrival of a second pulse based on discrete time sampling data obtained by a sampling stage from a first pulse over a predetermined number of time sampling periods; the sampling stage being controlled by a sampling clock;

- defining an observation window time period around the estimated first value for the time of arrival, the observation window having a start time and a finishing time, the observation window having a duration greater than or equal to the time sampling period;

- activating an integrator stage at the start time of the observation window;

- integrating a current to provide an output voltage as a function of time of integration;

- deactivating the integrator stage to cease integration on detection of the arrival of the pulse whose time of arrival is to be estimated; and

- determining a revised time of arrival of the pulse using a time value obtained from the output voltage of the integrator and the estimated first value of the time of arrival.

Preferably, the step of estimating a first value comprises detecting one or more envelopes of one or more incoming pulses, sampling a received pulse waveform at regular intervals and determining a first time of arrival based on discrete sampling data from the sampled pulse.

Preferably, the pulse comprises a pulse code sequence, the step of determining a revised time of arrival further comprising averaging a number of revised times of arrival for subsequent pulse code sequences.

Preferably, the step of integrating comprises integrating the current such that the output of the integrator stage rises linearly with time.

In a preferred embodiment, the method further comprises resetting the integrator stage at the finish time of the observation period.

Preferably, the method further comprises:

- filtering the output of the integrator stage in a low pass filter to obtain a filtered output;

- using the filtered output to control a phase shifter to adjust the sampling clock so as to move the sampling pulse towards an expected time of arrival of a pulse to be received.

In a preferred embodiment, the method further comprises:

- filtering the output of the integrator stage in a low pass filter to obtain a filtered output;

- using the filtered output to control a first voltage control oscillator to adjust the frequency of the sampling clock so as to move the sampling pulse towards an expected time of arrival of a pulse to be received.

Preferably, the method further comprises:

synchronizing the sampling clock to a repetition rate of the pulses in the train of pulses.

Preferably, the synchronizing step comprises:

applying the pulse to an input of a phase detector, the phase detector generate an output signal;

passing the output signal of the phase detector through a low pass filter to generate a filtered output signal;

applying the filtered output signal as a control signal to a voltage control oscillator which produces a sampler frequency output signal;

applying the sampler frequency output signal to a fractional counter to produce an output signal at the same nominal frequency as the frequency of the train of pulses;

applying the output signal of the fractional counter to an input of the phase detector;

comparing in the phase detector the pulse repetition rate of the train of pulses with the frequency of the output signal of the fractional counter;
and

controlling the frequency of the voltage control oscillator using the filtered output signal from the phase detector to lock the sampler frequency to the frequency of the train of pulses.

Preferably, the pulses in the pulse train comprise one or more packets of pulses, each packet comprising a range measuring portion and a waveform recovery portion for synchronizing a sampling clock used for waveform recovery with a transmission pulse clock, the method further comprising the steps of:

applying the pulse to an input of a phase detector, the phase detector being arranged to generate an output signal;

passing the output signal of the phase detector through a low pass filter to generate a filtered output signal;

applying the filtered output signal as a control signal to a voltage control oscillator which produces a sampler frequency output signal;

applying the sampler frequency output signal to a frequency divider to provide an output signal;

applying the output signal of the frequency divider to an input of the phase detector so that the output signal of the voltage control oscillator is controlled to produce a signal having a frequency at the sampling rate of the waveform recovery portion and locked to the pulse repetition rate of the ranging portion;

applying the output signal of the voltage control oscillator to an input of a further phase detector;

filtering in a low pass filter an output signal of the further phase detector to provide a filtered signal which is arranged to control a further voltage control oscillator;

applying an output signal from the further voltage control oscillator to a fractional counter to produce an output signal which is applied to an input of further phase detector;

controlling the frequency of the further voltage control oscillator using the filtered output signal to produce a signal having a frequency which differs from the frequency of the signal output from the first voltage control oscillator but is locked to the frequency of the first voltage control oscillator

and thereby to the frequency of the ranging portion, the ratio of the frequency of the filtered output signal and the frequency of the first voltage control oscillator being set by the fractional counter; the further voltage control oscillator acting as the sampler clock for the waveform recovery portion.

Preferably, the further voltage control oscillator operates at a frequency substantially equal to a multiple of the frequency of the first voltage control oscillator.

In a preferred embodiment, the method further comprises combining in an AND gate the output signals of the first and further voltage control oscillators to produce a signal to initiate a waveform recovery process so that the waveform recovery process is initiated at the same point for each packet.

According to a second aspect of the present invention there is provided an apparatus for estimating time of arrival of a pulse in a train of pulses in a ranging system, the apparatus comprising:

- an estimator for estimating a first value for the time of arrival of a second pulse based on discrete time sampling data obtained by a sampling stage from a first pulse over a predetermined number of time sampling periods; the sampling stage being controlled by a sampling clock;

- a processing stage for defining an observation window time period around the estimated first value for the time of arrival, the observation window having a start time and a finishing time, the observation window having a duration greater than or equal to the time sampling period;

- an integrator stage arranged to be activated at the start time of the observation window to integrate a current to provide an output voltage as a function of time of integration, the integrator stage being arranged to be deactivated to cease integration on detection of the arrival of the pulse whose time of arrival is to be estimated; and

a determination stage for determining a revised time of arrival of the pulse using a time value obtained from the output voltage of the integrator and the estimated first value of the time of arrival.

Preferably, the estimation stage is arranged to detect one or more envelopes of one or more incoming pulses, sample a received pulse waveform at regular intervals and determine a first time of arrival based on discrete sampling data from the sampled pulse.

Preferably, the pulse comprises a pulse code sequence, the determination stage being arranged to determine a revised time of arrival by averaging a number of revised times of arrival for subsequent pulse code sequences.

Preferably, the integrator stage is arranged to integrate the current such that the output of the integrator stage rises linearly with time.

Preferably, the integrator stage is arranged to be reset at the finish time of the observation period.

In a preferred embodiment, the apparatus further comprises:

- a low pass filter for filtering the output of the integrator stage to obtain a filtered output;

- a phase shifter arranged to be controlled using the filtered output to adjust the sampling clock so as to move the sampling pulse towards an expected time of arrival of a pulse to be received.

In a further preferred embodiment, the apparatus further comprises:

- a low pass filter for filtering the output of the integrator stage to obtain a filtered output;

a first voltage control oscillator arranged to be controlled using the filtered output to adjust the frequency of the sampling clock so as to move the sampling pulse towards an expected time of arrival of a pulse to be received.

Preferably, the apparatus further comprises:

a synchronization stage for synchronizing the sampling clock to a repetition rate of the pulses in the train of pulses.

Preferably, the synchronizing stage comprises:

a phase detector having an input to which a pulse in the pulse train is applied, the phase detector being arranged to generate an output signal;

a low pass filter arranged to receive the output signal of the phase detector to generate a filtered output signal;

a first voltage control oscillator arranged to receive the filtered output signal as a control signal to produce a sampler frequency output signal;

a fractional counter arranged to receive the sampler frequency output signal to produce an output signal at the same nominal frequency as the frequency of the train of pulses; the fractional counter being arranged to apply the output signal to an input of the phase detector;

the phase detector being arranged to compare the pulse repetition rate of the train of pulses with the frequency of the output signal of the fractional counter; and

a control stage for controlling the frequency of the voltage control oscillator using the filtered output signal from the phase detector to lock the sampler frequency to the frequency of the train of pulses.

Preferably, the pulses in the pulse train comprise one or more packets of pulses, each packet comprising a range measuring portion and a waveform recovery portion, the apparatus further comprising:

- a phase detector having an input for receiving the pulse train, the phase detector being arranged to generate an output signal;

- a low pass filter for filtering the output signal of the phase detector to generate a filtered output signal;

- a voltage control oscillator arranged to receive the filtered output signal as a control signal to produce a sampler frequency output signal;

- a frequency divider arranged to receive the sampler frequency output signal to provide an output signal;

- the output signal of the frequency divider being arranged to be applied to an input of the phase detector so that the output signal of the voltage control oscillator is controlled to produce a signal having a frequency at the sampling rate of the waveform recovery portion and locked to the pulse repetition rate of the ranging portion;

- a further phase detector arranged to receive the output signal of the voltage control oscillator;

- a further low pass filter for filtering an output signal of the further phase detector to provide a filtered signal which is arranged to control a further voltage control oscillator;

- a fractional counter arranged to receive an output signal from the further voltage control oscillator to produce an output signal which is applied to an input of further phase detector; and

a control stage for controlling the frequency of the further voltage control oscillator using the filtered output signal to produce a signal having a frequency which differs from the frequency of the signal output from the first voltage control oscillator but is locked to the frequency of the first voltage control oscillator and thereby to the frequency of the ranging portion, the ratio of the frequency of the filtered output signal and the frequency of the first voltage control oscillator being set by the fractional counter; the further voltage control oscillator acting as the sampler clock for the waveform recovery portion.

Preferably, the further voltage control oscillator operates at a frequency substantially equal to a multiple of the frequency of the first voltage control oscillator.

Preferably, the apparatus further comprises an AND gate arranged to combine the output signals of the first and further voltage control oscillators to produce a signal to initiate a waveform recovery process so that the waveform recovery process is initiated at the same point for each packet.

Thus, one or more embodiments provide the ability to distinguish a time delay difference based on large step-size signal samples, which have very low amplitude relationships to each other. The recovered timing accuracy is independent of the sampling step-size and therefore the signal sampling period may be large, which enable the hardwares to be less complex. Furthermore, there is no need for a high-speed multi-bit A/D converter and a low speed multi-bit A/D may be used.

Also, in one or more preferred embodiments in a packet pulse system where it is necessary to recover the waveform, the sampling clock for waveform recovery may be locked to the pulse repetition frequency of the ranging section which serves to improve stability of the recovery waveform and enables the starting point of the recovery process to be consistent from

packet-to-packet.

A pulse-based UWB transceiver system embodying the invention may be used to produce an active reflector device without a delay between transmitting and receiving of the signal to be reflected, thereby improving ranging accuracy.

Brief Description of the Drawings

The present invention will now be described by way of example and with reference to the accompanying drawings in which:

Figure 1(a) is a waveform of a received signal of a coded sequence as used in an UWB pulse transceiver;

Figure 1(b) is a waveform of the received signal of Figure 1(a) after envelope detection and shows sampling intervals;

Figure 1(c) is a diagram showing the output of a sampling stage and an indication of the differences between real TOA and estimated TOA;

Figure 2 is a diagram showing the observation window and envelope of a received pulse, and the times to trigger an integrator on/off to provide a fine TOA estimation;

Figure 3 is a block diagram of an integrator stage for obtaining a fine TOA estimation;

Figure 4 is a block diagram of a phase locked loop (PLL) application of the integrator based TOA estimation;

Figure 5(a) is a waveform showing a conventional waveform recovering scheme using a very low sampling speed;

Figure 5(b) is a block diagram of a synchronizing apparatus according to a preferred embodiment, for the sampler clock in a low speed waveform recovering method; and

Figure 6 is a block diagram and timing diagram of apparatus for aligning the clocks of the ranging pulse sequence and the waveform recovering sampler.

Detailed Description of Preferred Embodiments

Figures 1(a) to 1(c) show a conventional method of finding the time of arrival of a pulse. Figure 1(a) shows a waveform of a received signal of a coded sequence as used in an UWB pulse transceiver. Conventionally, the waveform of Figure 1 (a) is smoothed through an envelope detector or low pass filter. The resulting waveform is then sampled at regular intervals, as shown in Figure 1(b), to give a sampled output as shown in Figure 1(c). Figure 1(c) also shows the real arrival time and estimated arrival time to indicate the difference therebetween which is due to the discrete time sampling step and low time resolution the sampler.

The time of arrival (TOA) of the pulse is estimated based on the discrete samples, and is defined as the phase shift of the pulse code. The maximum delay should not be greater than the pulse code length. Such a system can only resolve the time of arrival to between two adjacent samples. Thus, the longer the sampling step, the greater the possible estimation error. A first preferred embodiment of the present invention aims to solve this problem. In this embodiment, for a periodic coded UWB pulse, the TOA is firstly estimated using a conventional method. From this, subsequently an integrator is initiated by a sample pulse prior to the estimated TOA and terminated by the arrival of the received pulse, as shown in Figure 2. As the estimated TOA, τ is averaged over many pulse code periods, it is relatively stable. However, τ is time discrete and hence there may be an error between the estimated TOA and the actual time of arrival. To correct for this error an observation window

based on τ is first defined. The start point of the observation window is $\tau - T$, where T is an integer multiple of τ .

For a periodic coded pulse sequence, after the common TOA estimation output becomes stable, the integrator is switched on at the start point of the observation window in the next coded pulse sequence period. When the first pulse arrives after the start point, the integrator is triggered off and the integration stops. The integrator output voltage $\{A\}$ is proportional to the delay from $\tau - T$ to the real TOA. The time-to-voltage ratio (dependent on the current: I) may be denoted by α , and the corrected TOA estimation may be denoted by:

$$\tau_c = \tau - T + \alpha A \quad (1)$$

In every period for the coded pulse sequence, τ_c is updated once. The output TOA is an averaged result over several periods which may reduce the effect of occasional errors due to incorrect detection of signal pulses.

Figure 3 shows a block diagram of an apparatus 1 according to a preferred embodiment of the invention for implementing the integrator based TOA estimator technique of Figure 2. The received signal, after preprocessing to produce the envelope of the signal, is applied to the input of a threshold comparison stage 2. The output of the threshold comparison stage 2 is applied to a switch 4 controlling the current 6 to an integrator 8. The envelope is also applied to a common sampling TOA estimation stage 10, the output of which is also applied to the switch 4 controlling the current 6 into the integrator 8. The output of the integrator 8 is applied to the input of a voltage read stage 12 which applies an output to clear the integrator 8 after reading.

The threshold comparison stage 2 ensures that each detected pulse in a sequence turns the switch 4 off to prevent current passing to the integrator 8. Once the common sampling TOA estimation stage 10 has stabilized to determine the approximate TOA, this stage emits a pulse at a time $\tau - T$ to turn the switch 4 on thus allowing the current 6 to be applied to the integrator 8, the output of which then rises linearly with time. The next received pulse from the threshold comparison stage 2 turns the current 6 off and the output of the integrator 8 remains constant.

At the end of the observation window, the voltage at the output of the integrator 8 is read by the voltage read stage 12 and the integrator 8 is cleared. The output as read by the voltage read stage 12 is then converted to the time domain and the resulting period is added to the time $\tau - T$ to produce a corrected TOA τ_c . After the correction, the TOA estimation will be a continuous value. The time resolution is independent of the sampling rate. However, the greater the sampling step, the longer the integrating time.

Another preferred embodiment of the invention is shown in Figure 4. In this embodiment, a phase locked loop (PLL) is formed by combining the apparatus of Figure 3 with a phase shifter or voltage control oscillator (VCO). The common components in the apparatus of Figures 3 and 4 are denoted by the same reference numerals.

Figure 4 shows a block diagram of an apparatus according to a second preferred embodiment in which the voltage read stage 12 of Figure 3 comprises a low speed digital to analogue converter which operates once after the true time of arrival of a pulse is reached and acts to clear the integrator 8. The output voltage 14 from the integrator 8 is applied to a low pass filter 16 and the output of the low pass filter 16 controls a phase shifter 18 which shifts the phase of the output of a sampling clock 20.

In operation, the output of the integrator 8 shifts the phase of the sampling clock 20 such that the sampling pulse moves towards the true TOA thereby reducing the TOA estimation error to a very low value. The output of the phase shifter 18 is also applied to a reply pulse sequence generator 22.

The apparatus of Figure 4 may be used in an active pulse sequence reflector.

Conventionally, a true passive reflector, such as a wall, may instantly reflect the pulse sequence. However, the passive reflector will greatly attenuate the signal strength. To overcome the shortcomings of a passive reflector, an active reflector may be used. An active reflector will generate the same pulse sequence as it receives and retransmit it.

A simple active reflector may be a pulse generator plus a pulse detector. Once the detector detects a pulse, the active reflector just generates a single pulse and retransmits it. This type of active reflector is basic. As it does not carry out pulse sequence detection and synchronization, the reflection contents are very easily corrupted by random noise. If occasional noise is wrongly detected, it will be permanently regarded as a pulse and will be transmitted at the same strength and shape as the real pulse. This type of error is very difficult to handle in the final signal processing.

Another type of active reflector which is more robust than that described above first samples the received signal and recovers the timing of the pulse code using code correlation processing. As code correlation is adopted, the pulse is detected code by code (a code consists of a number of pulses instead of a single pulse) thereby reducing the chance of error in the transmitted pulse sequence. However, as a sampler and clock such as that used in the receiver is used before the processing, and the reply sequence is transmitted using the same clock, an uncertain delay may be introduced. This may affect system performance.

The PLL arrangement of Figure 4 may be used to solve the uncertain delay problem. The output 14 of the integrator 8 is proportional to the uncertain delay, and after passing through the low-pass filter 16 to remove occasional noise, this delay information will control the phase shift or the VCO of the sampler 20 in real time, to adjust the sample clock pulse to approach the real TOA of the received pulse. Therefore the active reflector is now more like a real reflector without delay and its reflection is more reliable.

In a packet pulse based UWB system, ranging and waveform recovery are usually implemented in different parts of the packet. Moreover, the pulse periods for the two parts are different to each other. When it is desired to bring the ranging information to the waveform recovery part, that is, to indicate the acquisition point (i.e. the detected timing point in a pulse period; the acquisition point is related to the fine TOA estimation) of the ranging in a pulse waveform, the pulse repetition clock in the ranging part should be aligned with the sampler clock for waveform recovery.

In a conventional method, waveform recovery may be achieved by using a sampler frequency, which is close to but a little different from the pulse repetition rate, as shown in Figure 5(a) which illustrates a pulse envelope of a received signal in an UWB system at a repetition rate of f_1 . A sampling sequence having a sampling rate f_2 is also shown in Figure 5(a). After many pulse periods, one pulse is scanned and rebuilt. However, in such a conventional method, the sampler clock is independent of the pulse repetition clock, which causes the recovered pulse sequence period to be unstable.

According to a further preferred embodiment of the invention, synchronization of the sampling frequency f_2 to the incoming frequency f_1 is generated by a fractional PLL structure shown in Figure 5(b).

The fractional PLL structure shown in Figure 5(b) comprises a phase detector 30 for receiving an incoming waveform signal, the output of the phase detector

30 being filtered in a low pass filter 32. The output of the low pass filter 32 is applied to an input of a VCO 34 to control its frequency of oscillation. The output of the VCO 34 is applied to the input of an f_1 f_2 fractional counter 36 to provide an output at the same frequency as f_1 which is applied to a further input of the phase detector 30. The VCO 34 also provides an output at a frequency f_2 which is a stable sampler frequency synchronized to the transmitted pulse repetition rate. This output is applied to a sampling stage (not shown). In this embodiment, the generated frequency f_2 is locked to the frequency f_1 , although f_1 is different from f_2 . In other words, if f_1 is not stable, f_2 will follow f_1 and, in this way, the rebuilt waveform is stable.

Another preferred embodiment is shown in Figure 6 which aims to further align the clock for the pulse sequence to the ranging and the sampler clock for the waveform recovery part. The pulses for the ranging part of the sequence are applied to an input of a phase detector 40. The output of the phase detector 40 is applied to the input of a low pass filter 42. The output of the low pass filter 42 is applied to an input of a VCO 44 to control its frequency of oscillation. One output of the VCO 44 is applied to an input of the divider stage 46, the output of which is applied to a further input of the phase detector 40. A further output of the VCO 44 is applied to an input of an AND gate 48 and another output from the VCO 44 is applied to a second phase detector 50. The output of the second phase detector 50 is filtered in a low pass filter 52 and the output of the low pass filter 52 is applied to the input of a further VCO 54. The output of the further VCO 54 is applied to a fractional counter 56, the output of which is applied to a further input of the second phase detector 50. The output of the VCO 54 is also connected to the other input of the AND gate 48. The output of the AND gate 48 acts as a pulse to start the sampling process for the recovery of the waveform.

If the pulse repetition rate for the ranging portion of the pulse packet is, for example, 50KHz and the pulse repetition rate for the waveform recovery part

is 20MHz and the sampler clock rate is 19.998MHz, the 20MHz output from the first VCO 44 is divided in the 'divide by 400' stage 46 to produce a 50KHz waveform which is compared to the incoming waveform in the ranging portion of the packet in the phase detector 40. Any phase difference between the two signals will, after filtering in the low pass filter 42, control the frequency of the VCO 44 to reduce the phase difference between the signals so that the 20 MHz output from the VCO 44 will follow any variation in the frequency of the ranging portion of the incoming waveform.

Furthermore, the output of the second VCO 54 which may be at 19.998MHz or 39.996MHz, will be divided by the fractional counter 56 to produce a 20MHz signal which is compared in the phase detector 50 with the output from the VCO 44. Any phase difference between these two signals causes an output which, after filtering in the low pass filter 52, will provide a signal to the VCO 54 to remove the phase error. Thus the output of the VCO 54 which is used for sampling in the waveform recovery section will track any variation in the frequency of the incoming waveform.

The start point of the waveform recovery in a packet is triggered by the output of the AND gate 48. This is to ensure that the recovered waveform will have the same start point for every packet.

One or more preferred embodiments are particularly advantageous as they provide a continuous TOA estimation which is independent of the sampler step-size when the sampling period is smaller than the pulse repetition period. The hardware complexity may be reduced due to the adoption of a low speed sampler. In such an embodiment, an integrator may be used to provide a fine correction to the TOA estimation to provide an accurate estimate, which is particularly advantageous in a discrete time sampling UWB communication and positioning system. The system, however, remains simple because the sampler speed is not required to be

increased. One or more preferred embodiments additionally may align the ranging and the waveform recovery parts in a packet UWB system to improve the stability of the system's performance in low sampling rate waveform recovery schemes.

Various modifications to the embodiments of the present invention described above may be made. For example, other components and method steps can be added or substituted for those above. Thus, although the invention has been described above using particular embodiments, many variations are possible within the scope of the claims, as will be clear to the skilled reader, without departing from the scope of the invention.

Claims

1. A method of estimating time of arrival of a pulse in a train of pulses in a ranging system, the method comprising the steps of:

estimating a first value for the time of arrival of a second pulse based on discrete time sampling data obtained by a sampling stage from a first pulse over a predetermined number of time sampling periods; the sampling stage being controlled by a sampling clock;

defining an observation window time period around the estimated first value for the time of arrival, the observation window having a start time and a finishing time, the observation window having a duration greater than or equal to the time sampling period;

activating an integrator stage at the start time of the observation window;

integrating a current to provide an output voltage as a function of time of integration;

deactivating the integrator stage to cease integration on detection of the arrival of the pulse whose time of arrival is to be estimated; and

determining a revised time of arrival of the pulse using a time value obtained from the output voltage of the integrator and the estimated first value of the time of arrival.

2. A method according to claim 1, wherein the step of estimating a first value comprises detecting one or more envelopes of one or more incoming pulses, sampling a received pulse waveform at regular intervals and

determining a first time of arrival based on discrete sampling data from the sampled pulse.

3. A method according to claim 1, wherein the pulse comprises a pulse code sequence, the step of determining a revised time of arrival further comprising averaging a number of revised times of arrival for subsequent pulse code sequences.

4. A method according to claim 1, wherein the step of integrating comprises integrating the current such that the output of the integrator stage rises linearly with time.

5. A method according to claim 1, further comprising resetting the integrator stage at the finish time of the observation period.

6. A method according to claim 1, further comprising:

filtering the output of the integrator stage in a low pass filter to obtain a filtered output;

using the filtered output to control a phase shifter to adjust the sampling clock so as to move the sampling pulse towards an expected time of arrival of a pulse to be received.

7. A method according to claim 1, further comprising:

filtering the output of the integrator stage in a low pass filter to obtain a filtered output;

using the filtered output to control a first voltage control oscillator to adjust the frequency of the sampling clock so as to move the sampling pulse towards an expected time of arrival of a pulse to be received.

8. A method according to claim 1, further comprising:

synchronizing the sampling clock to a repetition rate of the pulses in the train of pulses.

9. A method according to claim 8, wherein the synchronizing step comprises:

applying the pulse to an input of a phase detector, the phase detector generate an output signal;

passing the output signal of the phase detector through a low pass filter to generate a filtered output signal;

applying the filtered output signal as a control signal to a voltage control oscillator which produces a sampler frequency output signal;

applying the sampler frequency output signal to a fractional counter to produce an output signal at the same nominal frequency as the frequency of the train of pulses;

applying the output signal of the fractional counter to an input of the phase detector;

comparing in the phase detector the pulse repetition rate of the train of pulses with the frequency of the output signal of the fractional counter; and

controlling the frequency of the voltage control oscillator using the filtered output signal from the phase detector to lock the sampler frequency to the frequency of the train of pulses.

10. A method according to claim 1, wherein the pulses in the pulse train comprise one or more packets of pulses, each packet comprising a range measuring portion and a waveform recovery portion, the method further comprising the steps of:

applying the pulse to an input of a phase detector, the phase detector being arranged to generate an output signal;

passing the output signal of the phase detector through a low pass filter to generate a filtered output signal;

applying the filtered output signal as a control signal to a voltage control oscillator which produces a sampler frequency output signal;

applying the sampler frequency output signal to a frequency divider to provide an output signal;

applying the output signal of the frequency divider to an input of the phase detector so that the output signal of the voltage control oscillator is controlled to produce a signal having a frequency at the sampling rate of the waveform recovery portion and locked to the pulse repetition rate of the ranging portion;

applying the output signal of the voltage control oscillator to an input of a further phase detector;

filtering in a low pass filter an output signal of the further phase detector to provide a filtered signal which is arranged to control a further voltage control oscillator;

applying an output signal from the further voltage control oscillator to a fractional counter to produce an output signal which is applied to an input of further phase detector;

controlling the frequency of the further voltage control oscillator using the filtered output signal to produce a signal having a frequency which differs from the frequency of the signal output from the first voltage control oscillator but is locked to the frequency of the first voltage control oscillator

and thereby to the frequency of the ranging portion, the ratio of the frequency of the filtered output signal and the frequency of the first voltage control oscillator being set by the fractional counter; the further voltage control oscillator acting as the sampler clock for the waveform recovery portion.

11. A method according to claim 10, wherein the further voltage control oscillator operates at a frequency substantially equal to a multiple of the frequency of the first voltage control oscillator.

12. A method according to claim 10, further comprising combining in an AND gate the output signals of the first and further voltage control oscillators to produce a signal to initiate a waveform recovery process so that the waveform recovery process is initiated at the same point for each packet.

13. An apparatus for estimating time of arrival of a pulse in a train of pulses in a ranging system, the apparatus comprising:

an estimator for estimating a first value for the time of arrival of a second pulse based on discrete time sampling data obtained by a sampling stage from a first pulse over a predetermined number of time sampling periods; the sampling stage being controlled by a sampling clock;

a processing stage for defining an observation window time period around the estimated first value for the time of arrival, the observation window having a start time and a finishing time, the observation window having a duration greater than or equal to the time sampling period;

an integrator stage arranged to be activated at the start time of the observation window to integrate a current to provide an output voltage as a function of time of integration, the integrator stage being arranged to be deactivated to cease integration on detection of the arrival of the pulse whose time of arrival is to be estimated; and

a determination stage for determining a revised time of arrival of the pulse using a time value obtained from the output voltage of the integrator and the estimated first value of the time of arrival.

14. An apparatus according to claim 13, wherein the estimation stage is arranged to detect one or more envelopes of one or more incoming pulses, sample a received pulse waveform at regular intervals and determine a first time of arrival based on discrete sampling data from the sampled pulse.

15. An apparatus according to claim 13, wherein the pulse comprises a pulse code sequence, the determination stage being arranged to determine a revised time of arrival by averaging a number of revised times of arrival for subsequent pulse code sequences.

16. An apparatus according to claim 13, wherein the integrator stage is arranged to integrate the current such that the output of the integrator stage rises linearly with time.

17. An apparatus according to claim 13, wherein the integrator stage is arranged to be reset at the finish time of the observation period.

18. An apparatus according to claim 13, further comprising:

a low pass filter for filtering the output of the integrator stage to obtain a filtered output;

a phase shifter arranged to be controlled using the filtered output to adjust the sampling clock so as to move the sampling pulse towards an expected time of arrival of a pulse to be received.

19. An apparatus according to claim 13, further comprising:

a low pass filter for filtering the output of the integrator stage to obtain a filtered output;

a first voltage control oscillator arranged to be controlled using the filtered output to adjust the frequency of the sampling clock so as to move the sampling pulse towards an expected time of arrival of a pulse to be received.

20. An apparatus according to claim 13, further comprising:

a synchronization stage for synchronizing the sampling clock to a repetition rate of the pulses in the train of pulses.

21. An apparatus according to claim 20, wherein the synchronizing stage comprises:

a phase detector having an input to which a pulse in the pulse train is applied, the phase detector being arranged to generate an output signal;

a low pass filter arranged to receive the output signal of the phase detector to generate a filtered output signal;

a first voltage control oscillator arranged to receive the filtered output signal as a control signal to produce a sampler frequency output signal;

a fractional counter arranged to receive the sampler frequency output signal to produce an output signal at the same nominal frequency as the frequency of the train of pulses; the fractional counter being arranged to apply the output signal to an input of the phase detector;

the phase detector being arranged to compare the pulse repetition rate of the train of pulses with the frequency of the output signal of the fractional counter; and

a control stage for controlling the frequency of the voltage control oscillator using the filtered output signal from the phase detector to lock the sampler frequency to the frequency of the train of pulses.

22. An apparatus according to claim 13, wherein the pulses in the pulse train comprise one or more packets of pulses, each packet comprising a range measuring portion and a waveform recovery portion, the apparatus further comprising:

a phase detector having an input for receiving the pulse train, the phase detector being arranged to generate an output signal;

a low pass filter for filtering the output signal of the phase detector to generate a filtered output signal;

a voltage control oscillator arranged to receive the filtered output signal as a control signal to produce a sampler frequency output signal;

a frequency divider arranged to receive the sampler frequency output signal to provide an output signal;

the output signal of the frequency divider being arranged to be applied to an input of the phase detector so that the output signal of the voltage control oscillator is controlled to produce a signal having a frequency at the sampling rate of the waveform recovery portion and locked to the pulse repetition rate of the ranging portion;

a further phase detector arranged to receive the output signal of the voltage control oscillator;

a further low pass filter for filtering an output signal of the further phase detector to provide a filtered signal which is arranged to control a further voltage control oscillator;

a fractional counter arranged to receive an output signal from the further voltage control oscillator to produce an output signal which is applied to an input of further phase detector; and

a control stage for controlling the frequency of the further voltage control oscillator using the filtered output signal to produce a signal having a frequency which differs from the frequency of the signal output from the first voltage control oscillator but is locked to the frequency of the first voltage control oscillator and thereby to the frequency of the ranging portion, the ratio of the frequency of the filtered output signal and the frequency of the first voltage control oscillator being set by the fractional counter; the further voltage control oscillator acting as the sampler clock for the waveform recovery portion.

23. An apparatus according to claim 22, wherein the further voltage control oscillator operates at a frequency substantially equal to a multiple of the frequency of the first voltage control oscillator.

24. An apparatus according to claim 22, further comprising an AND gate arranged to combine the output signals of the first and further voltage control oscillators to produce a signal to initiate a waveform recovery process so that the waveform recovery process is initiated at the same point for each packet.