ABSTRACT

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The present invention relates to a smart integrated circuit.

This smart integrated circuit is characterized in that it has a main processor (1) and an operating system executing a main program (P1) for constituting a main task-performing process, at least one secondary processor (2) capable of concurrently executing at least one secondary program (P2) for constituting at least one task-performing process, power supply circuits (6) common to the processors and means for ensuring that the secondary processor or processors with similar power and different operating signatures are executed concurrently with the main process by continuously or intermittently inducing, in the power supply circuits, power disturbances that are superimposed on those of the main process so as to produce a continuous or intermittent scrambling.

Fig. 1