FIG. 1

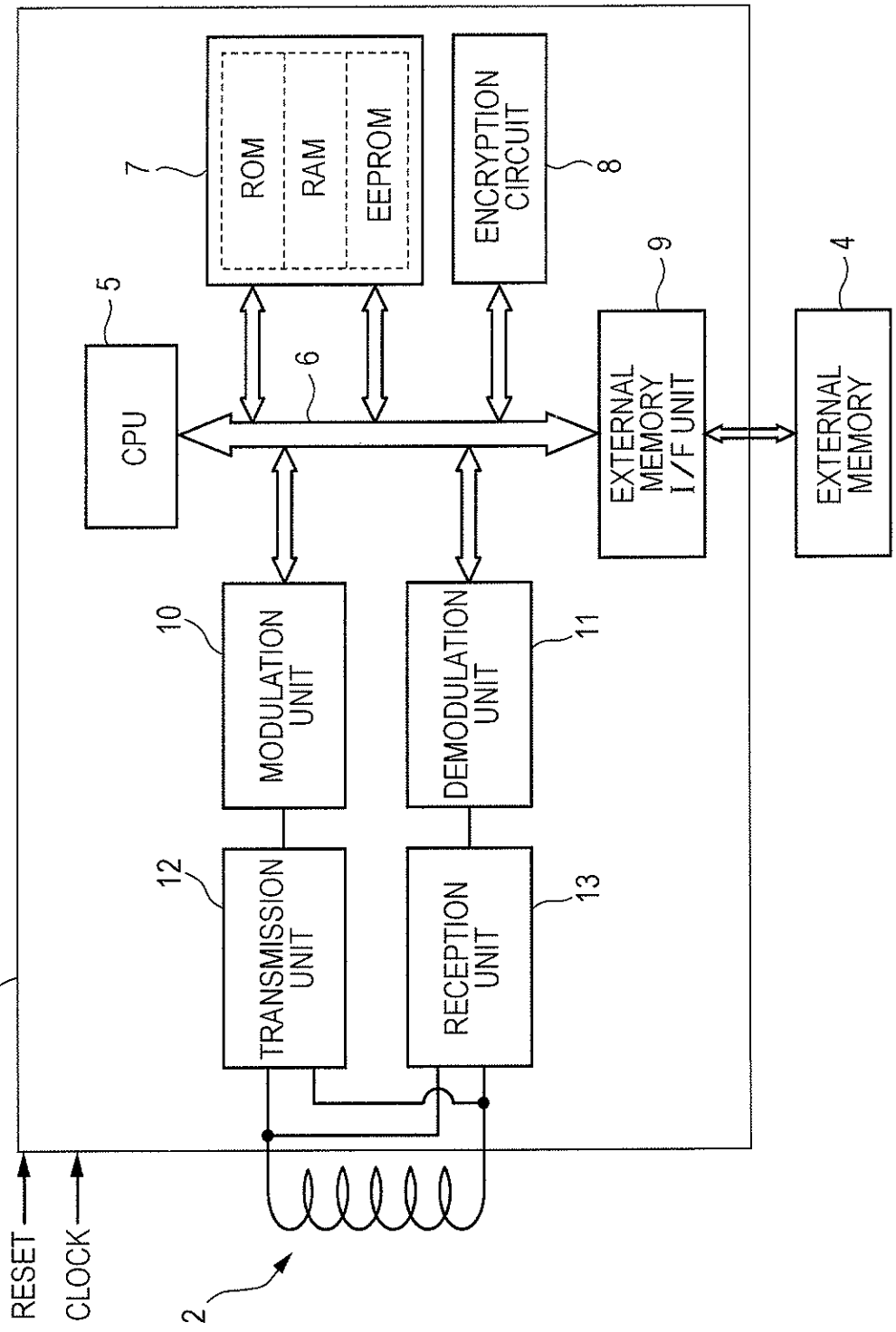

1
3
RESET
CLOCK
2
CPU
5
6
7
ROM
RAM
EEPROM
ENCRYPTION CIRCUIT
8
9
EXTERNAL MEMORY I/F UNIT
4
EXTERNAL MEMORY
10
MODULATION UNIT
11
DEMODULATION UNIT
12
TRANSMISSION UNIT
13
RECEPTION UNIT

FIG. 2

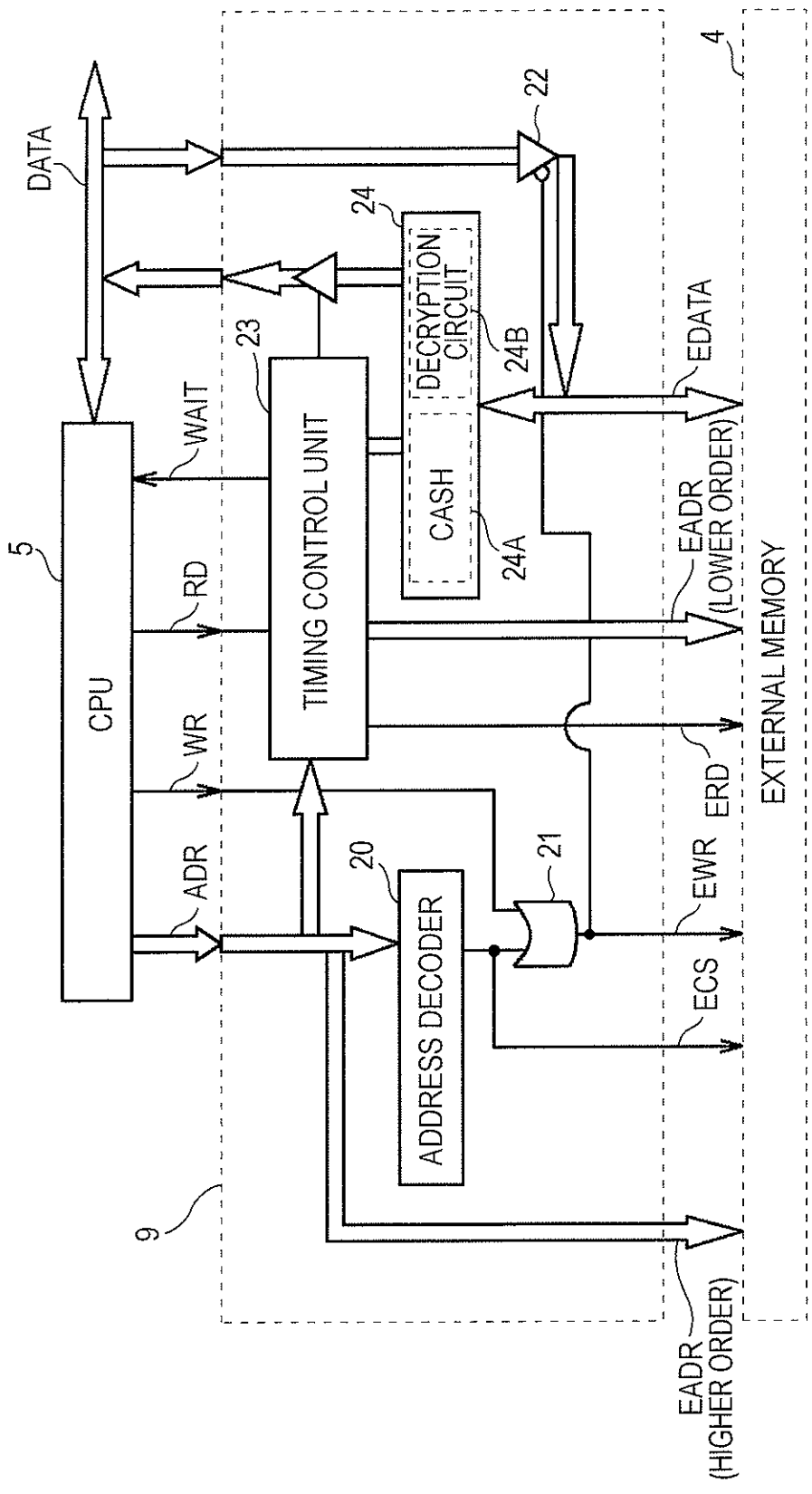

DATA
22
4
24
DECRYPTION CIRCUIT
24B
EDATA
23
WAIT
TIMING CONTROL UNIT
CASH
24A
EADR (LOWER ORDER)
5
CPU
RD
WR
ERD
EXTERNAL MEMORY
ADR
20
21
EWR
ADDRESS DECODER
ECS
9
EADR (HIGHER ORDER)

FIG. 3

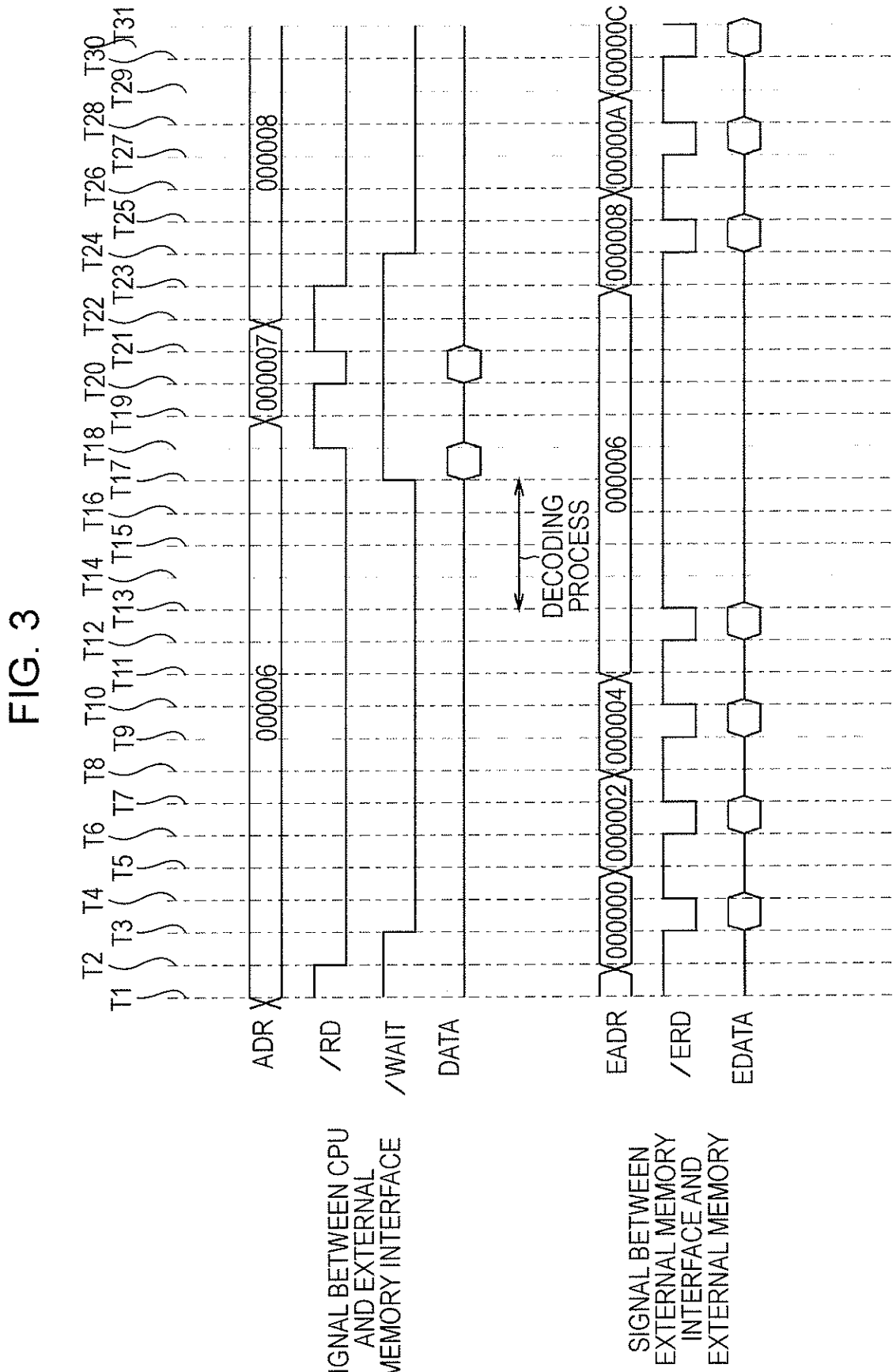
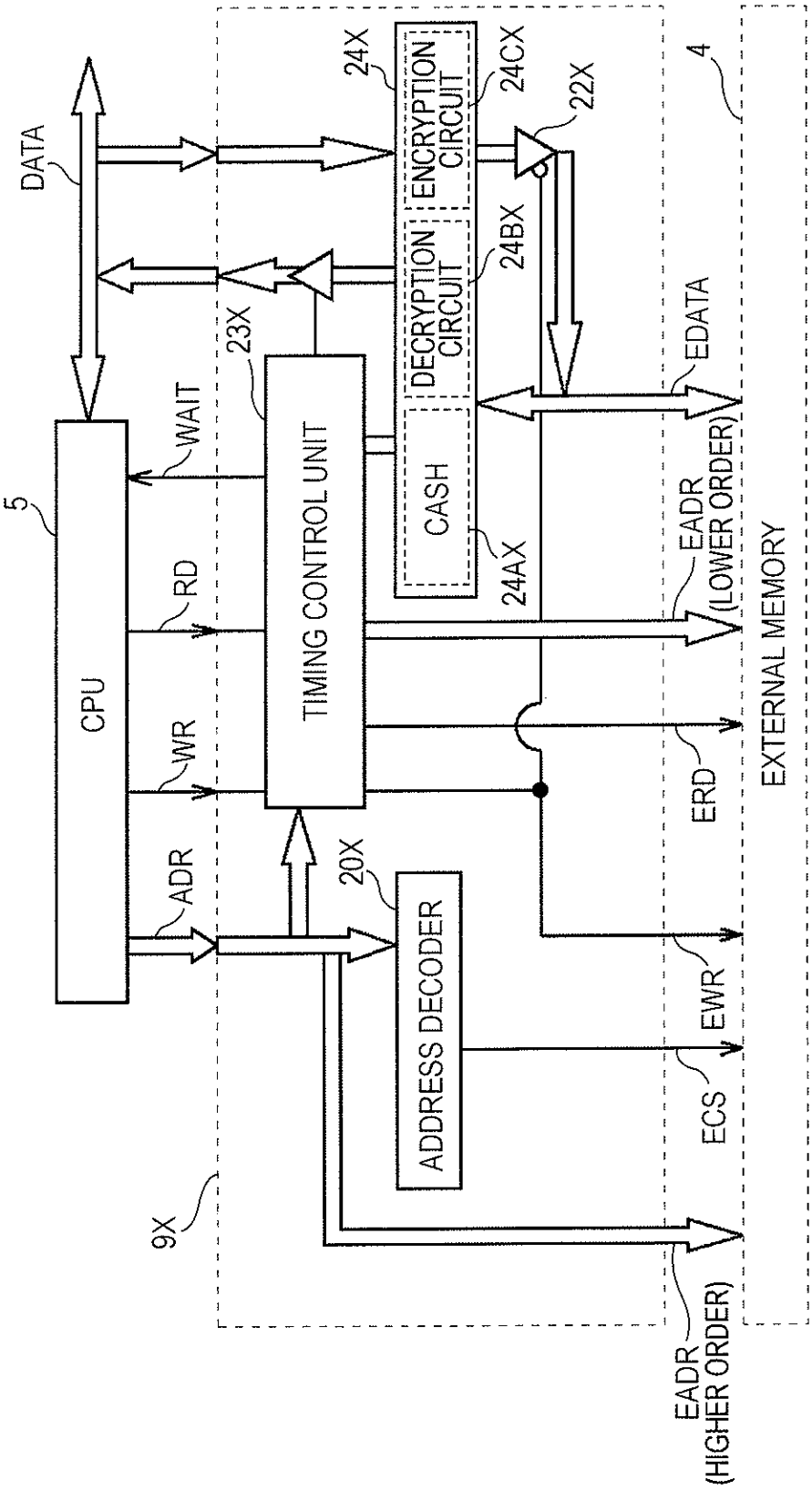

T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
T19
T20
T21
T22
T23
T24
T25
T26
T27
T28
T29
T30
T31
ADR
/RD
/WAIT
DATA
000006
000007
000008
DECODING PROCESS
SIGNAL BETWEEN CPU AND EXTERNAL MEMORY INTERFACE
EADR
/ERD
EDATA
000000
000002
000004
000006
000008
00000A
00000C
SIGNAL BETWEEN EXTERNAL MEMORY INTERFACE AND EXTERNAL MEMORY

FIG. 4


DATA
24X
ENCRYPTION CIRCUIT
24CX
22X
4
DECRYPTION CIRCUIT
24BX
EDATA
23X
WAIT
5
CPU
TIMING CONTROL UNIT
CASH
24AX
EADR (LOWER ORDER)
RD
WR
ERD
EXTERNAL MEMORY
ADR
20X
ADDRESS DECODER
EWR
ECS
9X
EADR (HIGHER ORDER)