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- (54) **Title:** SPARSE OPTIMIZATIONS FOR A MATRIX ACCELERATOR ARCHITECTURE

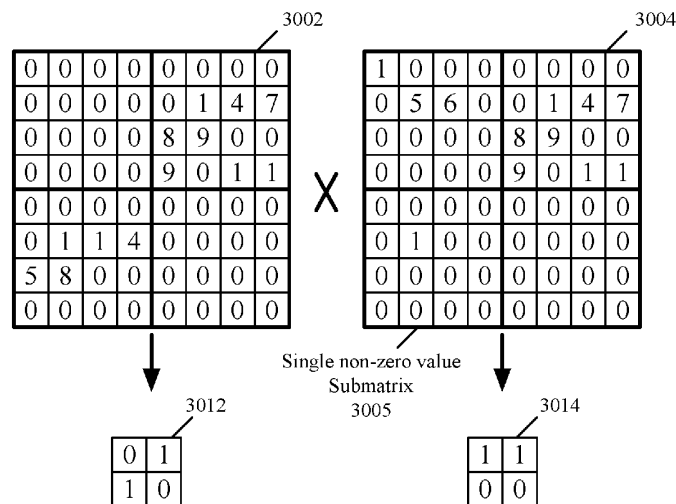


FIG. 30A

- (57) **Abstract:** Embodiments described herein include, software, firmware, and hardware logic that provides techniques to perform arithmetic on sparse data via a systolic processing unit. Embodiment described herein provided techniques to skip computational operations for zero filled matrices and sub-matrices. Embodiments additionally provide techniques to maintain data compression through to a processing unit. Embodiments additionally provide an architecture for a sparse aware logic unit.

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