

- 1 -

Resin sealing type semiconductor device in which a very small semiconductor chip is sealed in package with resin

The present invention relates to a resin sealing type semiconductor device wherein a very small semiconductor chip is sealed in a package with resin.

Semiconductor chips have been reduced in size in accordance with miniaturization of elements. Generally, as the size of a semiconductor chip decreases, the mechanical stress thereof lowers and thus the semiconductor chip is more difficult to be broken. The small semiconductor chip is more reliable about a variation in temperature than a large one and it can be manufactured at low cost. Using small semiconductor chips, a semiconductor device whose operating speed is high, power consumption is low, and electrical characteristic are good, can be achieved.

Fig. 1 is a cross sectional view showing a semiconductor device in which a very small semiconductor chip having the above-described features is sealed with resin. Semiconductor chip 12 is die-bonded onto bed 11 of a lead frame, lead 13 of the lead frame is connected to electrode pad 14 on chip 12 by bonding wire 15 and they are sealed in with mold resin 16. Since the lead frame to be processed is limited in size, lead 13 cannot be arranged sufficiently close to semiconductor chip 12 and inevitably bonding wire 15 is lengthened.

Although bonding wire 15 is in a correct position before the semiconductor chip is sealed in with resin,



it is deformed by the pressure exerted during the resin sealing as indicated by broken line A in Fig. 1 and is brought into contact with another bonding wire. There is a strong possibility that bonding wire 15 becomes defective.

As one of methods for solving the above problem, it is known to connect chip 12 and lead 13 by TAB (Tape Automated Bonding) tape 21 using a TAB technique, as shown in Fig. 2. The TAB technique is as follows. TAB tape 21 is formed by sticking electrode pad 14 and a thin-film wire made of Cu or the like corresponding to lead 13 on a resin film, and the TAB tape allows electrode pad 14 and lead 13 to be bonded at once.

TAB tape 21 is resistible to the pressure exerted when the chip is sealed in with resin and thus not deformed. Since electrode pad 14 and lead 13 can be bonded at once, the productivity of semiconductor devices is high. According to the TAB technique, however, a bump (projected electrode) 22 needs to be formed on electrode pad 14 so that the electrode pad does not contact the edge of the chip or the chip is not damaged by the bonding operation, and a special device for forming the bump is required. For this reason, an equipment investment in manufacturing process increases the manufacturing cost and it is economically difficult to apply the TAB technique to the semiconductor device of the present invention whose price is low.

It is accordingly a first object of the present invention to provide a resin sealing type semiconductor device which prevents defects from being caused by deformation of a wire when a semiconductor chip is sealed in with resin and which can thus be manufactured at relatively low cost. It is a second object of the present invention to provide a resin sealing type semiconductor device which suppresses an increase in cost of equipment investment in manufacturing process and whose manufacturing cost is relatively low, reliability is



high and productivity is high.

To attain the first object of the present invention, there is provided a resin sealing type semiconductor device comprising:

5 a semiconductor chip on the surface of which a plurality of electrodes is arranged;

a bed fixed to the semiconductor chip;

10 a printed circuit board which is fixed to a periphery of at least one of a surface and an undersurface of the bed so as to overhang from the bed and on a surface of which a wiring pattern is formed;

a plurality of lead frames arranged so as to surround the bed;

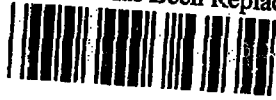
15 first connecting means for connecting the electrodes arranged on the semiconductor chip and one end of the wiring pattern formed on the printed circuit board; and

20 second connecting means for connecting the lead frames and the other end of the wiring pattern formed on the printed circuit board.

25 With the above structure of the semiconductor device, an interval between the bed and each of the leads can be supplemented with the printed circuit board which is fixed so as to overhang from the bed and on which the wiring pattern is formed. The distance between the electrode pads and the printed circuit board is thus shortened. Since the semiconductor chip and the leads are connected via the substrate, the reliability of the semiconductor device becomes high without
30 adopting the TAB technique wherein bumps need to be formed on the chip when the chip and leads are directly connected to each other.

To attain the second object of the present invention, there is provided a resin sealing type semiconductor device comprising:
35

a semiconductor chip on the surface of which a plurality of electrodes is arranged;



a bed fixed to the semiconductor chip;

a printed circuit board which is fixed on the bed in the vicinity of the semiconductor chip and on which a wiring pattern is formed to be connected to the electrodes;

a plurality of lead frames arranged so as to surround the bed; and

a wiring of a film carrier type connected to the wiring pattern on the printed circuit board and to the lead frames.

According to this structure of the present invention, no bumps need to be formed using the TAB technique in order to connect the printed circuit board and the leads. The manufacturing cost of semiconductor devices is not increased so greatly, which improves the productivity of the devices. If a printed circuit board is connected to leads using the TAB technique in a multi-chip package (MCP) semiconductor device, the reliability and productivity of the MCP semiconductor device are improved.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a cross sectional view of a conventional resin sealing type semiconductor device in which a very small semiconductor chip is sealed with resin;

Fig. 2 is a cross sectional view of the conventional semiconductor device shown in Fig. 1 in which the semiconductor chip is connected to leads of lead frames using the TAB technique;

Fig. 3 is a cross sectional view of a resin sealing type semiconductor device according to a first embodiment of the present invention in which a very small semiconductor chip is sealed with resin;

Fig. 4 is a cross sectional view of a resin sealing type semiconductor device according to a second embodiment of the present invention in which the semiconductor

chip as shown in Fig. 3 is sealed with resin;

Fig. 5 is a cross sectional view of a resin sealing type semiconductor device according to a third embodiment of the present invention in which the semiconductor chip as shown in Fig. 3 is sealed with resin;

Fig. 6 is a cross sectional view of a resin sealing type semiconductor device according to a fourth embodiment of the present invention in which the semiconductor chip as shown in Fig. 3 is sealed with resin;

Fig. 7 is a perspective view of an MCP (multi chip package) to which the structure of the semiconductor chip shown in Fig. 3 is applied, according to a fifth embodiment of the present invention; and

Fig. 8 is a cross sectional view of the MCP shown in Fig. 7 which is sealed with resin.

Embodiments of the present invention will be described with reference to accompanying drawings.

Fig. 3 is a cross-sectional view of the configuration of a resin sealing type semiconductor device according to the first embodiment of the present invention. Semiconductor chip 32 is die-bonded onto bed 31 of a lead frame by solder or conductive epoxy resin. Insulation wiring substrate 33 is fixed to an end portion on the surface of bed 31 so as to overhang from bed 31. A plurality of desired wiring patterns, not shown, is formed on printed circuit board 33, and printed circuit board 33 is used to connect lead 34 of the lead frame and semiconductor chip 32 which cannot be made close to each other any more in view of processing dimensions. Each of a plurality of I/O electrode pads 35 formed on chip 32 is connected to one 36 of connecting terminals of substrate 33 by means of bonding wire 37, and lead 34 is connected to the other connecting terminal 38 of substrate by means of TAB tape 39. Semiconductor chip 32 including printed circuit board 33 is then covered with mold resin 40, and part of lead 34 is exposed outside as an outer lead.

According to the first embodiment, in a semiconductor device produced by sealing very small semiconductor chip 32 in a package with resin, the deformation of bonding wire 37 due to pressure applied when the sealing operation is performed, neither causes any short circuit nor affects the reliability of the semiconductor device since the bonding wire is short. Even if such a bonding wire is used, the yield can be improved. Since semiconductor chip 32 and printed circuit board 33 are connected by bonding wire 37, no special device need to be used for forming bumps (projected electrodes) on I/O electrode pad 35 of chip 32. It is thus only an OLB (outer lead bonding) apparatus for connecting printed circuit board 33 and lead 34 by TAB tape 39 that is required as a new equipment. The investment in equipment in the manufacturing process can thus be reduced.

In the semiconductor device whose price is low and in which bumps are formed on electrode pad 35 and it is economically difficult to connect electrode 35 and lead 34 and by the TAB tape, if printed circuit board 33 is formed, the semiconductor device can be manufactured with high reliability and at low cost.

Furthermore, since the TAB technique is used to connect printed circuit board 33 and lead 34, the productivity of semiconductor devices can be enhanced. No bumps need to be formed and thus the manufacturing cost of the semiconductor devices is not increased.

The methods of electrically connecting chip 32 and printed circuit board 33 and electrically connecting printed circuit board 33 and lead 34 are not limited to the first embodiment. For example, as shown in Fig. 4, printed circuit board 33 and lead 34 can be connected to each other by bonding wire 41. As illustrated in Fig. 5, the electrical connection of printed circuit board 33 and lead 34 can be performed by forming contact portion 51 on the undersurface of printed circuit board 33 using a wireless bonding technique. It is therefore

necessary only to perform a bonding operation which is the most suitable for a semiconductor chip. If bed 31 is small and has no space for fixing printed circuit board 33, board 33 can be fixed not onto the surface but onto the undersurface of bed 31, as shown in Fig. 6. Various applications can thus be made to the first embodiment.

Fig. 7 illustrates an MCP (multi chip package) to which the semiconductor chip shown in Fig. 3 is applied.

As illustrated in Fig. 7, semiconductor chips 55-61 are properly arranged and die-bonded onto beds 51-54 of lead frames fixed by hanging pins 50. Printed circuit boards 62-65 are formed on beds 51-54 so as to surround the semiconductor chips. A desired wiring pattern is formed on each of printed circuit boards 62-65 and used to electrically connect lead 66 and each of chips 55-61, which cannot be made close to each other any more in view of processing dimensions, and to connect chips 55-61 to one another. A plurality of I/O electrode pads 67 formed on the surface of each of chips 55-61 is connected by bonding wires 69 to connecting terminals 68 of the wiring patterns, which are near the semiconductor chips. The connecting terminals of the wiring patterns, which are near the periphery of one of printed circuit boards 62-65, are connected to the wiring patterns of other printed circuit boards and electrically connected to leads 66. The former connection is performed by bonding wires 70, and the latter connection is performed by TAB tapes 71 using the TAB technique. TAB tape 71 is obtained by forming lead line 73 plated with copper on polyamide film 72 so as to correspond to lead 66. The connecting terminals of each of printed circuit boards 62-65 are connected to their corresponding leads 66 at once.

Fig. 8 is a cross sectional view of the MCP shown in Fig. 7 which is sealed with resin. In Fig. 8, the same elements as those in Fig. 7 are denoted by the same

reference numerals. The printed circuit boards are connected to each other by bonding wires, and the semiconductor chips are connected to printed circuit boards by bonding wires. The printed circuit boards are connected
5 to their corresponding leads 66 by TAB tapes 71. The MCP is thus sealed with mold resin 81. Like the structure shown in Fig. 3, no bumps need to be formed, so that the manufacturing cost is not so increased, and an MCP of a multi-pin structure having a great large number
10 of leads 66 is improved in reliability and productivity.

As described above, according to the present invention, a resin sealing type semiconductor device whose price is low and reliability is high can be provided, and an MCP can be improved in reliability and
15 productivity.

Reference signs in the claims are intended for better understanding and shall not limit the scope.



THIS SHEET HAS BEEN
REPLACED

REPLACEMENT SHEET

25 JUL 1996

Claims:

9

1. A resin sealing type semiconductor device in which a very small semiconductor chip is sealed with resin, characterized by comprising:

5 a semiconductor chip (32) on a surface of which a plurality of electrodes (35) is arranged;

a bed (31) fixed to said semiconductor chip (32);

10 a printed circuit board (33) which is fixed to a periphery of at least one of a surface and an undersurface of said bed so as to overhang from said bed (31) and on a surface of which a wiring pattern is formed;

a plurality of lead frames (34) surrounding said bed (31) and close to said printed circuit board (33);

15 first connecting means for connecting the electrodes (35) formed on said semiconductor chip (32) to one end (36) of the wiring pattern formed on the surface of said printed circuit board (33); and

20 second connecting means for connecting said lead frames (34) to other end (38) of the wiring pattern formed on the surface of said printed circuit board (33),

whereby said device is covered with mold resin (40) with parts of said lead frames left.

25 2. A resin sealing type semiconductor device according to claim 1, characterized in that said first connecting means is a bonding wire (37).

3. A resin sealing type semiconductor device according to claim 1, characterized in that said second connecting means is a bonding wire (41).

30 4. A resin sealing type semiconductor device according to claim 1, characterized in that said second connecting means directly connects the lead frames (34) and the other end (38) of the wiring pattern of said printed circuit board (33).

35 5. A resin sealing type semiconductor device according to claim 1, characterized in that said second

This Sheet Has Been Replaced





25 JUL 1996

connecting means is of a film carrier type in which a lead (39) is stuck on a film.

5 6. A resin sealing type semiconductor device according to claim 1, characterized in that said first and second connecting means are bonding wires (37, 41).

7. A resin sealing type semiconductor device according to claim 1, characterized in that said first connecting means is a bonding wire (37) and said second connecting means is of a film carrier type in which a lead (39) is stuck on a film.

8. A resin sealing type semiconductor device in which a very small semiconductor chip is sealed with resin, characterized by comprising:

15 a semiconductor chip (55, 56, 57, 58, 59, 60, 61) on a surface of which a plurality of electrodes (67) is arranged;

a bed (51, 52, 53, 54) fixed to said semiconductor chip (55, 56, 57, 58, 59, 60, 61);

20 a printed circuit board (62, 63, 64, 65) which is fixed onto said bed (51, 52, 53, 54) in the vicinity of said semiconductor chip (55, 56, 57, 58, 59, 60, 61) and on a surface of which a wiring pattern is formed and connected to said electrodes (67);

25 a plurality of lead frames (66) surrounding said bed (51, 52, 53, 54); and

wiring (71) of a film carrier type for connecting the wiring pattern on said printed circuit board (62, 63, 64, 65) and said lead frames (66),

30 whereby said device is covered with mold resin (81) with parts of said lead frames (66) left.

9. A resin sealing type semiconductor device according to claim 8, characterized in that said printed circuit board (62, 63, 64, 65) and the electrodes (67) of said semiconductor chip are connected to each other by a bonding wire (69).

10. A resin sealing type semiconductor device according to claim 8, characterized in that said wiring



THIS SHEET HAS BEEN
REPLACED

REPLACEMENT SHEET

25 JUL 1996

11

(71) is formed by connecting the wiring pattern on said printed circuit board (62, 63, 64, 65) and said lead frames (66) by a lead (73) stuck on a film (72).

5 11. A resin sealing type semiconductor device in which a very small semiconductor chip is sealed with resin, characterized by further comprising:

a plurality of semiconductor chips (55, 56, 57, 58, 59, 60, 61) on a surface of each of which a plurality of electrodes (67) is arranged;

10 a plurality of beds fixed to said semiconductor chips (55, 56, 57, 58, 59, 60, 61);

15 a plurality of printed circuit boards (62, 63, 64, 65) which is fixed onto said beds (51, 52, 53, 54) in the vicinity of said semiconductor chips (55, 56, 57, 58, 59, 60, 61) and on surfaces of which wiring patterns are formed and connected to said electrodes (62, 63, 64, 65);

a plurality of lead frames (66) surrounding said beds (51, 52, 53, 54); and

20 wiring (71) of a film carrier type for connecting the wiring patterns on said printed circuit boards (62, 63, 64, 65) and said lead frames,

whereby said device is covered with mold resin (81) with parts of said lead frames (66) left.

25 12. A resin sealing type semiconductor device according to claim 11, characterized in that at least one of said plurality of semiconductor chips (55, 56, 57, 58, 59, 60, 61) is formed on each of said beds (51, 52, 53, 54).

30 13. A resin sealing type semiconductor device according to claim 11, characterized in that the wiring patterns on said printed circuit boards (62, 63, 64, 65) are connected to the electrodes (67) of said semiconductor chips by bonding wires.

35 14. A resin sealing type semiconductor device according to claim 11, characterized in that said wiring (71) is formed by connecting the wiring pattern on said



* C L M S *

THIS SHEET HAS BEEN
REPLACED

REPLACEMENT SHEET

25 JUL 1996

12

printed circuit boards (62, 64, 64, 65) and said lead frames (66) by a lead (73) stuck on a film.

5 15. A resin sealing type semiconductor device according to claim 11, characterized in that said printed circuit boards (62, 63, 64, 65) are separated from said beds (51, 52, 53, 54).

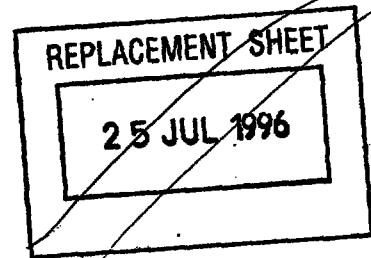
10 16. A resin sealing type semiconductor device according to claim 11, characterized in that said printed circuit boards (62, 63, 64, 65) are separated from said beds (51, 52, 53, 54) and have connecting means for electrically connecting said printed circuit boards (62, 63, 64, 65).

15 17. A resin sealing type semiconductor device according to claim 16, characterized in that said connecting means of said printed circuit boards (62, 63, 64, 65) are bonding wires (70).

This Sheet Has Been Replaced



* C L N S *



Abstract: (Fig. 3)

"RESIN SEALING TYPE SEMICONDUCTOR DEVICE IN WHICH A
VERY SMALL SEMICONDUCTOR CHIP IS SEALED IN PACKAGE
WITH RESIN"

A lead of a lead frame cannot be made close to a very small semiconductor chip in view of processing dimensions. If a TAB technique is used to directly connect the semiconductor chip and the lead in order to improve in reliability, a device for forming a bump on an electrode of the chip is required, which increases the cost of investment in equipment. A printed circuit board (33) is formed between the lead (34) and bed (31) and a bonding wire (37) is used to shorten the length of wiring and thus to decrease in cost and improve in reliability. Since an electrode pad (35) of the semiconductor chip (32), the printed circuit board (33), and the lead (34) are connected to each other using the TAB technique, the productivity of semiconductor devices is increased. Using the TAB technique, no bumps are formed anywhere and the cost of investment in equipment is not so increased.

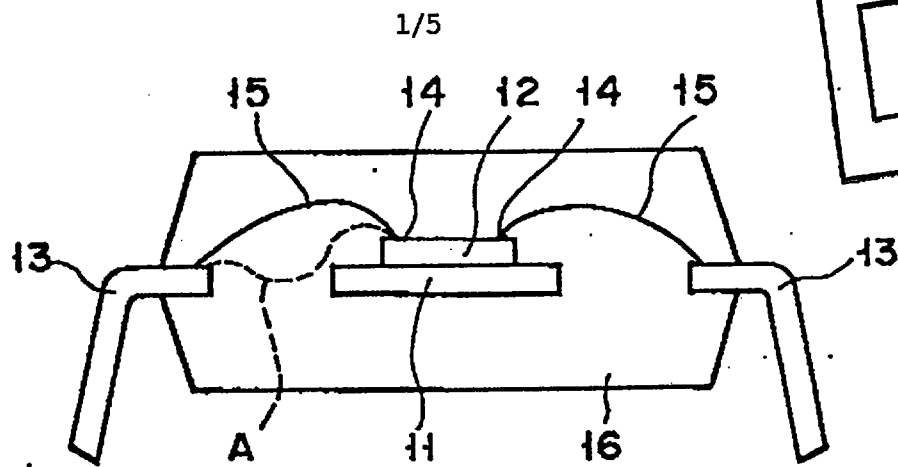
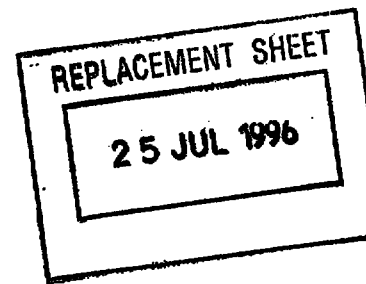


FIG. 1

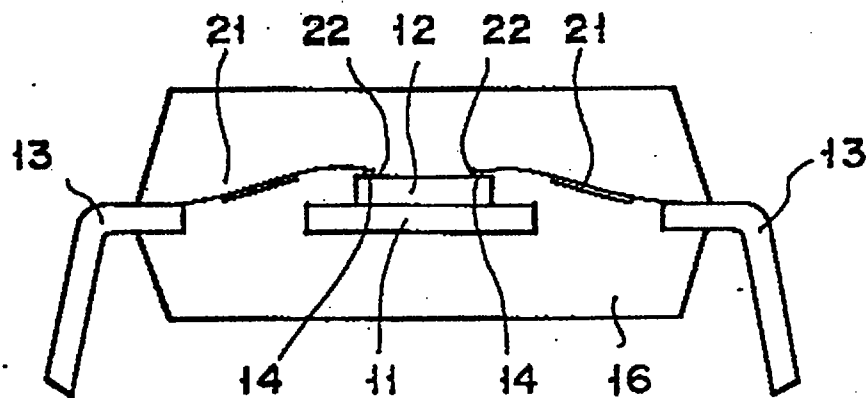


FIG. 2

25 JUL 1996

2/5

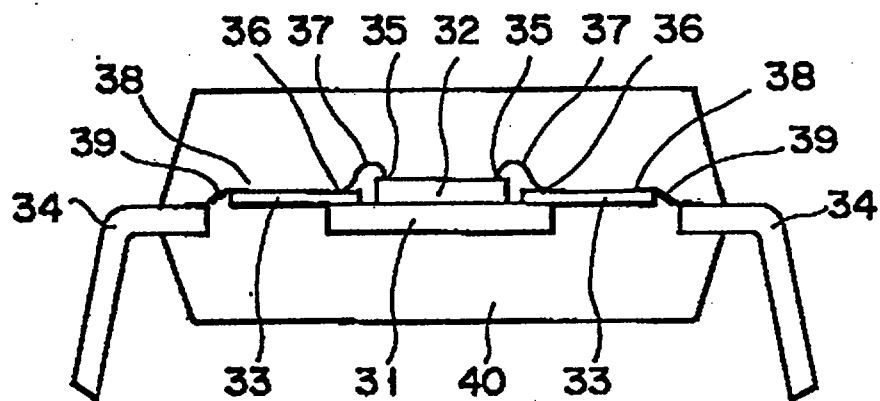


FIG. 3

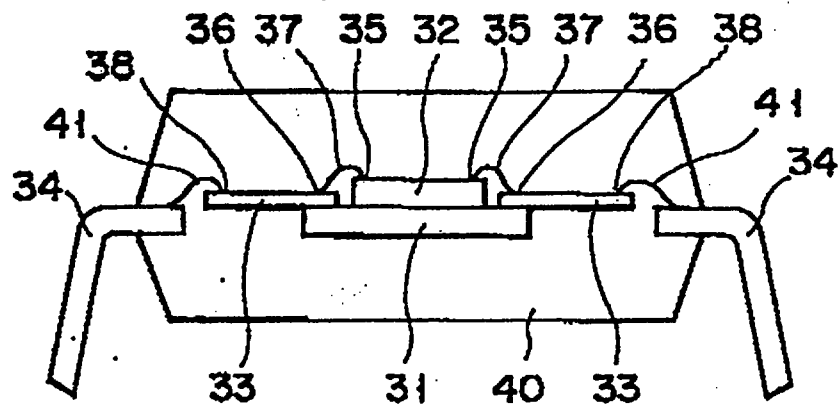


FIG. 4

25 JUL 1996

3/5

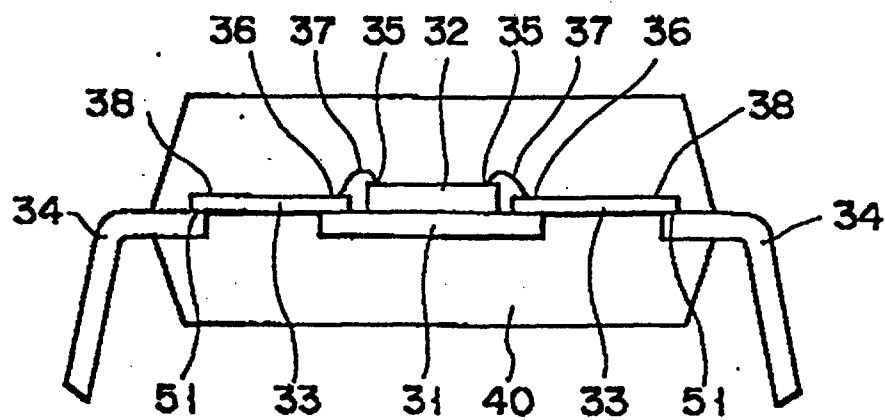


FIG. 5

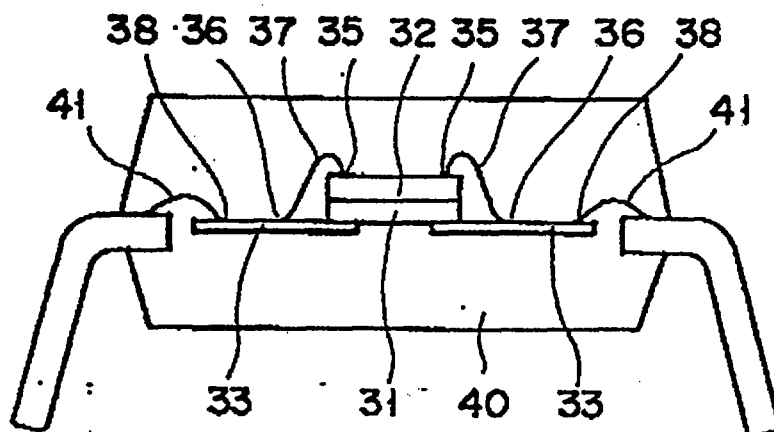


FIG. 6

REPLACEMENT SHEET

25 JUL 1996

4/5

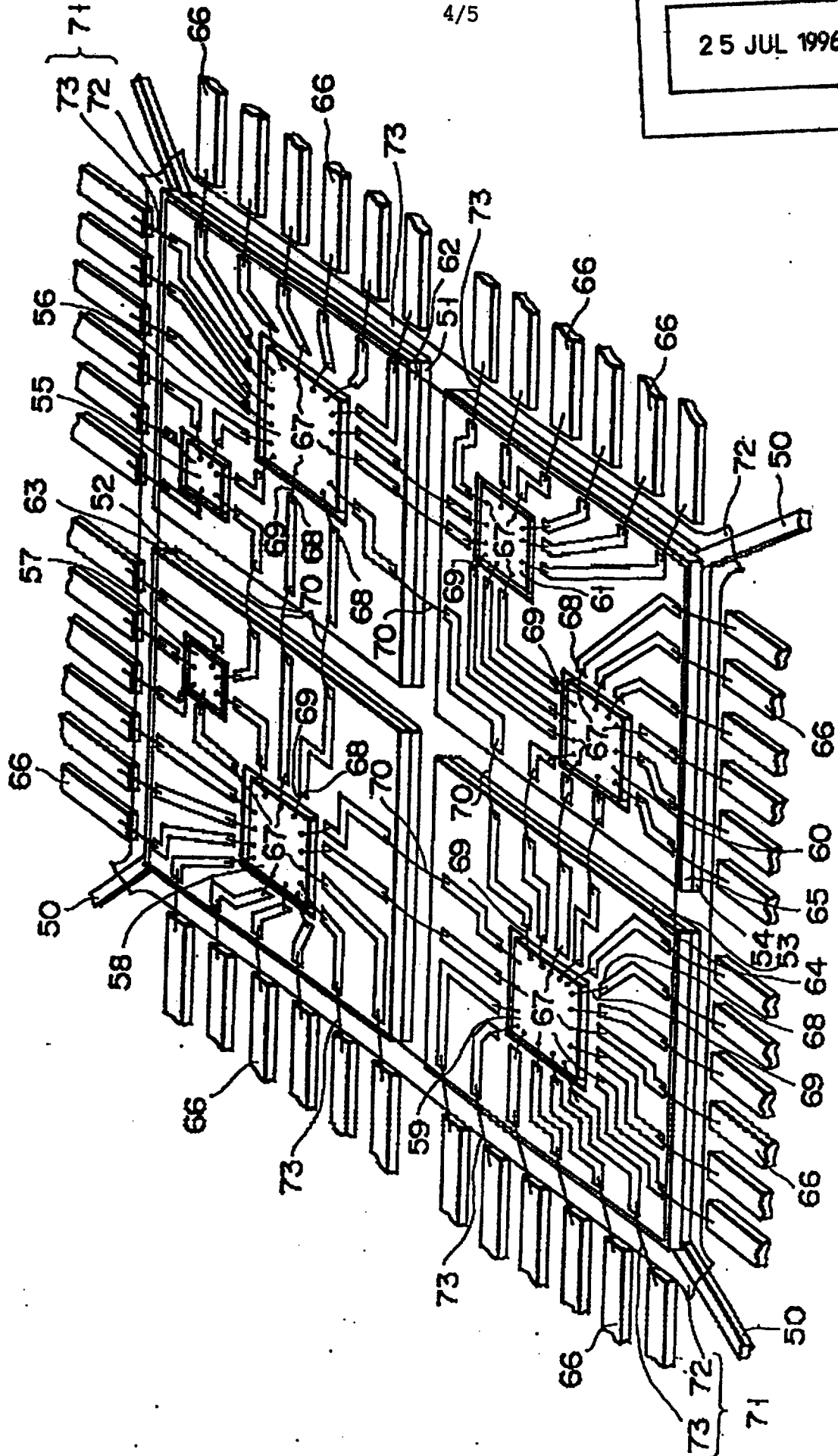


FIG. 7

REPLACEMENT SHEET

25 JUL 1996

5/5

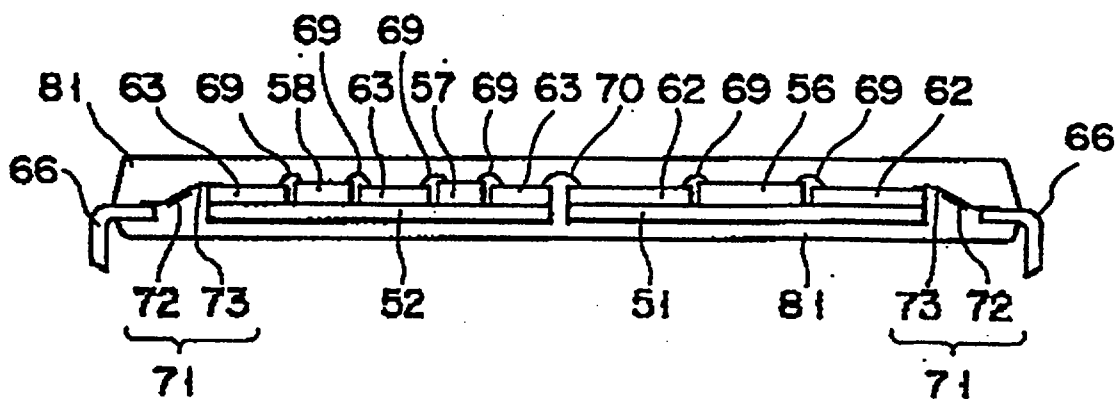
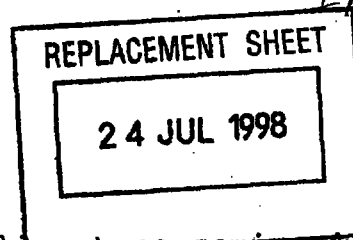


FIG. 8



9



9602863-4

IPO'S COPY

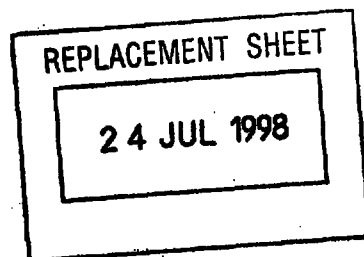
CLAIMS

1. A moulded material sealing ~~type semiconductor~~ device for sealing a very small semiconductor chip (32) having a plurality of electrodes (35) arranged on a surface of the semiconductor chip (32), comprising:

a bed (31) having upper and lower surfaces, on the upper one of which said semiconductor chip (32) is mounted;

a plurality of leads (34) surrounding and terminating close to said bed (31);

a printed circuit board (33) fixed on one of the upper and lower surfaces of said bed so as to overhang from said bed or to overlap said bed such that an outer peripheral portion of said printed circuit board is aligned with an outer peripheral portion of said bed, said printed circuit board defining an aperture therein at the same position as the chip and having thereon a wiring pattern having first and second ends (36, 38) on said printed circuit board and between said semiconductor chip (32) and said leads (34), said wiring pattern interconnecting each electrode (35) of the semiconductor chip with a respective said lead (34) via first connecting means (37) connecting the electrodes (35) on said semiconductor chip (32) to the first end (36) of the wiring pattern on the surface of said printed circuit board (33) and via second connecting means (39)



connecting said leads (34) to the second end (38) of the wiring pattern on the surface of said printed circuit board (33); and

molded resin material (40) covering said semiconductor device with parts of said leads (34) left uncovered.

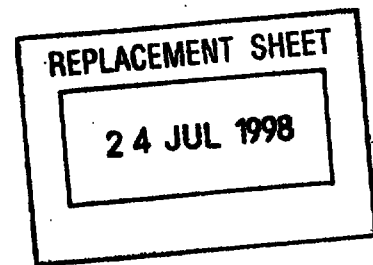
2. A moulded material sealing type semiconductor device according to claim 1, wherein said printed circuit board (33) is fixed to a peripheral surface portion of the upper surface of said bed (31) without contacting said semiconductor chip (32).

3. A moulded material sealing type semiconductor device according to claim 1 or 2, wherein the electrodes (35) of the semiconductor chip (32) are without corresponding bumps (projected electrodes) for the connections between the first connecting means (37) and the electrodes (35).

4. A moulded material sealing type semiconductor device according to any one of claims 1 to 3, wherein said first connecting means is a bonding wire (37).

5. A moulded material sealing type semiconductor device according to any one of claims 1 to 3, characterized in that said second connecting means is a bonding wire (41).

6. A moulded material sealing type semiconductor device according to any one of claims 1 to 3, wherein



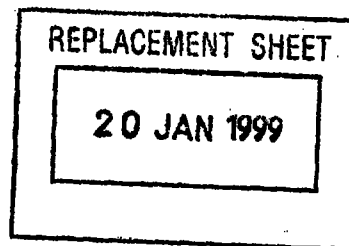
said second connecting means directly connects the leads (34) to the second end (38) of the wiring pattern of said printed circuit board (33).

7. A moulded material sealing type semiconductor device according to any one of claims 1 to 3, wherein said second connecting means is a TAB tape (39).

8. A moulded material sealing type semiconductor device according to any one of claims 1 to 3, wherein said first and second connecting means are bonding wires (37, 41).

9. A moulded material sealing type semiconductor device according to any one of claims 1 to 3, wherein said first connecting means is a bonding wire (37) and said second connecting means is a TAB tape (39).

10. A moulded material sealing type semiconductor device according to any one of claims 1 to 3, wherein said bed is one of a plurality of beds (51-54), said chip is one of a plurality of chips (56-61) and at least one of said plurality of chips is formed on each of said beds.



9602863-4

IPO'S COPY

- 2 -

it is deformed by the pressure exerted during the resin sealing as indicated by broken line A in Fig. 1 and is brought into contact with another bonding wire. There is a strong possibility that bonding wire 15 becomes defective.

As one of methods for solving the above problem, it is known to connect chip 12 and lead 13 by TAB (Tape Automated Bonding) tape 21 using a TAB technique, as shown in Fig. 2. The TAB technique is as follows. TAB tape 21 is formed by sticking electrode pad 14 and a thin-film wire made of Cu or the like corresponding to lead 13 on a resin film, and the TAB tape allows electrode pad 14 and lead 13 to be bonded at once.

TAB tape 21 is resistible to the pressure exerted when the chip is sealed in with resin and thus not deformed. Since electrode pad 14 and lead 13 can be bonded at once, the productivity of semiconductor devices is high. According to the TAB technique, however, a bump (projected electrode) 22 needs to be formed on electrode pad 14 so that the electrode pad does not contact the edge of the chip or the chip is not damaged by the bonding operation, and a special device for forming the bump is required. For this reason, an equipment investment in manufacturing process increases the manufacturing cost and it is economically difficult to apply the TAB technique to the semiconductor device of the present invention whose price is low.

It is accordingly an object of the present invention to provide a resin sealing type semiconductor device which prevents defects from being caused by deformation of a wire when a semiconductor chip is sealed in with resin and which can thus be manufactured at relatively low cost.

20 JAN 1999

- 3 -

To attain the object of the present invention, there is provided a moulded material sealing type semiconductor device for sealing a very small semiconductor chip (32) having a plurality of electrodes (35) arranged on a surface of the semiconductor chip (32), comprising:

a bed (31) having upper and lower surfaces, on the upper one of which said semiconductor chip (32) is mounted;

a plurality of leads (34) surrounding and terminating close to said bed (31);

a printed circuit board (33) fixed on one of the upper and lower surfaces of said bed so as to overhang from said bed such that an overhanging surface of said printed circuit board fills a gap between the outer periphery of said bed and an inner periphery of said leads, said printed circuit board defining an aperture therein at the same position as the chip and having thereon a wiring pattern having first and second ends (36, 38) on said printed circuit board and between said semiconductor chip (32) and said leads (34), said wiring pattern interconnecting each electrode (35) of the semiconductor chip with a respective said lead (34) via first connecting means (37) connecting the electrodes (35) on said semiconductor chip (32) to the first end (36) of the wiring pattern on the surface of said printed circuit board (33) and via second connecting means (39) connecting said leads (34) to the second end (38) of the wiring pattern on the surface of said printed circuit board (33); and

molded resin material (40) covering said semiconductor device with parts of said leads (34) left uncovered.

20 JAN 1999

5

10

15

20

With the above structure of the semiconductor device, an interval between the bed and each of the leads can be supplemented with the printed circuit board which is fixed so as to overhang from the bed and on which the wiring pattern is formed. The distance between the electrode pads and the printed circuit board is thus shortened. Since the semiconductor chip and the leads are connected via the substrate, the reliability of the semiconductor device becomes high without adopting the TAB technique wherein bumps need to be formed on the chip when the chip and leads are directly connected to each other.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

25

Fig. 1 is a cross sectional view of a conventional resin sealing type semiconductor device in which a very small semiconductor chip is sealed with resin;

30

Fig. 2 is a cross sectional view of the conventional semiconductor device shown in Fig. 1 in which the semiconductor chip is connected to leads of lead frames using the TAB technique;

35

Fig. 3 is a cross sectional view of a resin sealing type semiconductor device according to a first embodiment of the present invention in which a very small semiconductor chip is sealed with resin;

Fig. 4 is a cross sectional view of a resin sealing type semiconductor device according to a second embodiment of the present invention in which the semiconductor

20 JAN 1999

CLAIMS

1. A moulded material sealing type semiconductor device for sealing a very small semiconductor chip (32) having a plurality of electrodes (35) arranged on a surface of the semiconductor chip (32), comprising:

a bed (31) having upper and lower surfaces, on the upper one of which said semiconductor chip (32) is mounted;

a plurality of leads (34) surrounding and terminating close to said bed (31);

a printed circuit board (33) fixed on one of the upper and lower surfaces of said bed so as to overhang from said bed such that an overhanging surface of said printed circuit board fills a gap between the outer periphery of said bed and an inner periphery of said leads,

said printed circuit board defining an aperture therein at the same position as the chip and having thereon a wiring pattern having first and second ends (36, 38) on said printed circuit board and between said semiconductor chip (32) and said leads (34), said wiring pattern interconnecting each electrode (35) of the semiconductor chip with a respective said lead (34) via first connecting means (37) connecting the electrodes (35) on said semiconductor chip (32) to the first end (36) of the wiring pattern on the surface of said printed circuit board (33) and via second connecting means (39)