

ISOTHERMAL TRANSISTOR STRUCTURES

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductors for integrated circuits. More specifically, the present invention relates to isothermal transistor structures for transistors employed in integrated circuits.

BACKGROUND OF THE INVENTION

[0002] Integrated circuit FET transistors which are required to control high levels of current, such as those in power regulation circuits, etc., can suffer from failures and/or undesired operational parameters due to thermal issues. Commonly, for many such high current circuit needs, transistors are ganged together to provide the necessary current carrying capacity and, for a variety of reasons including process variations in their manufacture and/or layout constraints, different ones of these transistors can experience difference thermal loads in operation. There are also a variety of other circuit designs and configurations wherein two or more transistors are in thermal proximity and their thermal loads can affect the operation of the each other.

[0003] Generally, as an FET is heated, its operating parameters change. For example, its threshold voltage commonly will decrease and its subthreshold voltage current will increase as its operating temperature increases. When FET transistors are ganged together, or otherwise in close thermal proximity, and some of those transistors experience higher temperatures than others, the increases in the subthreshold current leakage of those hotter transistors result in further increased heating of those same transistors, leading to increased subthreshold leakage current increases, leading to further heating of those transistors, etc. in a sort of positive feedback loop often referred to as thermal runaway. If not properly addressed, such anisothermal behavior of the transistors in thermal proximity can result in premature aging and/or outright failure of the transistors and circuits employing them. Accordingly, circuit designers must devote significant effort and resources in attempts to achieve isothermal performance of FET transistors in high current, and other, circuits.

[0004] Recently, a new transistor design has been developed which can be fabricated in Middle of Line, or Back End of Line manufacturing stages. These transistors can be fabricated over conventional MOS transistors formed in Front End of Line manufacturing stages and/or over

other layers of the new transistors allowing for stacked circuits, but these new transistors are also subject to possible thermal effects as described above.

[0005] It is desired to have substantially isothermal transistor structures for these new transistors which are reliable and easy to fabricate.

SUMMARY OF THE INVENTION

[0006] It is an object of the present invention to provide novel isothermal transistor structures and a method of manufacturing such structures, which obviates or mitigates at least one disadvantage of the prior art.

[0007] According to a first aspect of the present invention, there is provided an isothermal structure of at least two transistors located in thermal proximity to one another, the structure including: at least two transistors formed in a back end of line and/or a middle of line manufacturing process and formed in thermal proximity to one another such that heat generated in at least one of the at least two transistors raises the temperature of the other of the at least two transistors; a layer of thermally conductive material formed thermally adjacent the at least two transistors, wherein the layer of thermally conductive material receives and dissipates heat from the transistors when the transistors are operating.

[0008] According to another aspect of the present invention, there is provided a method of manufacturing an isothermal transistor structure of at least two transistors which are in thermal proximity to one another, comprising the steps of: forming the at least two transistors with a middle of line and/or back end of line manufacturing process; and forming a layer of thermally conductive material thermally adjacent to the at least two transistors.

[0009] According to yet another aspect of the present invention, there is provided an integrated circuit formed on a silicon die having first and second opposed surfaces, comprising: logic circuitry formed on a first of said two opposed surfaces; power circuitry formed on a second of said two opposed surfaces, the power circuitry including: at least two transistors in thermal proximity formed in a back end of line and/or a middle of line manufacturing process; and a layer of thermally conductive material formed thermally adjacent the at least two transistors, wherein the thermally conductive material receives and dissipates heat from the transistors; and at least one via connecting the power circuitry to the logic circuitry.

[0010] According to yet another aspect of the present invention, there is provided an integrated circuit formed on a silicon die, comprising: logic circuitry formed on a surface of the silicon die; a layer of electrically insulating material formed over the logic circuitry; at least two transistors, in thermal proximity, formed in a back end of line and/or middle of line manufacturing process on the layer of electrically insulating material; and a layer of thermally conductive material formed thermally adjacent the at least two transistors such that the layer of thermally conductive material receives and dissipates heat from the at least two transistors when the at least two transistors are operating.

[0011] The present invention provides a novel isothermal transistor structure to enable isothermal operation of two or more transistors which are ganged together or which are otherwise in thermal proximity. The isothermal structure is fabricated in middle of line or back end of line processes and can be formed over conventional circuitry or over other layers of circuitry fabricated in middle of line or back end of line processes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Preferred embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

Figure 1 shows a schematic representation of a prior art physical structure of ganged transistors;

Figure 2 shows an example plot of the temperatures of the transistors of Figure 1 when operating at high current levels;

Figure 3 shows a schematic representation of an isothermal transistor structure in accordance with an aspect of the present invention;

Figure 4 shows an example plot, similar to that of Figure 2, for the transistors of Figure 3 when operating at high current levels;

Figure 5 shows a schematic representation of another isothermal transistor structure in accordance with an aspect of the present invention;

Figure 6 shows a cross section through a die of an integrated circuit employing isothermal transistor structures in accordance with an aspect of the present invention;

Figure 7 shows a cross section of through a die of another integrated circuit employing isothermal transistor structures in accordance with an aspect of the present invention;

Figure 8 shows a flowchart of a method of manufacturing isothermal transistor structures in accordance with an aspect of the present invention; and

Figure 9 shows a flowchart of another method of manufacturing isothermal transistor structures in accordance with an aspect of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] A prior art structure of four transistors (T1 through T4) which are ganged, or which are otherwise in thermal proximity, is indicated generally at 20 in Figure 1. As will be apparent to those of skill in the art, the present discussion is not limited to instances of four transistors and it is contemplated that the present invention is useful with instances of fewer, or many more, transistors which are arranged in a ganged configuration or which are otherwise in thermal proximity. As used herein, the term “thermal proximity” is intended to define a configuration wherein the distance between transistors is such that thermal energy created in one transistor can result in heating of another transistor.

[0014] Transistors T1 through T4 can be conventional FETs which have been manufactured on a substrate 24 of an integrated circuit which, in most circumstances, is a layer of silicon dioxide (SiO₂) formed as an insulating layer over a silicon die on which the integrated circuit including transistors T1 through T4 is fabricated. While silicon dioxide is widely employed as it is a good electrical insulator and is easily formed, it is a poor conductor of thermal energy.

[0015] Figure 2 shows an example plot of the operating temperatures of transistors T1 through T4. As shown, the temperatures of transistors T2 and T3, which are each located between and adjacent a pair of other transistors, are significantly higher than Transistors T1 and T4 and, in fact, in the illustrated example, the temperatures of T2 and T3 are above the point of thermal runaway, indicated by line 28.

[0016] Recently, as disclosed in published PCT patent application WO 2023/285936 to Barlage et al, (the contents of which are incorporated herein by reference) novel thin film metal oxide transistors, referred to herein as “BTFTs”, have been developed. These BTFTs have properties such that they can be formed in a relatively substrate-agnostic manner and in Middle of Line (“MOL”) or Back End of Line (“BEOL”) manufacturing stages. Thus, the BTFTs are able to be grown on either SiO₂ or on thermally conductive and/or other electrically insulating layers which pose engineering challenges for conventional transistors manufactured in Front End of

Line ("FEOL") processes. Further, BTFTs can be manufactured after, and on top of, conventional MOS logic and other circuitry which has been fabricated conventionally in FEOL processes and/or on other substrates or on top of layers other BTFTs.

[0017] It is contemplated that one common use for these BTFTs will be in high current and/or power circuit applications, such as voltage regulators and/or I/O drivers, etc. wherein it may be desired to gang two or more BTFTs together to provide a necessary current carrying capacity or wherein transistors may otherwise be in thermal proximity

[0018] With conventional semiconductor devices (such as MOS devices) and circuits, the interconnects between components typically comprise layers of insulators and metal conductors which are typically fabricated in MOL or BEOL processes to connect the components of the desired circuits while ensuring electrical isolation between components. These resulting MOL and/or BEOL interconnect structures are not conducive to thermal dissipation, but in many cases this is not a concern as heat generated in these structures during circuit operation is relatively small, due to the generally low ohmic losses in the structures.

[0019] However, in circumstances wherein significant functions are implemented in, on or above these BEOL interconnect structures, such as when functional circuits are fabricated using the above-mentioned BTFTs, the ability to dissipate heat from the BTFTs is required. In particular, voltage regulators and/or I/O drivers can advantageously be implemented with BTFTs and, in such cases, thermal management can become a significant issue.

[0020] To enable the desired operation of the BTFTs in such cases, the present inventors have determined that isothermal operation of the BTFTs can be achieved in a novel, and particularly effective manner, using isothermal transistor structures as described below with reference to Figures 3 and 5.

[0021] Specifically an isothermal transistor structure 100 of four BTFTs, BT1 through BT4, is shown in Figure 3. In this example, transistors BT1 through BT4 are manufactured after FEOL processing has been performed on the integrated circuit on which BT1 through BT4 are to be formed and structure 100 can be formed on top of circuitry formed in those FEOL stages of manufacture, or atop other layers of BTFT devices, or on any other suitable substrate, such as the backside of a semiconductor die.

[0022] As is well known, in conventional integrated circuit manufacturing after the FEOL manufacturing processes are complete, an insulating layer, such as silicon dioxide, is formed

over the circuit die to protect the die and to insulate the FEOL circuits from metallization layers and other features added in MOL and/or BEOL manufacturing processes.

[0023] In Figure 3, such an insulating layer is indicated at 104a and it can be formed of any suitable material, such as silicon dioxide, and in any suitable manner as will be apparent to those of skill in the art.

[0024] In the circumstances wherein structure 100 is formed over another layer of BTFTs, electrical insulating layer 104a can be any suitable electrical insulating material used to cover the previous layer of BTFTs (such as silicon dioxide or the like) and, in circumstances wherein arrangement 100 is formed directly on a substrate, such as the backside of a semiconductor device die, electrical insulating layer 104a can be the substrate itself (in cases where the substrate is an electrical insulator) or a layer electrical insulating material formed on the substrate, such as silicon dioxide, etc.

[0025] A layer 108 of material having good thermal conductivity is then formed over insulating layer 104a. Thermally conductive layer 108 can be a layer of a material which preferably can be formed at a temperature which is compatible with MOL and/or BEOL temperature limitations, e.g. – below 400°C, such as aluminum nitride (AlN), boron nitride (BN), silicon carbide (SiC), diamond or other known materials. These materials can be formed over insulating layer 104a in any suitable known manner, including atomic layer deposition (ALD) or chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), etc.

[0026] While the thickness of insulating layer 104a is not particularly limited, it is desired that thermally conducting layer 108 be at least about 10 nm to about 300 nm in thickness to provide good thermal conduction and dissipation of the heat from transistors BT1 through BT4. More preferably, thermally conducting layer 108 can be about 15 nm to about 200 nm in thickness, and more preferably, from about 20nm to about 100nm in thickness.

[0027] Ideally, thermally conducting layer 108 is thermally connected to at least one side (e.g. – top or bottom) of the die on which the integrated circuit including the BTFTs is formed to aid in the dissipation of heat from thermally conductive layer 108.

[0028] As mentioned above, it is contemplated that thermally conducting layer 108 can be formed by ALD processes or by any other suitable processes such as CVD or PECVD processes, with the latter two requiring less time to form thicker instances of thermally conducting layer 108 than when formed by ALD processes. Preferably, the thickness of thermally

conducting layer 108 is selected to be proportional to the total area of the transistors which are in thermal proximity to one another.

[0029] While diamond, boron nitride and/or aluminum nitride are each thermal conductors and electrical insulators, many other thermally conductive materials which may be considered for use as layer 108 may not be good electrical insulators. When such thermally conductive but poor electrically insulating materials are selected for use as layer 108, an optional second layer 104b of an electrical insulating material, such as silicon dioxide, is preferably formed over thermal conducting layer 108 before fabrication of transistors BT1 Through BT4 is performed.

[0030] It is contemplated that, in many circumstances, another layer 104c of insulating material or sealant will typically be formed over transistors BT1 through BT4 to protect the resultant circuits. Layers 104a, 104b (if present) and 104c can be formed of the same material, or can be formed from two or more different materials, if desired.

[0031] As indicated in Figure 3, if present, optional insulating layer 104b is much thinner than thermally conducting layer 108 to allow heat from transistors BT1 through BT4 to effectively pass through it to thermally conducting layer 108. For example, if insulating layer 104b is formed of silicon dioxide, it can have a thickness of from about 5 nm to about 100 nm, and more preferably from about 10 nm to about 50nm, which is sufficient to provide electrical insulation for transistors BT1 through BT4, without unduly inhibiting the transfer of heat from those transistors to thermally conducting layer 108. The selection of other insulating materials for insulating layer 104b would have different desired thicknesses depending upon their thermal conductivities, as will be apparent to those of skill in the art.

[0032] Figure 4 shows an example plot of the operating temperatures of transistors BT1 through BT4. As shown, the temperatures of the transistors are each quite similar, as thermally conducting layer 108 acts to prevent the formation of "hot spots" by distributing and dissipating the heat from the transistors and the transistors are approximately equally distant from thermal runaway temperature 28.

[0033] While the example of the present invention discussed above with respect to Figures 3 and 4 shows thermally conductive layer 108 formed under the BTFTs, it is also contemplated that thermally insulating layer 108 can be formed over the BTFTs, essentially turning structure 100 upside down, as shown in Figure 5. In fact, it is contemplated that in some cases, this will be a preferred implementation of the present invention as it enables a simplified connection of

thermally conductive layer 108 to an outer surface (e.g. – top or bottom) of the semiconductor device die on which the circuit is formed.

[0034] In Figure 5, wherein similar features to those of Figure 3 are indicated with like reference numerals, an isothermal transistor structure 200 is illustrated comprising four BTFTs (BT1 through BT4). BT1 through BT4 have been formed on an insulating substrate layer 104a, such as a layer of silicon dioxide, glass, a polymer material, etc. as was discussed with reference to the structure of Figure 3.

[0035] A thermally conductive layer 108 is then formed over the transistors BT1 through BT4. In this example, thermally conductive layer 108 is formed of aluminum nitride (AlN), diamond or boron nitride, which are also electrical insulators and as such the need for optional layer 104b of electrically insulating material is avoided. In other cases, wherein thermally conductive layer 108 is formed of a material which is not an electrical insulator, optional layer 104b of electrically insulating material will be formed over transistors BT1 through BT4 and thermally conductive layer 108 will be formed atop layer 104b. If required, layer 104b can have a thickness of from about 5 nm to about 100 nm and more preferably from about 10 nm to about 50 nm and, in either case, as before thermally conductive layer 108 can have a thickness of about 10 nm to about 300 nm, and more preferably between about 15 nm to about 200 nm and more preferably from about 20 nm to about 100nm.

[0036] An electrically insulating layer 104c can then be formed over thermally conductive layer 108 to allow other MOL or BEOL layers, such as metallization layers, or layers of additional BTFT transistors, etc. to be formed over structure 200. In the illustrated example, electrically insulating layer 104c is formed of the same material as insulating layers 104a and 104b (if present), but it is also contemplated that insulating layer 104c can be formed from any other suitable insulating material, as will be apparent to those of skill in the art or, insulating layer 104c can be omitted altogether and thermally conductive layer 108 can act as the outer surface of the die on which the integrated circuit of structure 200 is formed.

[0037] Thus in the isothermal transistor structures of Figure 3 and/or Figure 5, the BTFTs are thermally adjacent to a layer of thermally conductive material. As used herein, the term “thermally adjacent” is intended to describe configurations wherein the BTFTs are either in direct contact with the layer of thermally conductive material, or are separated from the layer of thermally conductive material by a relatively thin layer of electrically insulating material which

does not significantly impede or prevent the transfer of heat between BTFTs and the layer of thermally conductive material.

[0038] Figure 6 shows a cross section (not to scale) of an integrated circuit 300 which has conventional transistor circuits 304, including metal interconnects, etc., which have been formed on one side of a silicon die 308. The other side of die 308, includes power circuits 312 formed with BTFTs to implement voltage regulators, I/O drivers and other circuits for integrated circuit 300. As circuits 312 operate with relatively high power levels, and thus are subject to relatively high thermal loads, the present inventors have determined that constructing such circuits with BTFTs employing the present invention is advantageous. As BTFTs can be manufactured in MOL or BEOL manufacturing stages, conventional transistor circuits 304 can be manufactured first in FEOL manufacturing stages, and circuits 312 manufactured after.

[0039] As will now be apparent to those of skill in the art, in semiconductor device 300, logic conventional transistor circuits 304 receive power from voltage regulators implemented in circuits 312, and control signals and data signals (I/O) are exchanged between circuits 304 and circuits 312. The connections to allow the exchange of signals and power between the top and bottom sides of die 308 can be achieved in a variety of manners, as will be apparent to those of skill in the art, such as with Trans Silicon Vias (TSVs) 316 as shown in the Figure.

[0040] Figure 7 shows a cross section of an integrated circuit 350, similar to integrated circuit 300, but wherein power circuits 312 have been manufactured on the same side of die 308 as conventional transistor circuits 304, and specifically on top of circuits 304.

[0041] Figure 8 shows a flowchart of a method 400 of manufacturing transistor structures in accordance with an aspect of the present invention, wherein the thermally conductive layer is formed under the BTFTs.

[0042] The method commences at step 404 wherein a thermally conductive material is selected and layer of the selected material is formed over a substrate. As discussed above, the substrate can be any suitable substrate material, such as silicon dioxide, glass, polymers, etc.

[0043] Next, at step 408, a determination is made as to whether the selected thermally conductive material is an electrically insulating material. If the selected thermally conductive material is not an electrical insulator, the method continues at step 412 wherein a layer of an electrically insulating material is formed over the layer of thermally conductive material formed at step 404. The thickness of the layer of electrically insulating material formed at step 412 is

preferably within the ranges of thicknesses discussed above, such that when the BTFTs are formed, they are thermally adjacent to the layer of thermally conductive material. The method then proceeds to step 416.

[0044] If at step 408, if it is determined that the thermally conductive material of step 404 is an electrical insulator, the method proceeds at step 416.

[0045] At step 416 at least two BTFT transistors are formed, in thermal proximity to one another, on the surface of the layer of thermally conductive material of step 404, or on the surface of the layer of electrically layer of thermally conductive material, if present, of step 412.

[0046] The method completes at step 420 wherein a layer of electrically insulating material is formed over the at least two transistors.

[0047] Figure 9 shows a flowchart of a method 500 of manufacturing transistor structures in accordance with an aspect of the present invention, wherein the thermally conductive layer is formed over the transistors.

[0048] The method commences at step 504 wherein at least two BTFT transistors are formed, in thermal proximity to one another, on a suitable substrate.

[0049] At step 508, a thermally conductive material is selected.

[0050] At step 512, if it is determined that the selected thermally conductive material is not an electrical insulator, the method proceeds to step 516 wherein a layer of electrically insulating material is formed over the transistors and the method proceeds to step 520.

[0051] If at step 512 it is determined that the thermally conductive material is an electrical insulator, the method proceeds to step 520.

[0052] At step 520, a layer of the selected thermally conductive material is formed over the transistors and, if present, over the layer of electrically insulating material formed at step 516.

[0053] It is contemplated that, in some cases, the layer of thermally conductive material formed at step 520 can act as a sealing layer to complete the method, and it is contemplated that in other cases the method will instead complete at step 524 wherein a layer of electrically insulating material will be formed over the layer of thermally conductive material formed in step 520.

[0054] As will now be apparent, when manufactured with either of the above-described methods, a structure is obtained whereby two or more BTFTs which are in thermal proximity to

one another are also thermally adjacent to a layer of a thermally conductive material which results in the two or more BTFTs being an isothermal transistor structure.

[0055] As mentioned above, the isothermal transistor structures of the present invention can be formed on a side of the semiconductor die opposite the side on which conventional circuitry is formed or can be formed on the same side of a semiconductor die as the conventionally formed circuitry with the isothermal transistor structures being formed over the conventional circuitry. In either case, the isothermal transistor structures of the present invention are formed in MOL or BEOL manufacturing stages and can be formed over top of the conventionally FEOL manufactured circuitry or other layers of MOL or BEOL-formed BTFTs.

[0056] The above-described embodiments of the invention are intended to be examples of the present invention and alterations and modifications may be effected thereto, by those of skill in the art, without departing from the scope of the invention which is defined solely by the claims appended hereto.

We claim:

1. An isothermal structure of at least two transistors located in thermal proximity to one another, the structure including:
 - at least two transistors formed in a back end of line and/or a middle of line manufacturing process and formed in thermal proximity to one another such that heat generated in at least one of the at least two transistors raises the temperature of the other of the at least two transistors;
 - a layer of thermally conductive material formed thermally adjacent the at least two transistors, wherein the layer of thermally conductive material receives and dissipates heat from the transistors when the transistors are operating.
2. The isothermal structure of claim 1 wherein the layer of thermally conductive material has a thickness of from about 10 nm to about 300 nm.
3. The isothermal structure of claim 2 wherein the thermally conductive layer is electrically conductive and the structure further includes including a layer of electrically insulating material between the transistors and the layer of thermally conductive material.
4. The isothermal structure of claim 3 wherein the layer of insulating material has a thickness of from about 5 nm to about 100 nm
5. The isothermal structure of claim 4 further including a second layer of electrically insulating material formed over the isothermal structure to substantially seal the structure.
6. The isothermal structure of claim 1 wherein the thermally conductive material is an electrical insulator.
7. The isothermal structure of claim 4 wherein the layer of electrically insulating material and the second layer of electrically insulating material are formed of the same material.

8. The isothermal structure of claim 1 wherein the layer of thermally conductive material has a thickness of from about 15 nm to about 200 nm.
9. The isothermal structure of claim 1 wherein the layer of thermally conductive material has a thickness of from about 20 nm to about 100 nm.
10. The isothermal structure of claim 3 wherein the layer of electrically insulating material has a thickness of from about 5 nm to about 100 nm.
11. The isothermal structure of claim 3 wherein the layer of electrically insulating material has a thickness of from about 10 nm to about 50 nm.
12. The isothermal structure of claim 1 wherein the structure is formed in an integrated circuit on a die and wherein the thermally conductive layer is in thermal contact with at least one surface of the die to dissipate heat there through.
13. The isothermal structure of claim 1 wherein the at least two transistors are ganged together.
14. A method of manufacturing an isothermal transistor structure of at least two transistors which are in thermal proximity to one another, comprising the steps of:
 - forming the at least two transistors with a middle of line and/or back end of line manufacturing process; and
 - forming a layer of thermally conductive material thermally adjacent to the at least two transistors.
15. The method of claim 14 wherein the layer of thermally conductive material has a thickness of from about 10 nm to about 300 nm.
16. The method of claim 14 wherein the thermally conductive layer is electrically conductive further including the step of forming a layer of electrically insulating material

between the at least two transistors and the layer of thermally conductive material.

17. The method of claim 16 wherein the layer of electrically insulating material has a thickness of from about 5 nm to 100nm.

18. The method of claim 14 wherein the layer of thermally conductive material is formed by chemical vapor deposition.

19. An integrated circuit formed on a silicon die having first and second opposed surfaces, comprising:

- logic circuitry formed on a first of said two opposed surfaces;
- power circuitry formed on a second of said two opposed surfaces, the power circuitry including:
 - at least two transistors in thermal proximity formed in a back end of line and/or a middle of line manufacturing process; and
 - a layer of thermally conductive material formed thermally adjacent the at least two transistors, wherein the thermally conductive material receives and dissipates heat from the transistors; and
- at least one via connecting the power circuitry to the logic circuitry.

20. The integrated circuit of claim 19 wherein the power circuitry implements at least one voltage regulator and the at least one via provides power from the at least one voltage regulator to the logic circuitry.

21. An integrated circuit formed on a silicon die, comprising:

- logic circuitry formed on a surface of the silicon die;
- a layer of electrically insulating material formed over the logic circuitry;
- at least two transistors, in thermal proximity, formed in a back end of line and/or middle of line manufacturing process on the layer of electrically insulating material; and
- a layer of thermally conductive material formed thermally adjacent the at least two transistors such that the layer of thermally conductive material receives and dissipates

heat from the at least two transistors when the at least two transistors are operating.

22. The integrated circuit of claim 21 wherein the thermally conductive material is electrically conductive and further including a layer of electrically insulating material formed between the at least two transistors and the layer of thermally conductive material.