FIG. 1A

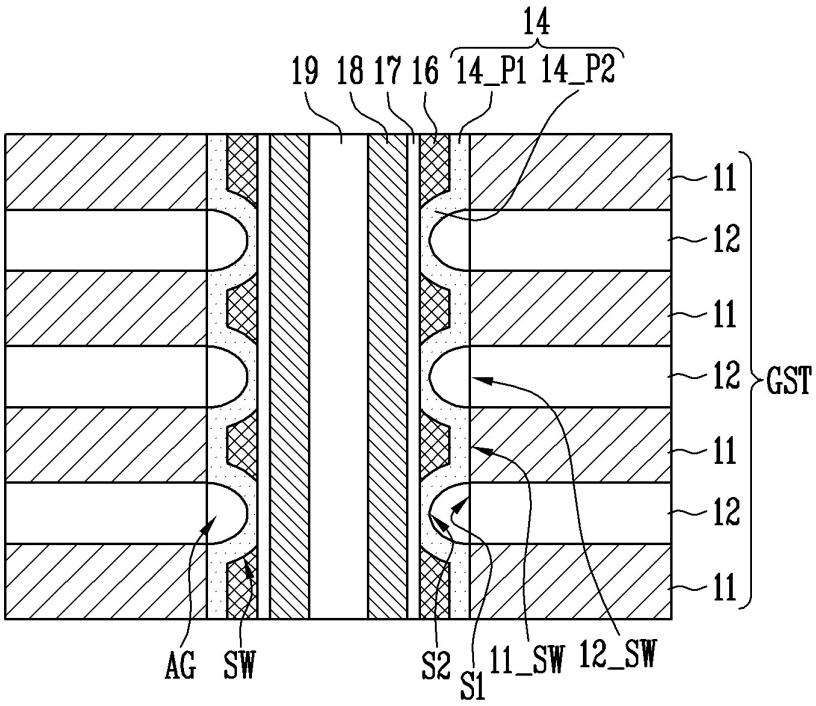

14
19
18
17
16
14_P1
14_P2
11
12
11
12
GST
11
12
11
AG
SW
S2
S1
11_SW
12_SW

FIG. 1B

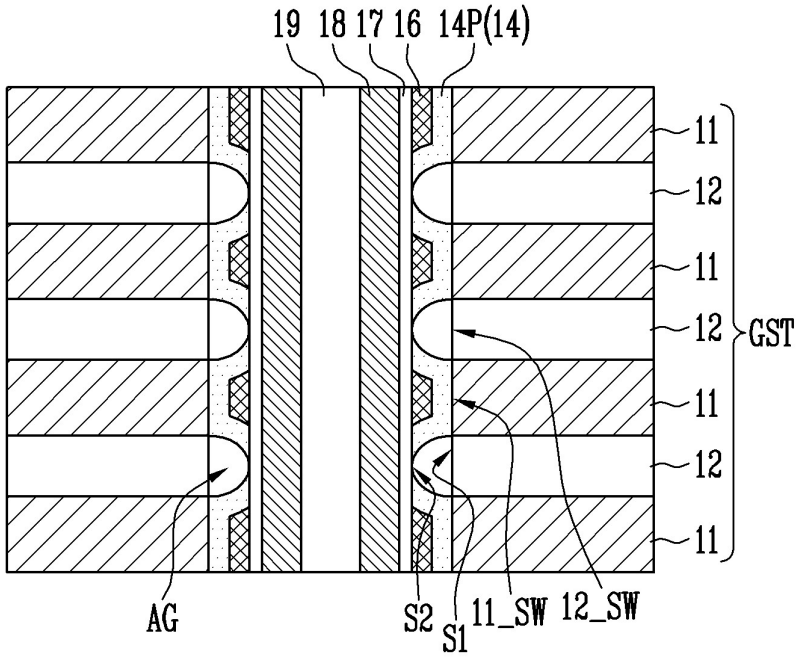

19
18
17
16
14P(14)
11
12
11
12
GST
11
12
11
AG
S2
S1
11_SW
12_SW

FIG. 1C

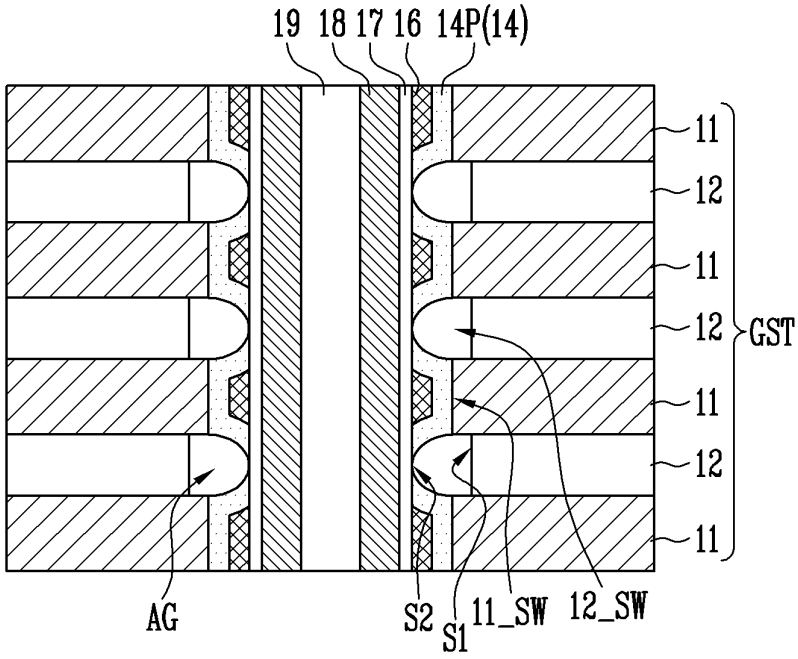


FIG. 2A

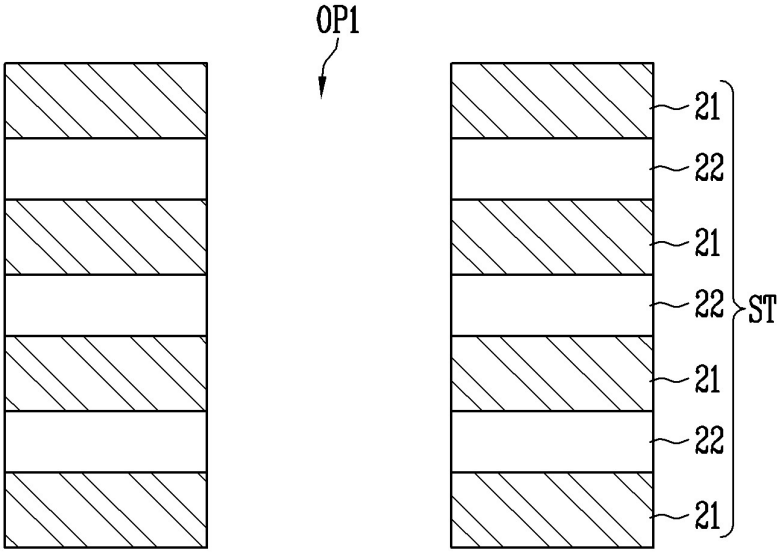


FIG. 2B

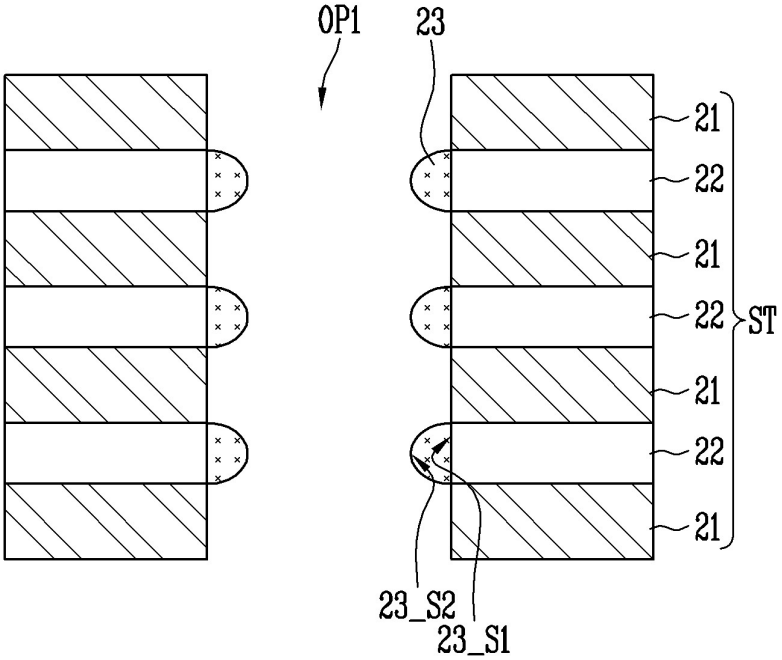


FIG. 2C

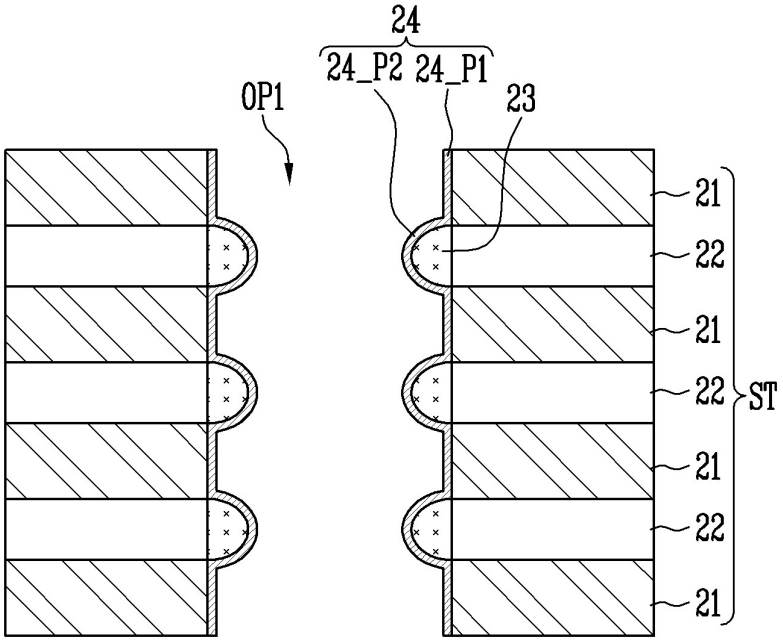

24
24_P2 24_P1
OP1
23
21
22
21
22
21
22
21
ST

FIG. 2D

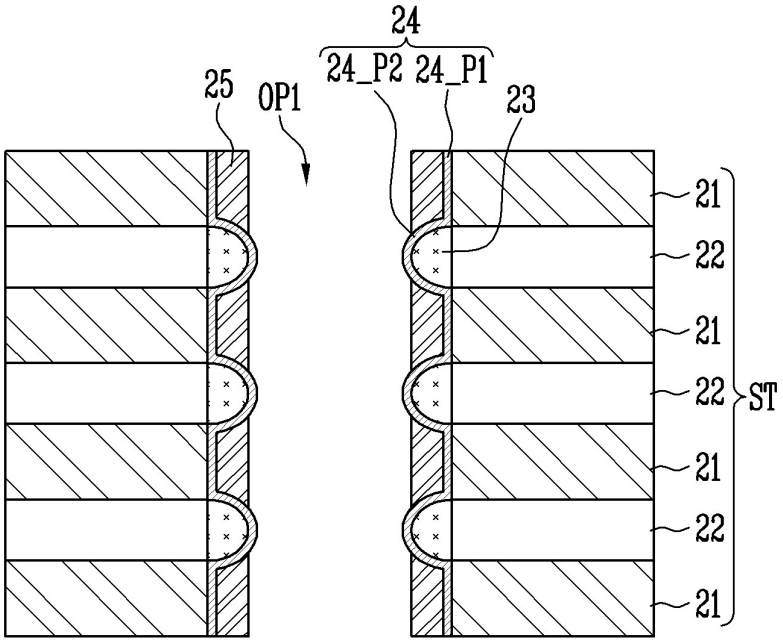

24
24_P2 24_P1
25
OP1
23
21
22
21
22
21
22
21
ST

FIG. 2E

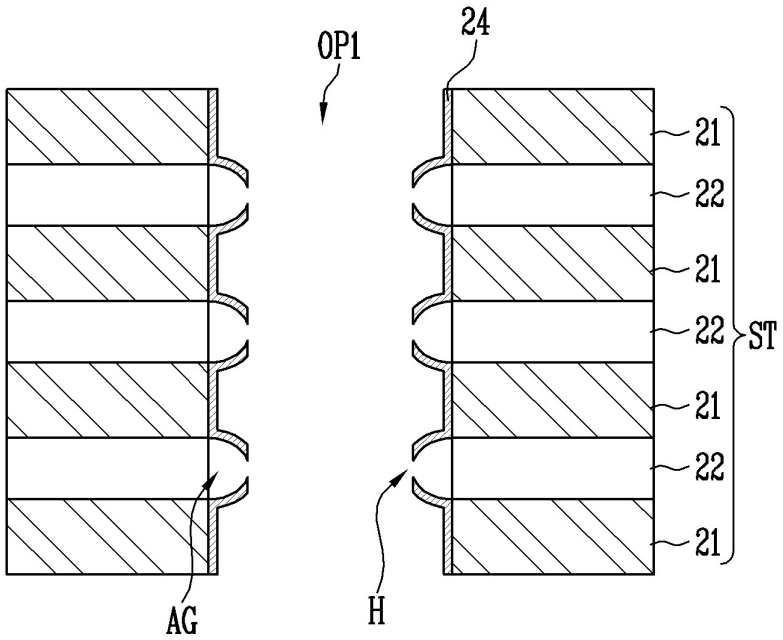

OP1
24
21
22
21
22
ST
21
22
21
AG
H

FIG. 2F

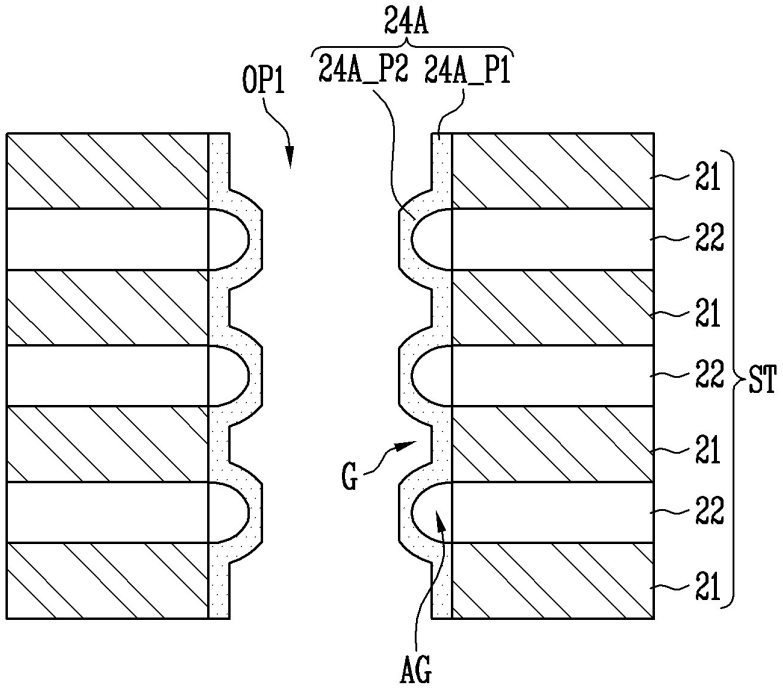

24A
24A_P2
24A_P1
OP1
21
22
21
22
ST
21
22
21
G
AG

FIG. 2G

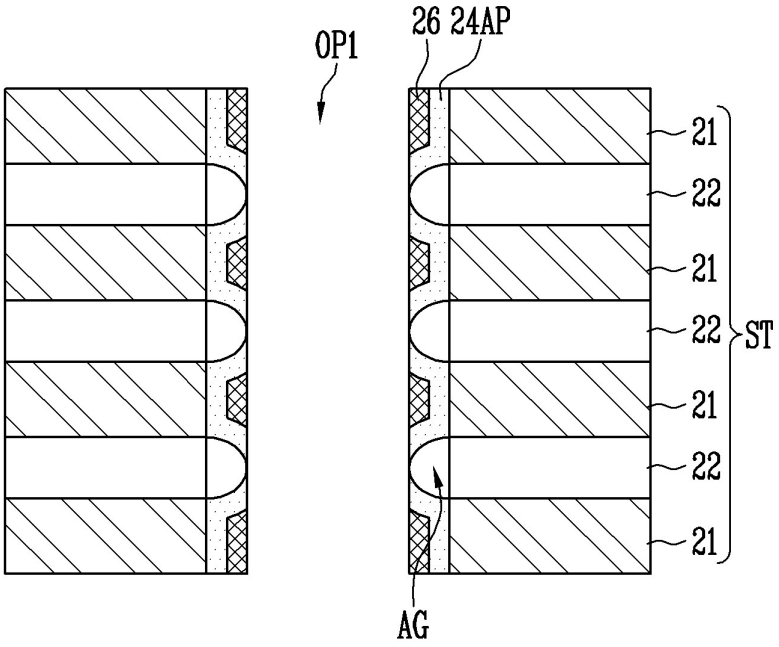

OP1
26
24AP
21
22
21
22
ST
21
22
21
AG

FIG. 2H

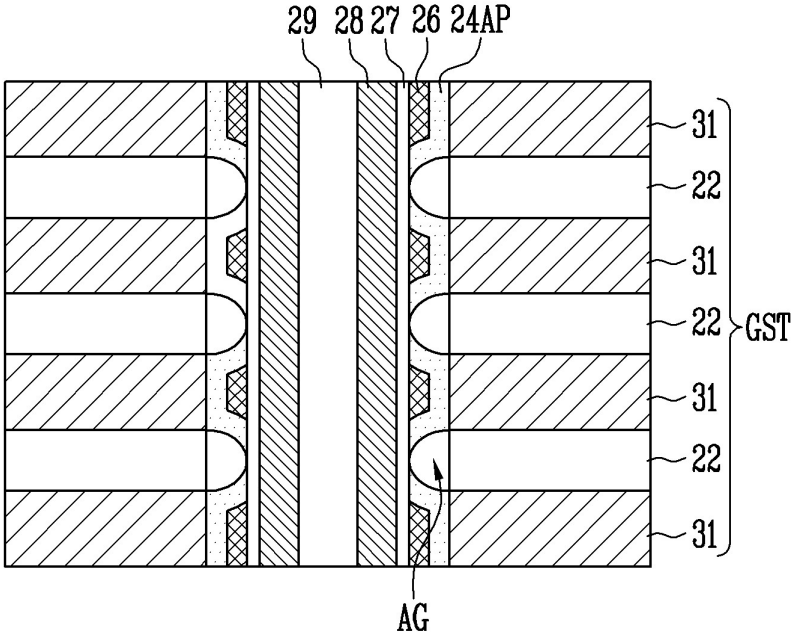

29
28
27
26
24AP
31
22
31
22
GST
31
22
31
AG

FIG. 3A

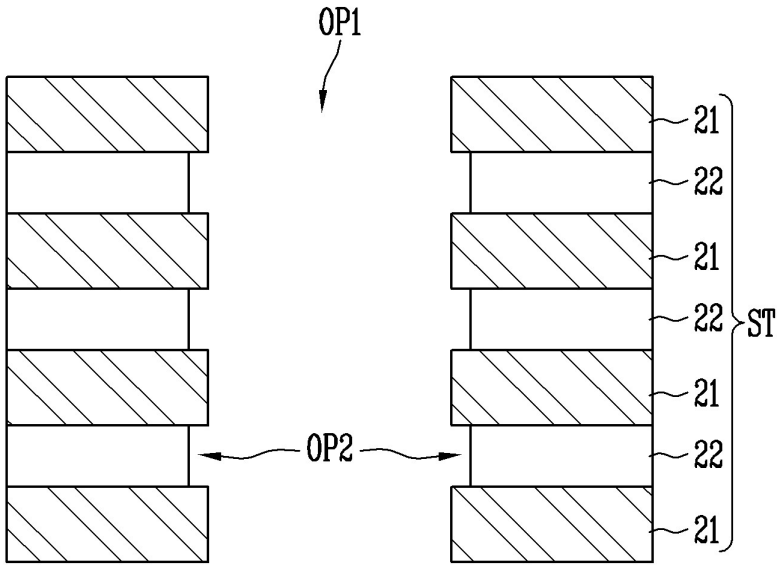


FIG. 3B

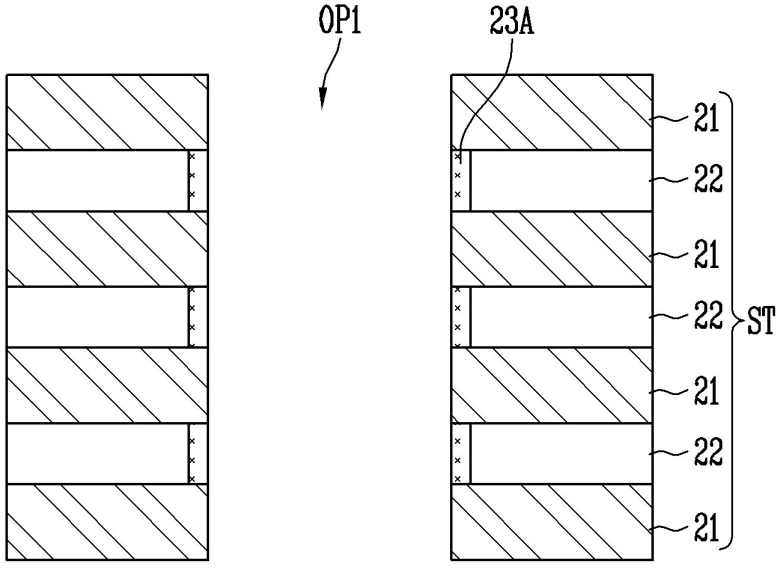


FIG. 3C

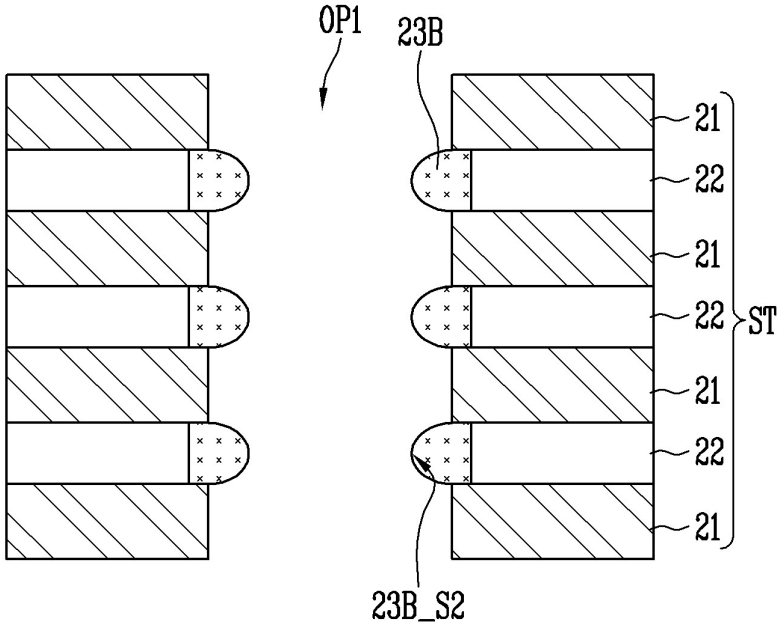

OP1
23B
21
22
21
22
ST
21
22
21
23B_S2

FIG. 3D

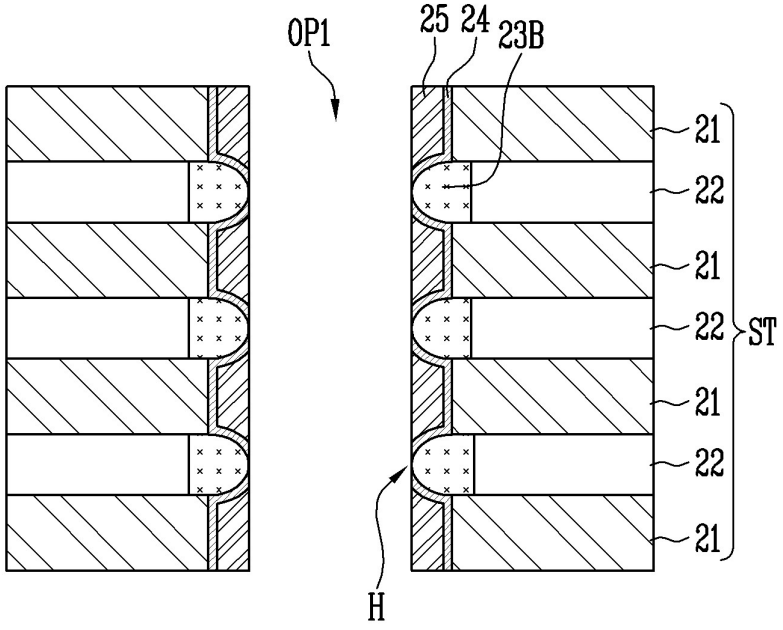

OP1
25
24
23B
21
22
21
22
ST
21
22
21
H

FIG. 3E

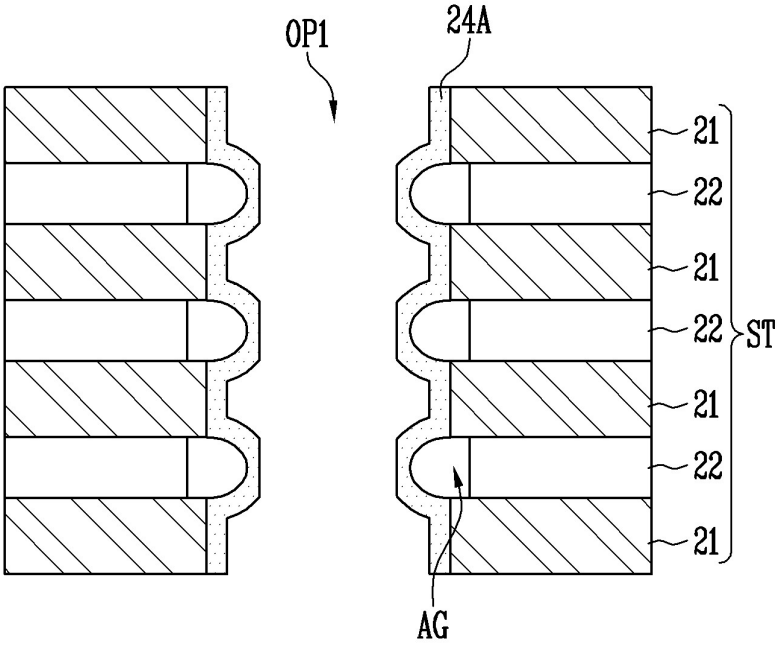


FIG. 4A

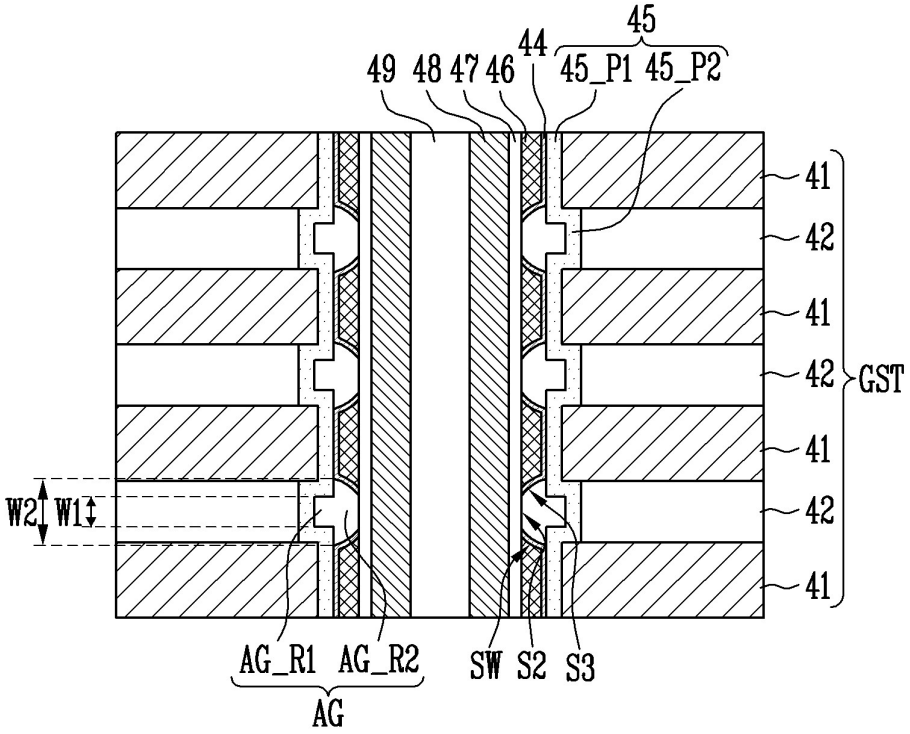

45
44
49 48 47 46
45_P1 45_P2
41
42
41
42
GST
41
42
41
W2
W1
AG_R1 AG_R2
AG
SW S2 S3

FIG. 4B

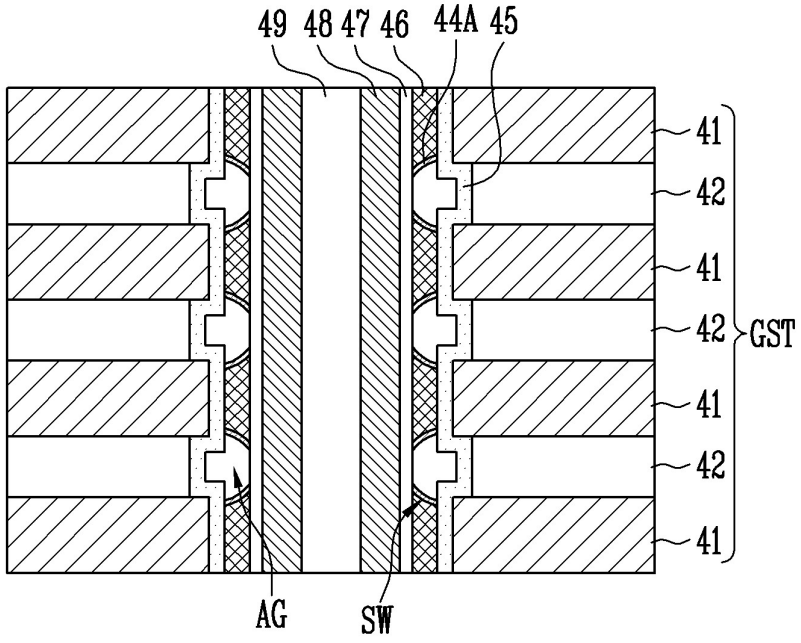

49 48 47 46 44A 45
41
42
41
42
GST
41
42
41
AG
SW

FIG. 4C

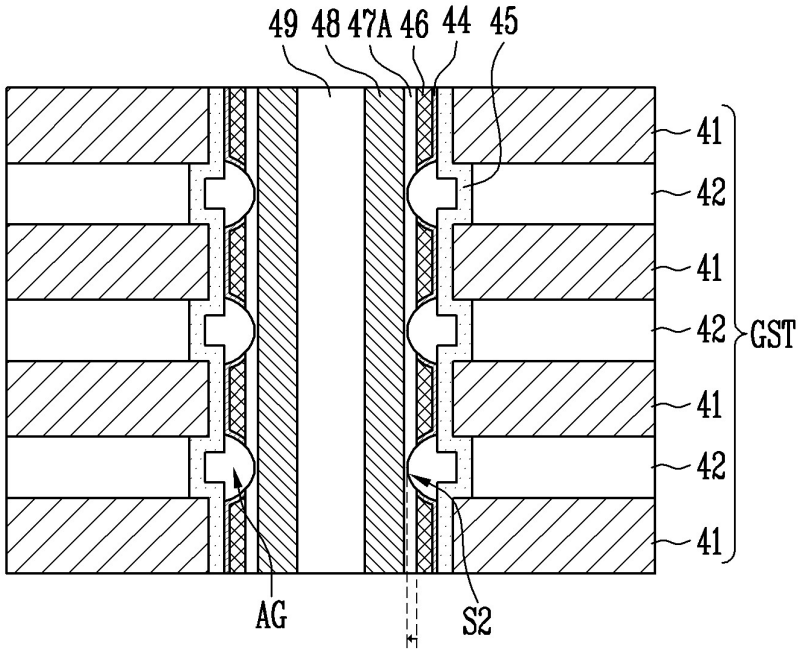


FIG. 5A

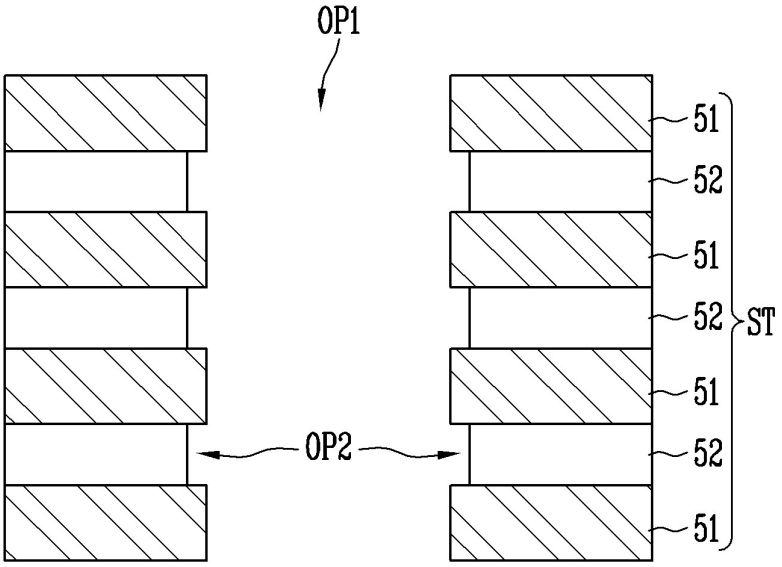

OP1
51
52
51
52
ST
51
OP2
52
51

FIG. 5B

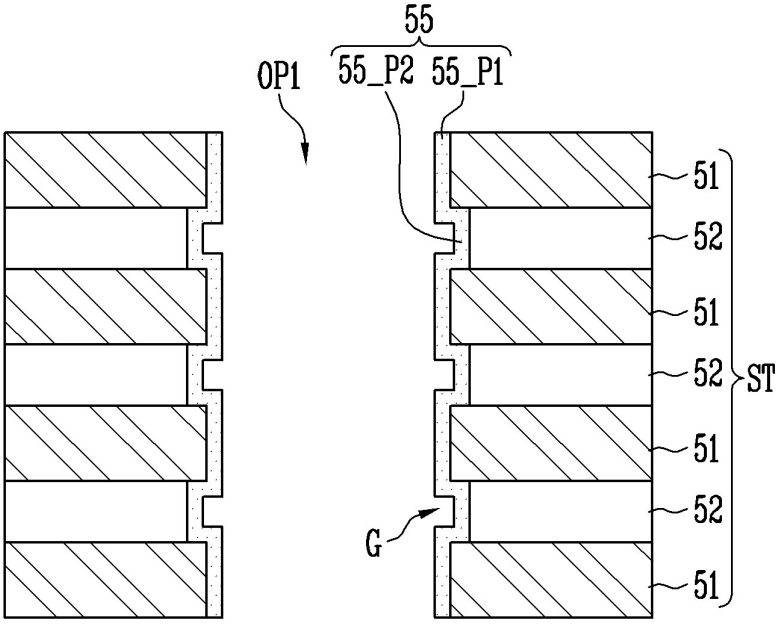

55
55_P2
55_P1
OP1
51
52
51
52
ST
51
G
52
51

FIG. 5C

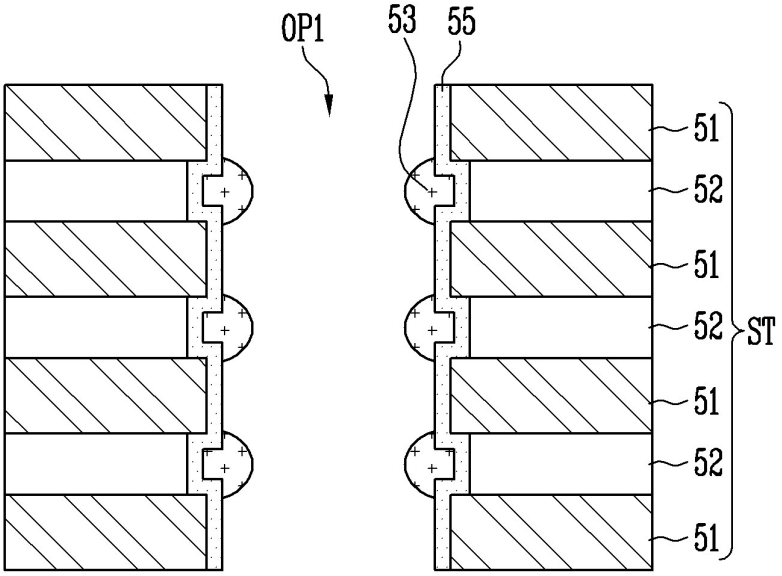


FIG. 5D

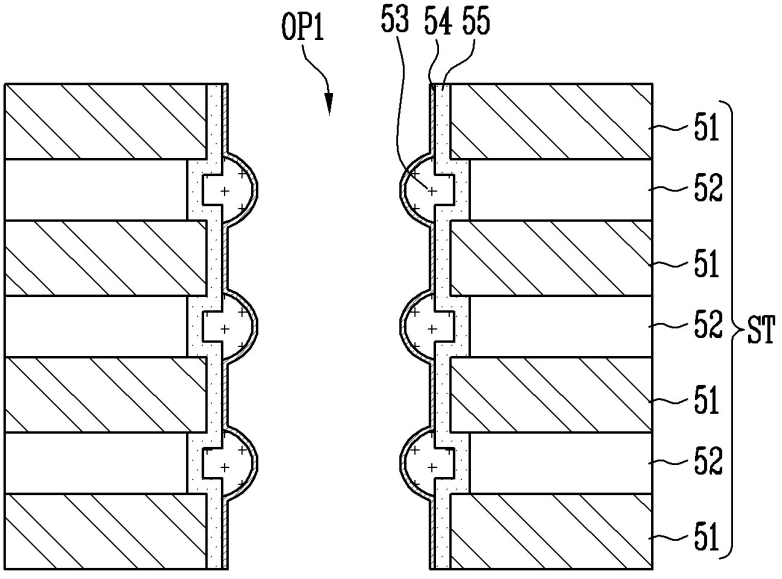


FIG. 5E

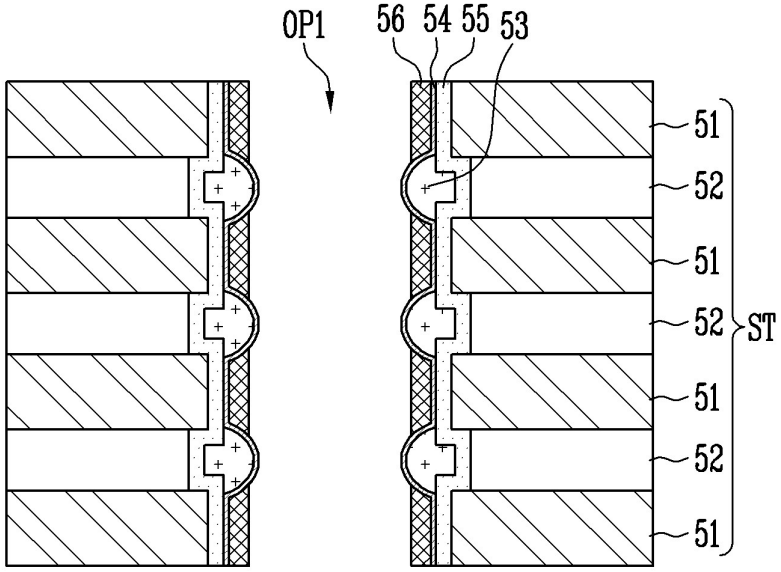

OP1
56
54
55
53
51
52
51
52
ST
51
52
51

FIG. 5F

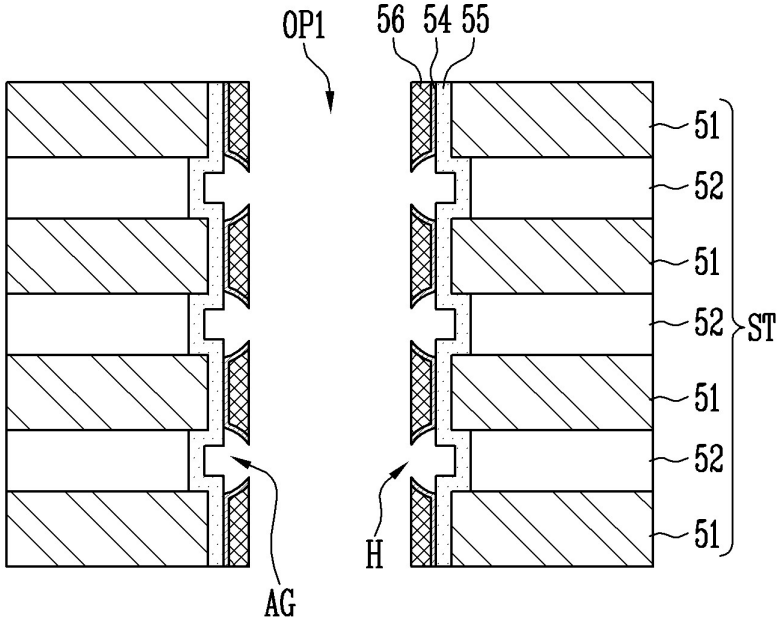

OP1
56
54
55
51
52
51
52
ST
51
52
51
H
AG

FIG. 5G

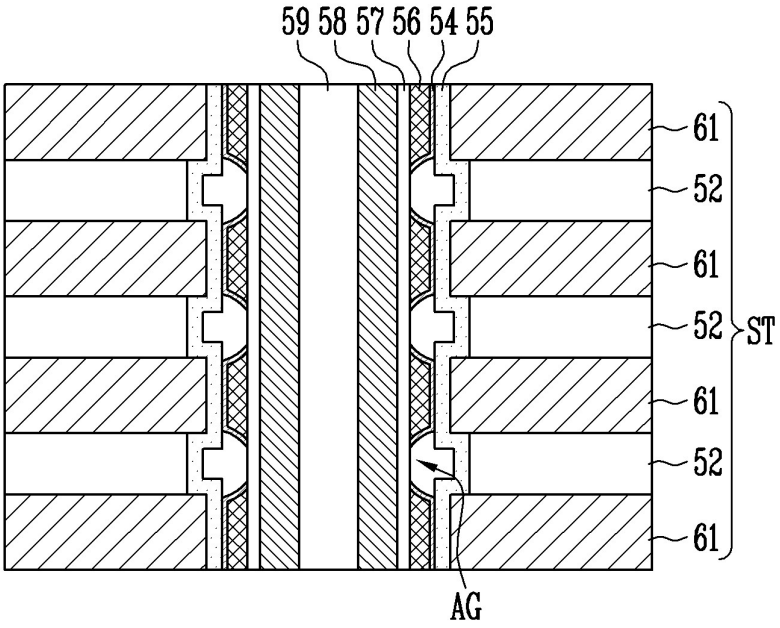


FIG. 6A

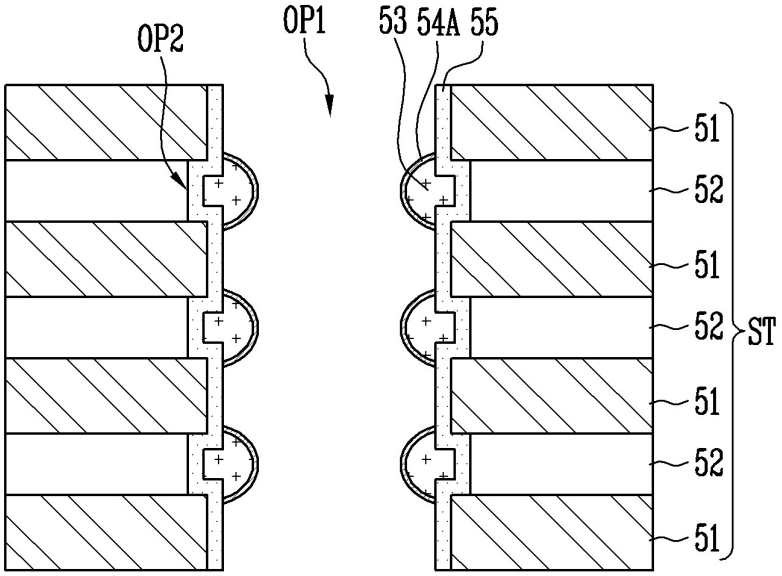

OP2
OP1
53
54A
55
51
52
51
52
51
52
51
ST

FIG. 6B

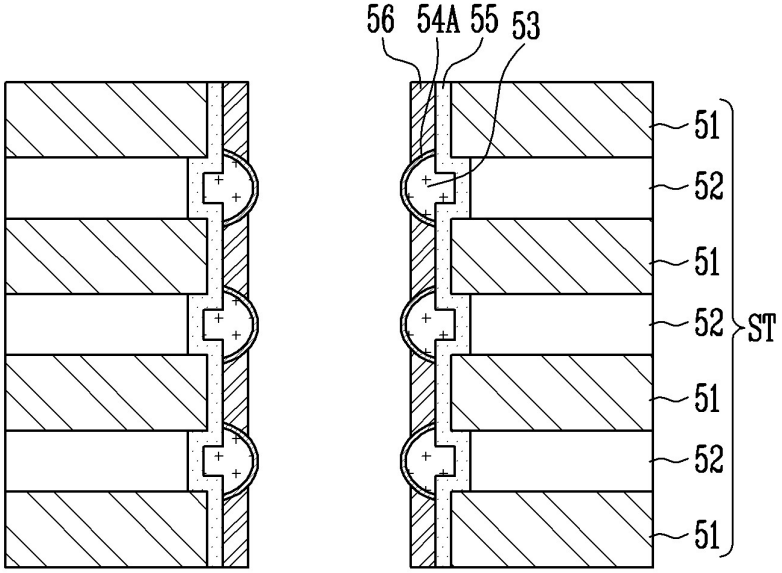

56
54A
55
53
51
52
51
52
51
52
51
ST

FIG. 7A

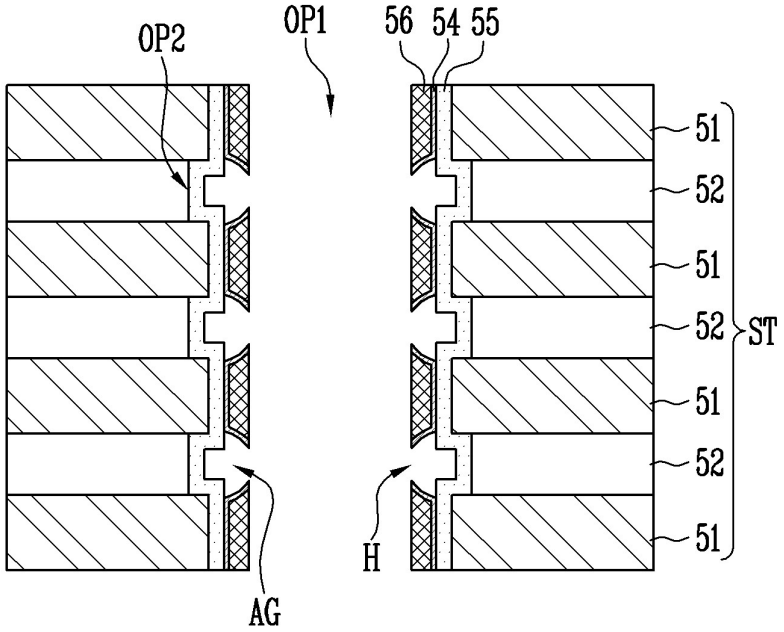

OP2
OP1
56
54
55
51
52
51
52
ST
51
52
51
H
AG

FIG. 7B

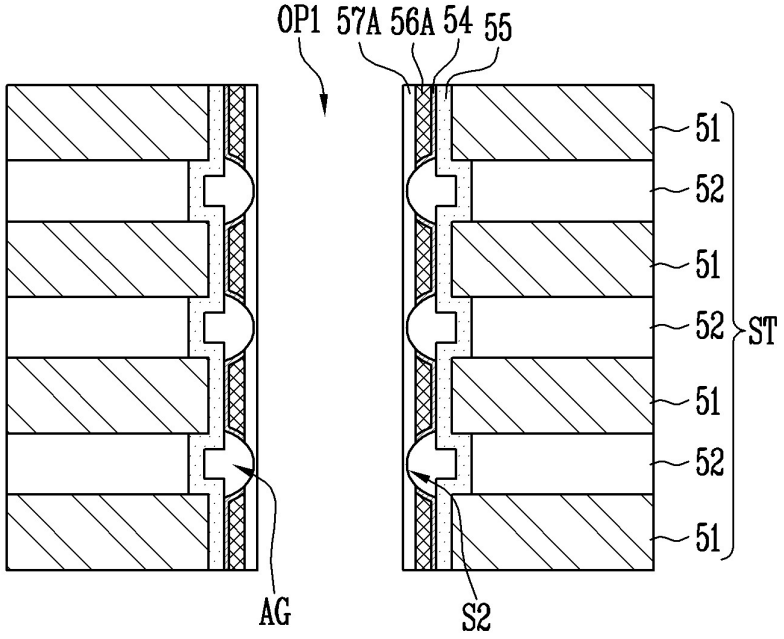

OP1
57A
56A
54
55
51
52
51
52
ST
51
52
51
AG
S2

FIG. 8A

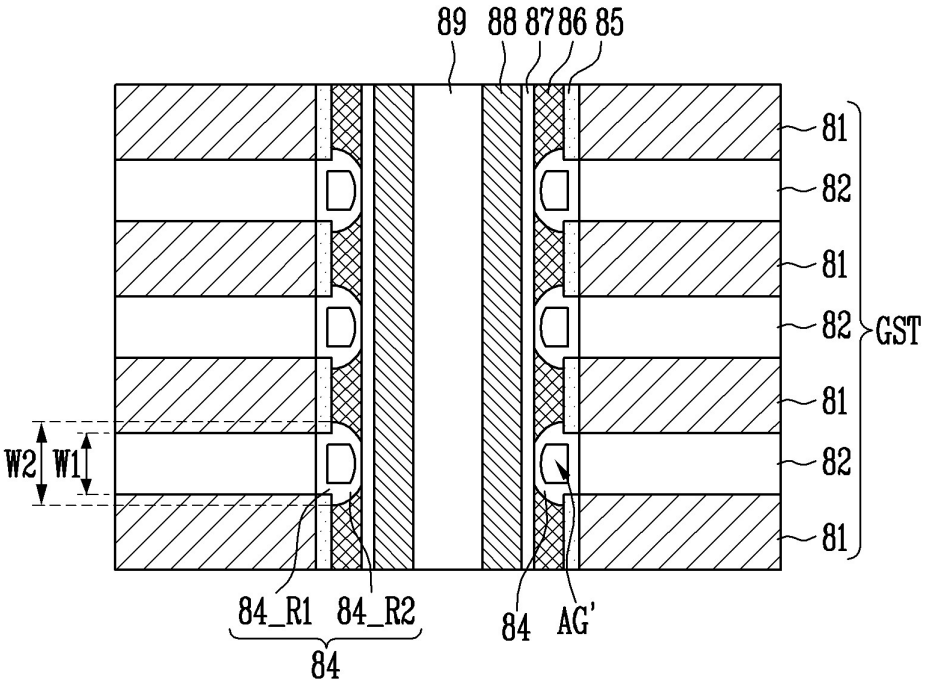

89
88
87
86
85
81
82
81
82
GST
81
82
81
W2
W1
84_R1
84_R2
84
84
AG'

FIG. 8B

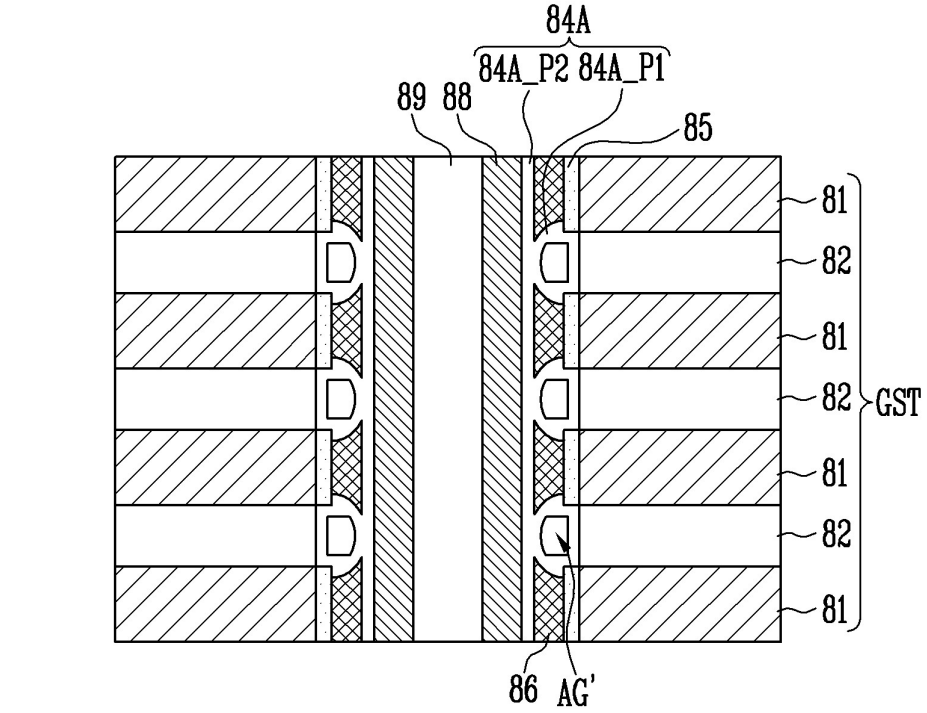

84A
84A_P2
84A_P1
89
88
85
81
82
81
82
GST
81
82
81
86
AG'

FIG. 8C

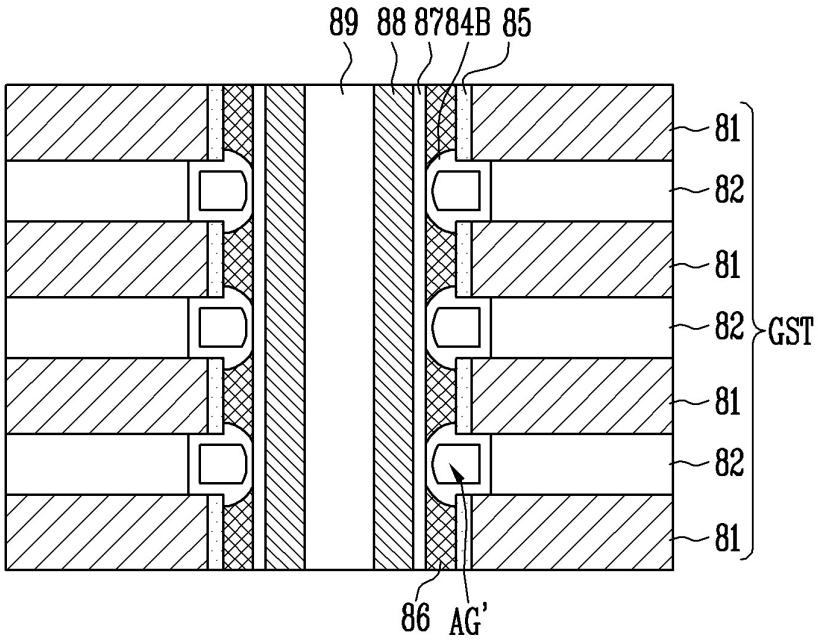


FIG. 9A

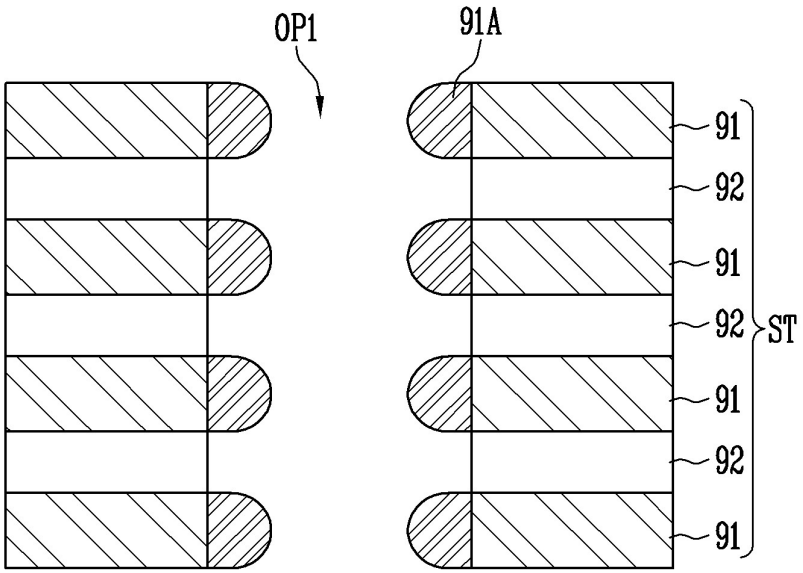


FIG. 9B

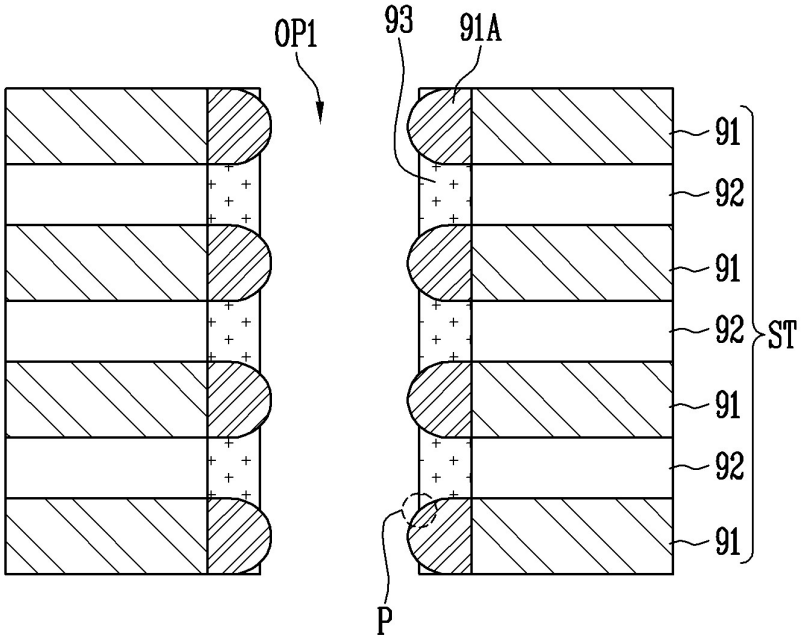


FIG. 9C

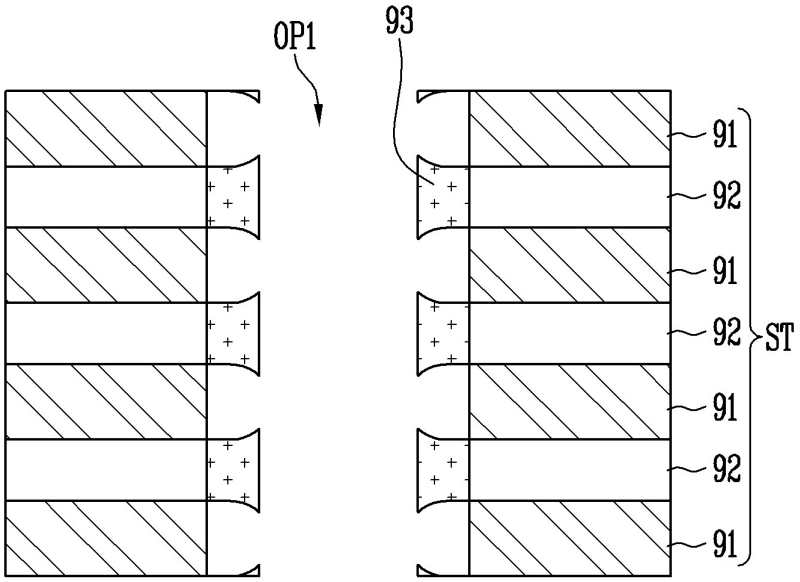


FIG. 9D

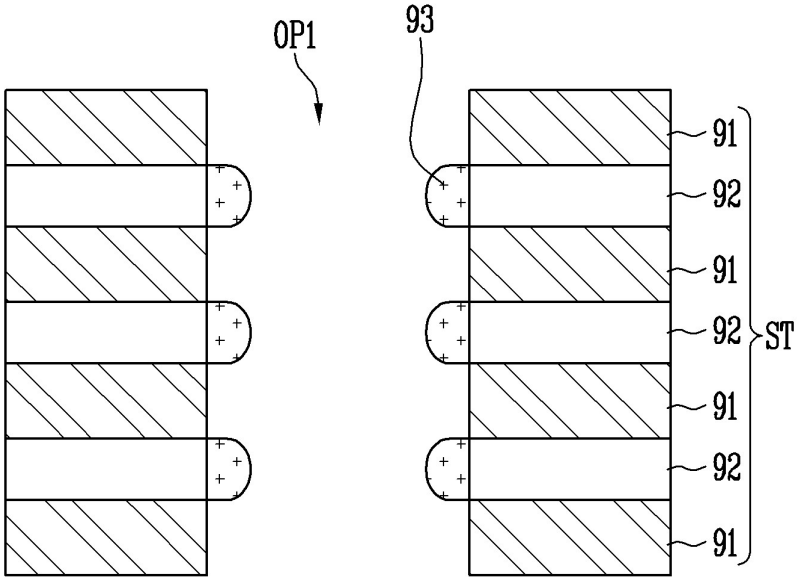


FIG. 9E

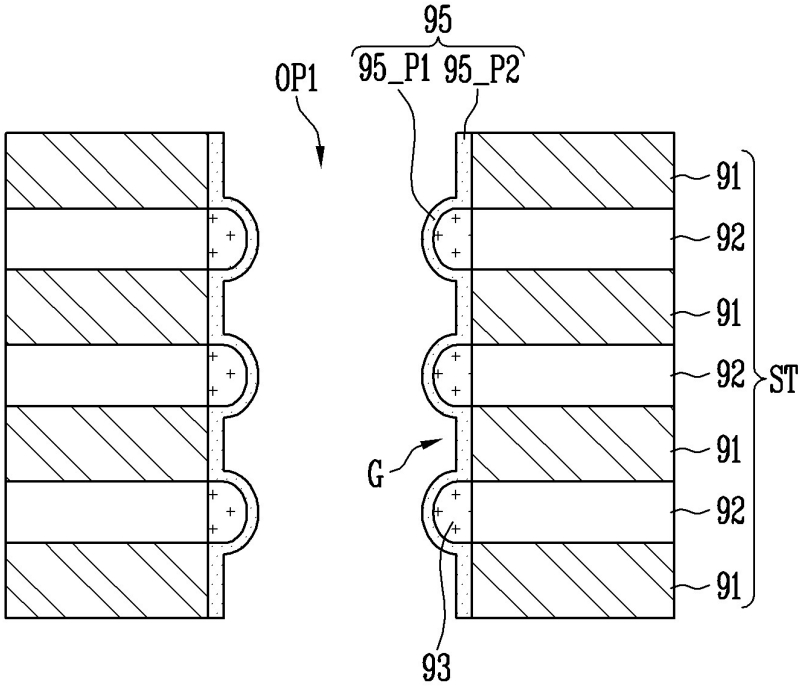

95
95_P1
95_P2
OP1
91
92
91
92
ST
G
91
92
91
93

FIG. 9F

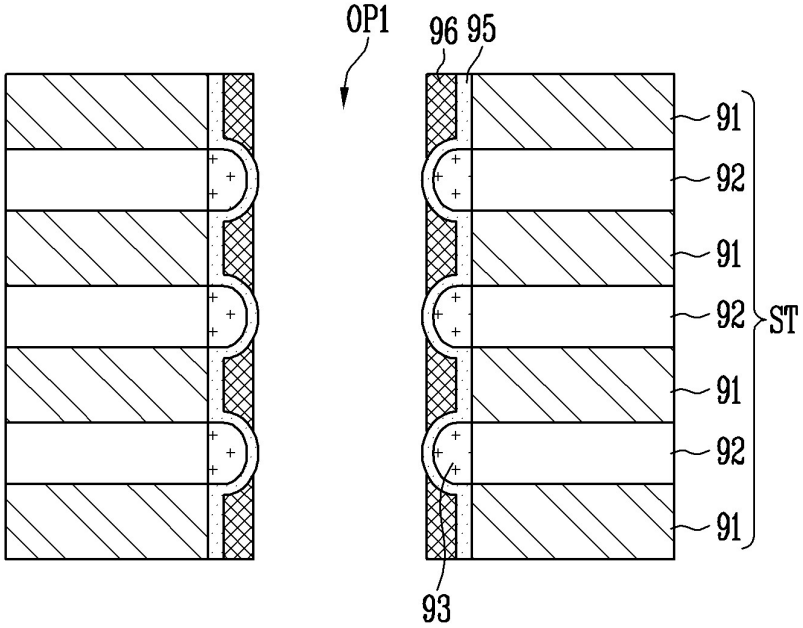

OP1
96
95
91
92
91
92
ST
91
92
91
93

FIG. 9G

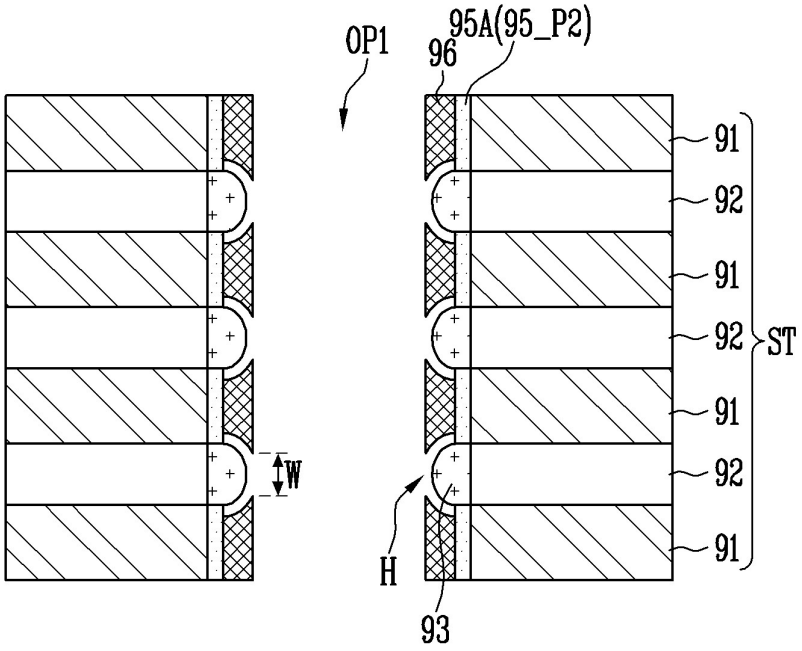

OP1
95A(95_P2)
96
91
92
91
92
91
92
91
ST
W
H
93

FIG. 9H

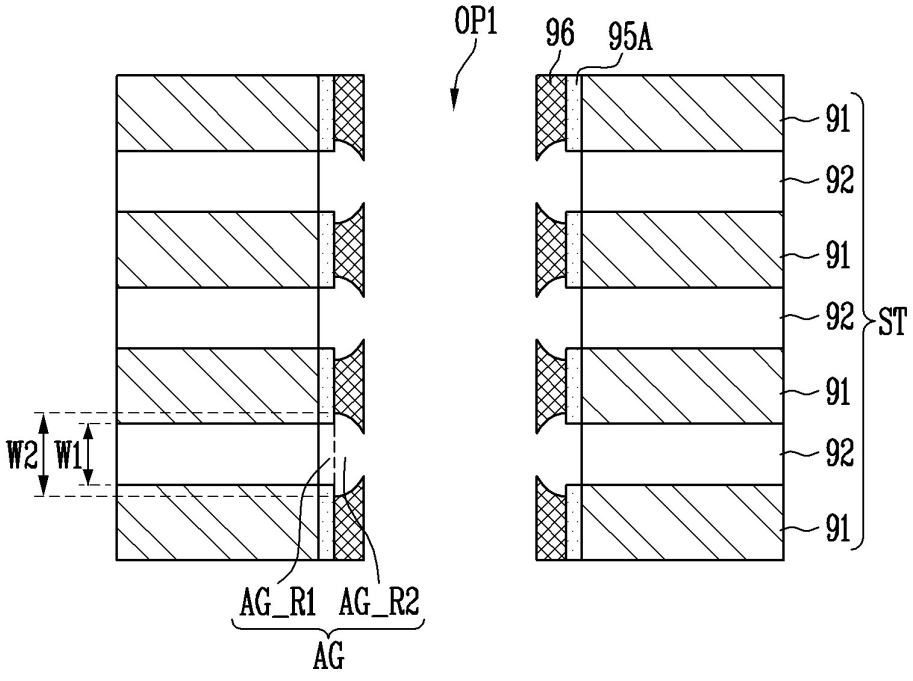

OP1
96
95A
91
92
91
92
91
92
91
ST
W2
W1
AG_R1
AG_R2
AG

FIG. 9I

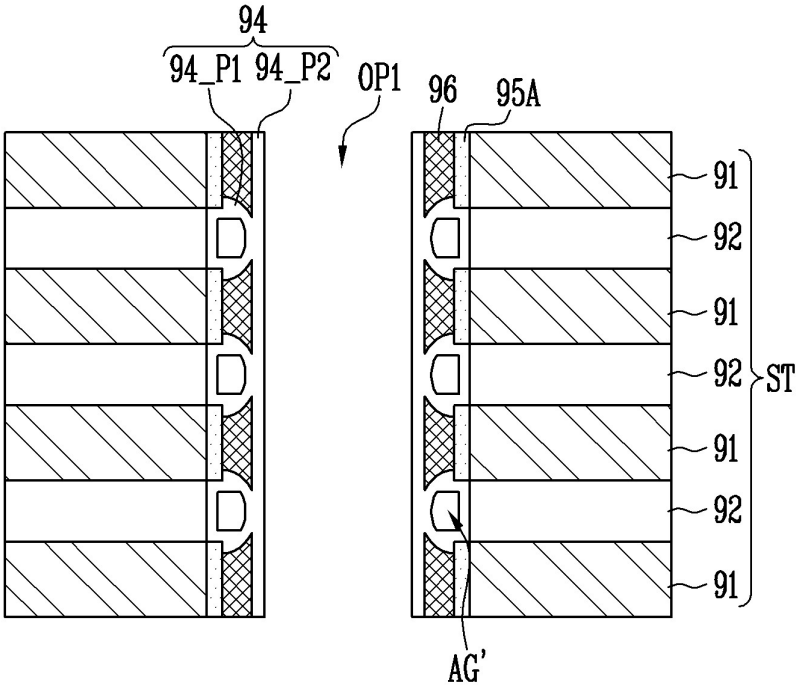

94
94_P1
94_P2
OP1
96
95A
91
92
91
92
ST
91
92
91
AG'

FIG. 9J

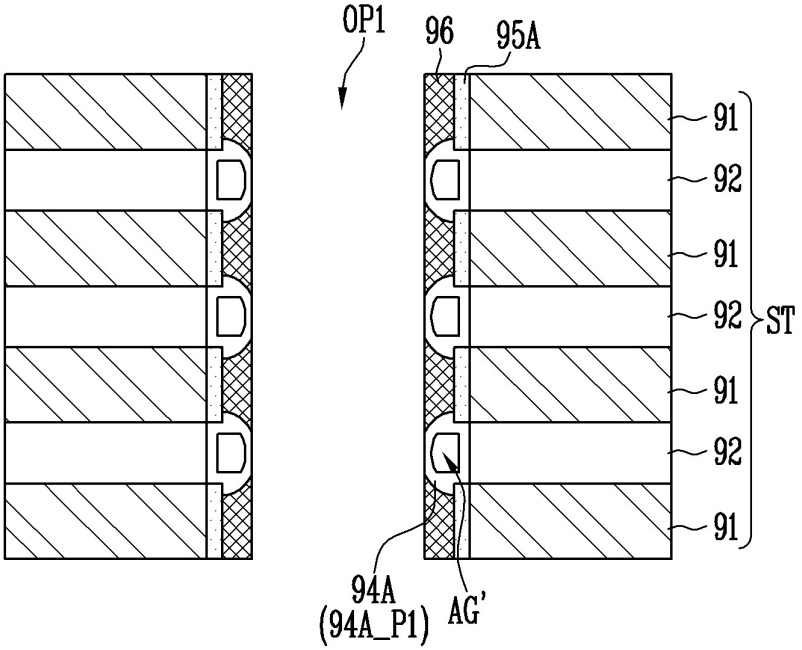

OP1
96
95A
91
92
91
92
ST
91
92
91
94A
(94A_P1)
AG'

FIG. 9K

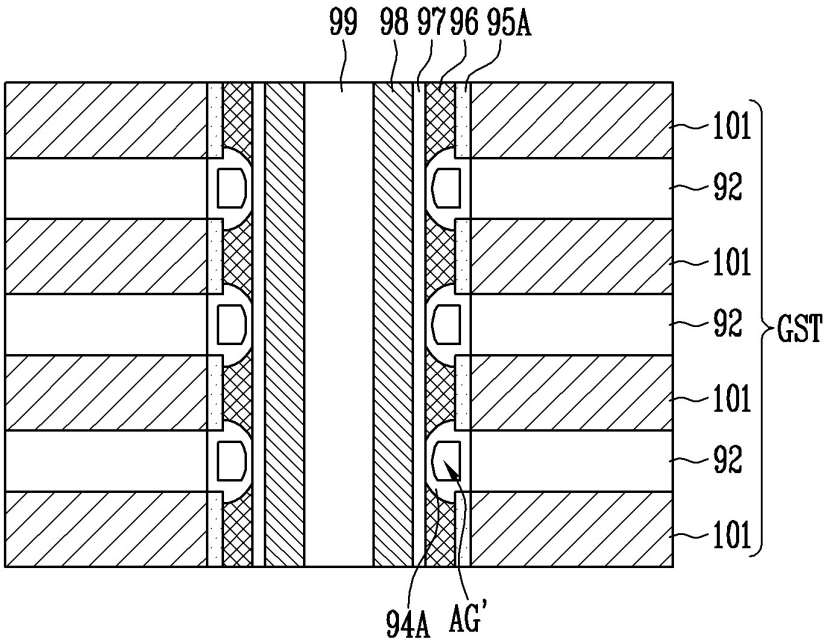


FIG. 10A

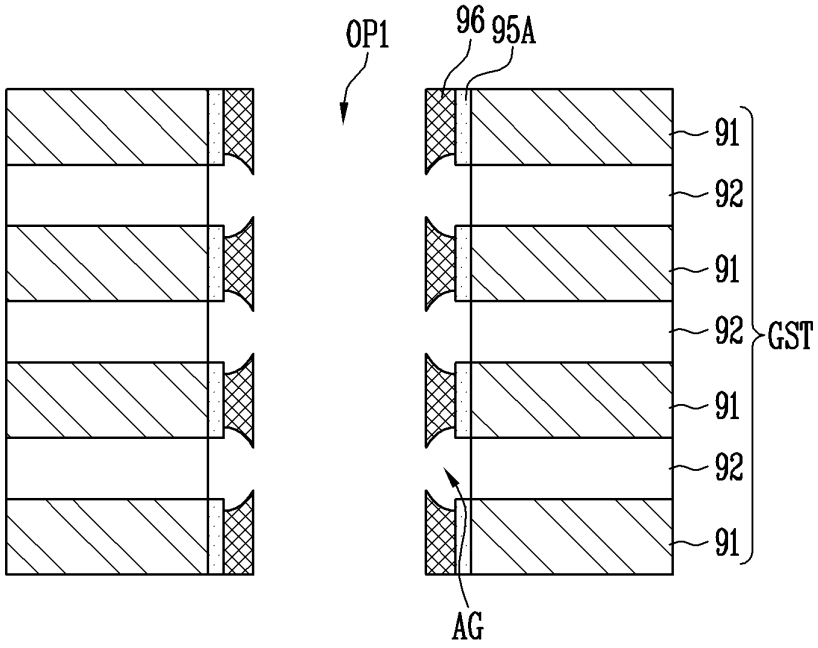


FIG. 10B

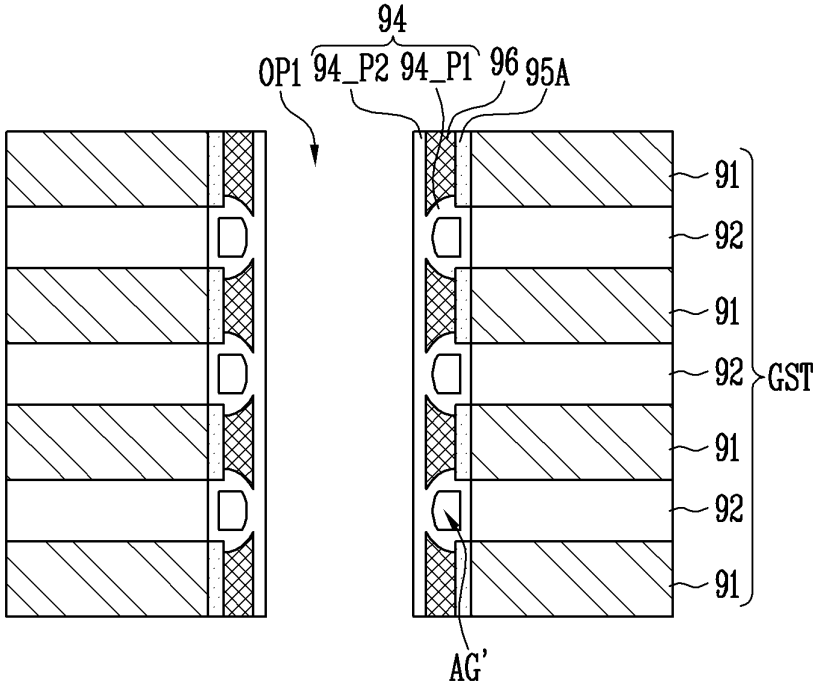


FIG. 10C

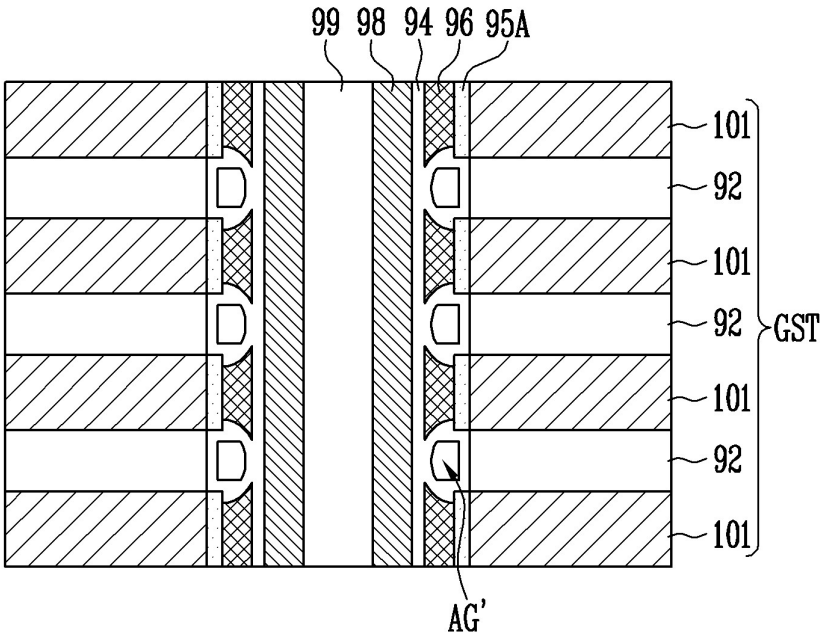


FIG. 11A

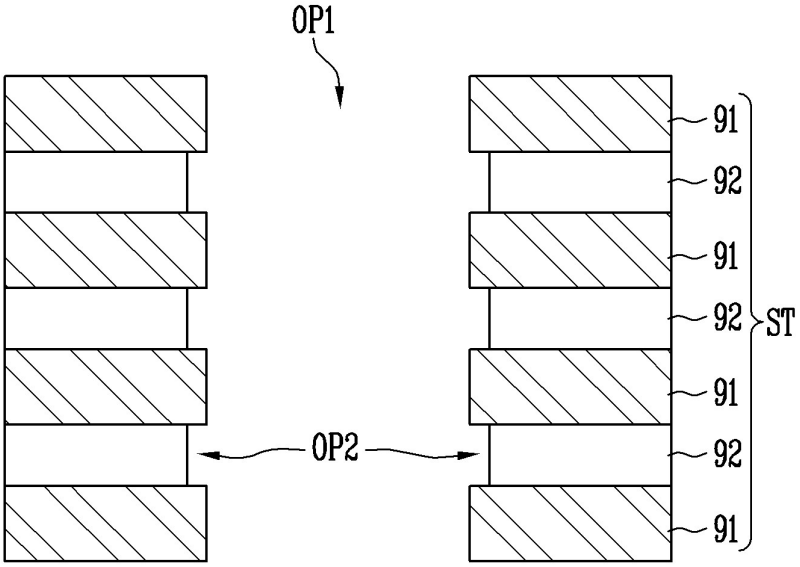


FIG. 11B

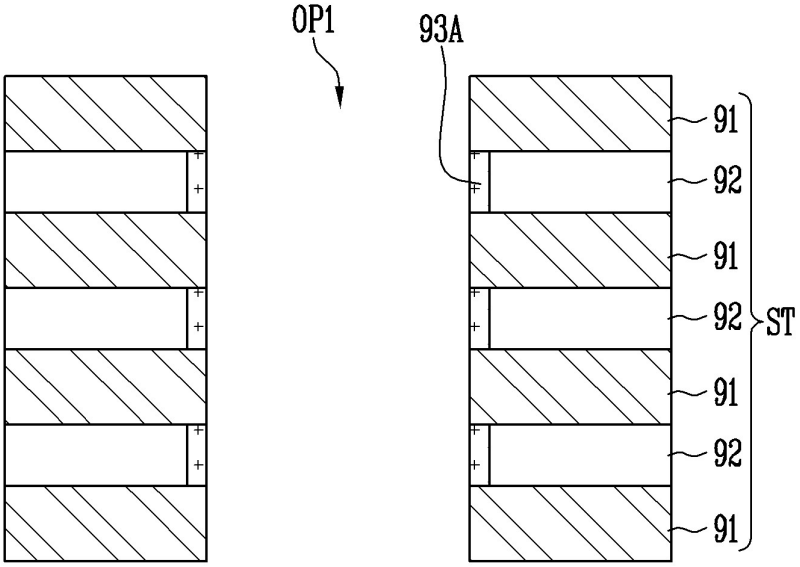


FIG. 11C

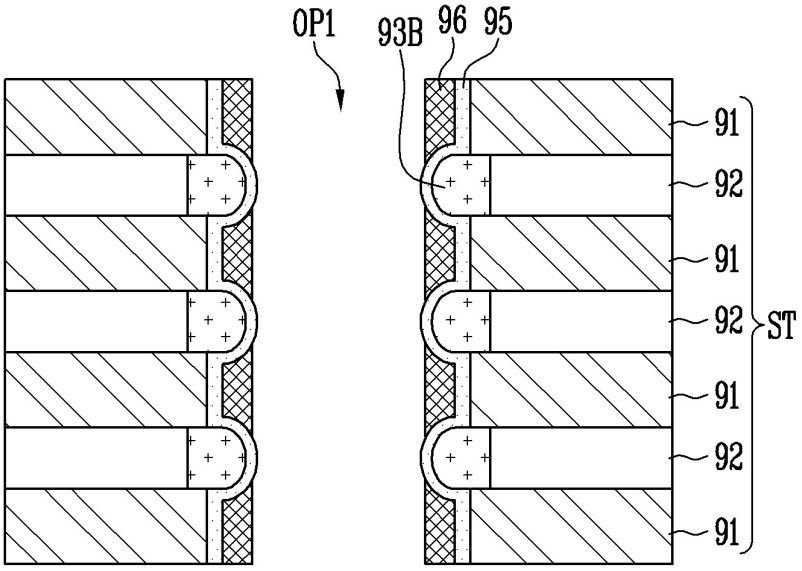


FIG. 11D

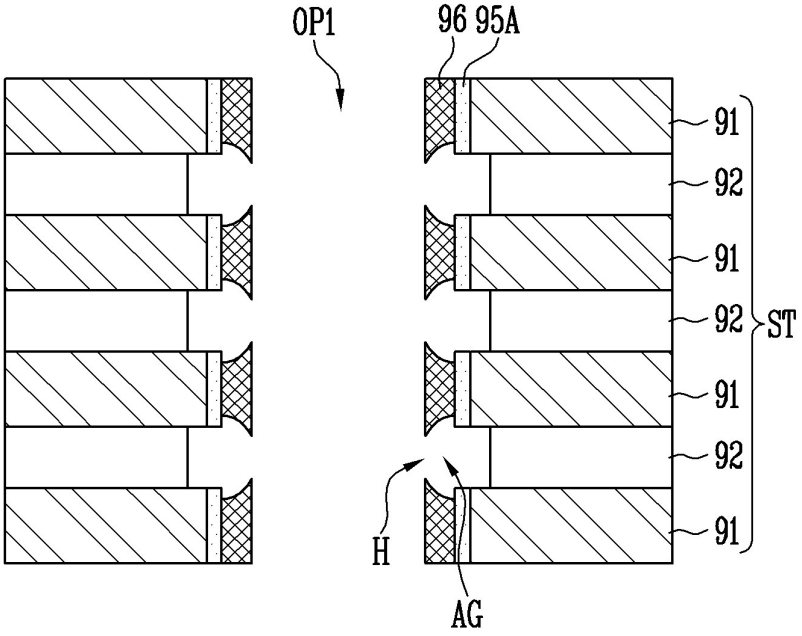


FIG. 11E

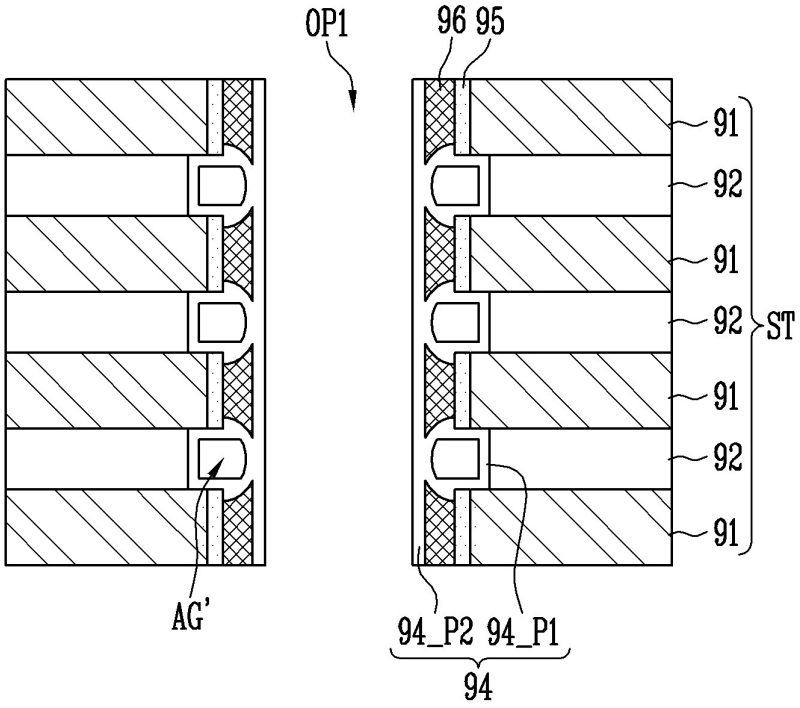


FIG. 12

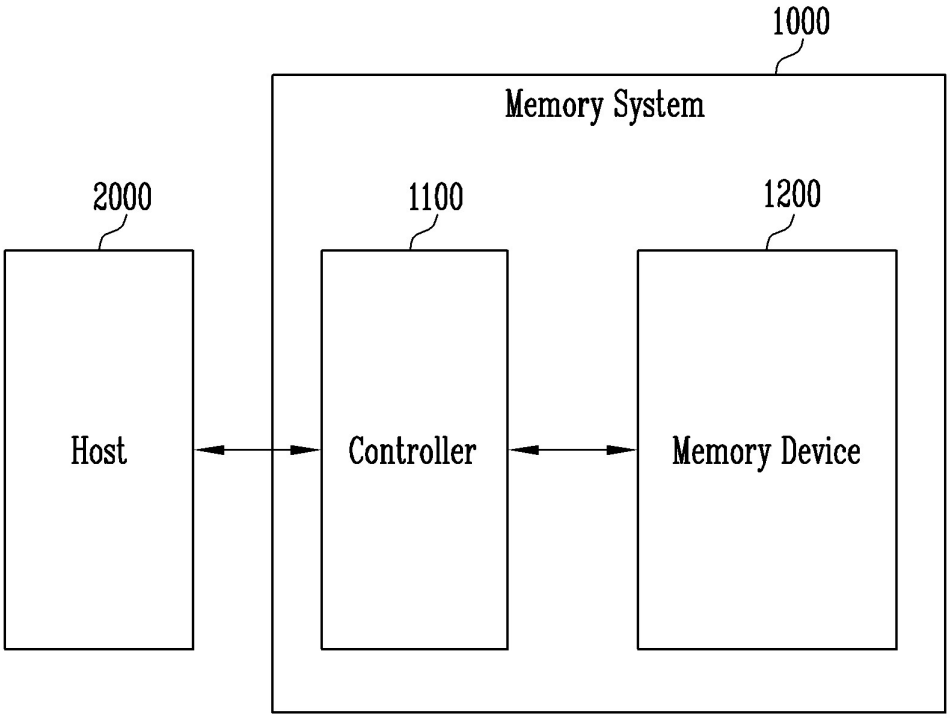

1000
Memory System
2000
1100
1200
Host
Controller
Memory Device

FIG. 13

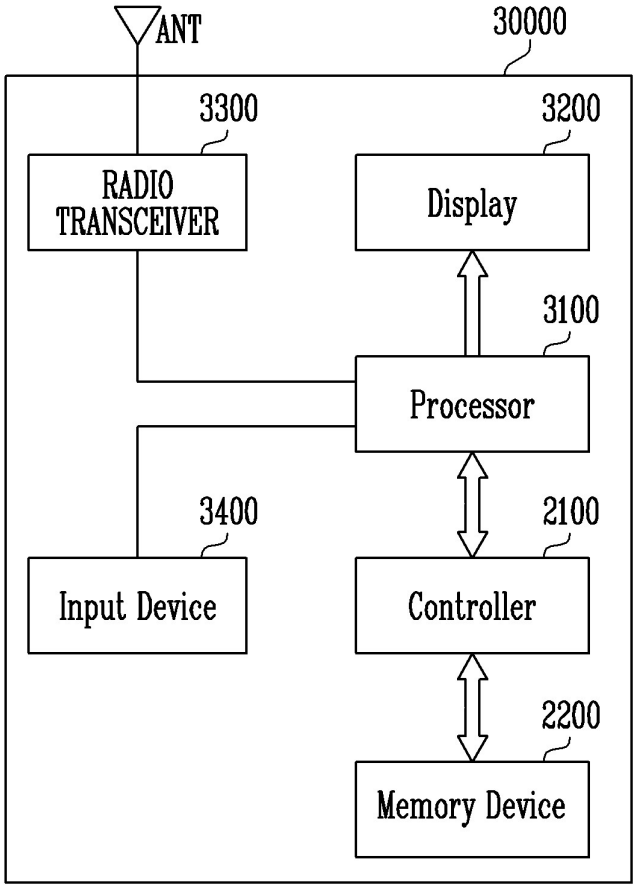

ANT
30000
3300
3200
RADIO TRANSCEIVER
Display
3100
Processor
3400
2100
Input Device
Controller
2200
Memory Device

FIG. 14

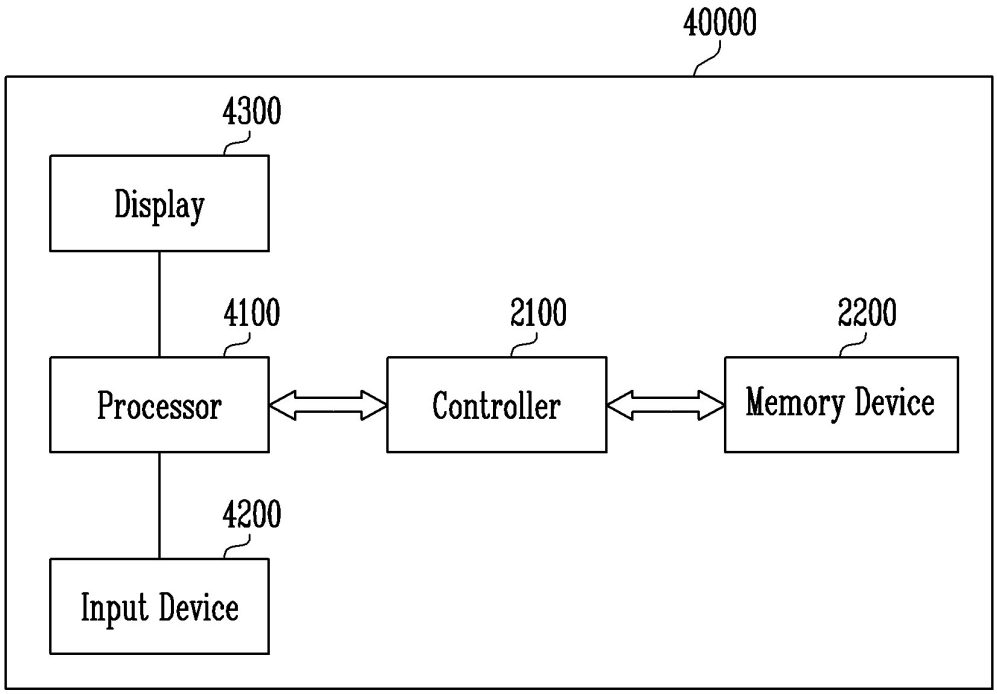

40000
4300
Display
4100
Processor
2100
Controller
2200
Memory Device
4200
Input Device

FIG. 15

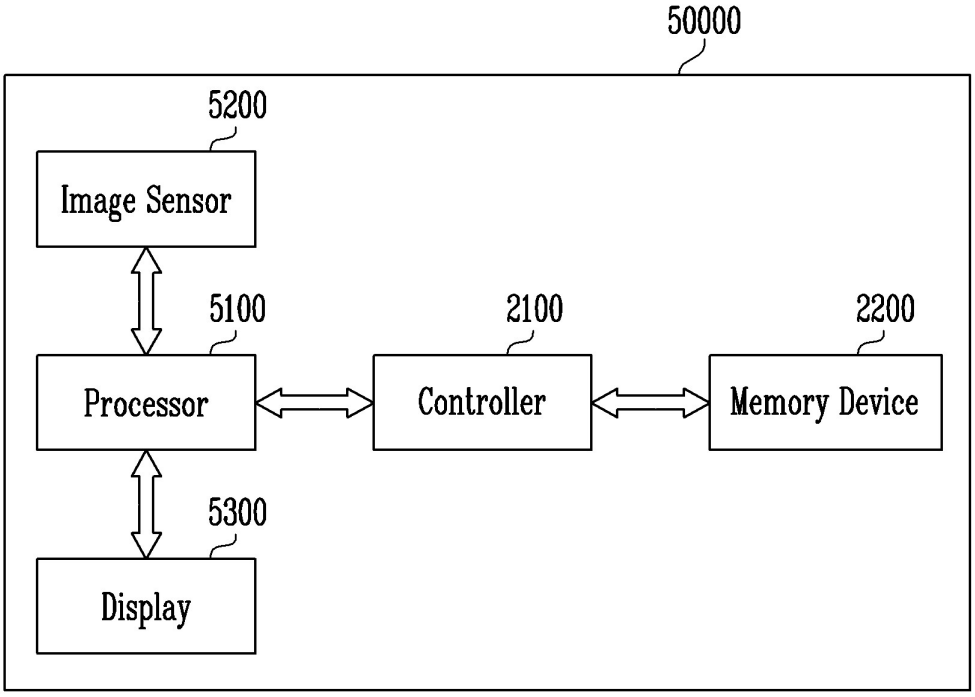
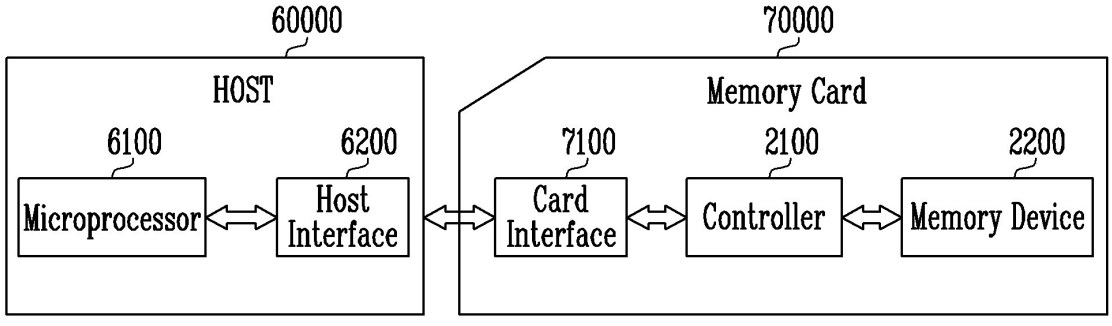

50000
5200
Image Sensor
5100
2100
2200
Processor
Controller
Memory Device
5300
Display

FIG. 16


60000
70000
HOST
Memory Card
6100
6200
7100
2100
2200
Microprocessor
Host Interface
Card Interface
Controller
Memory Device