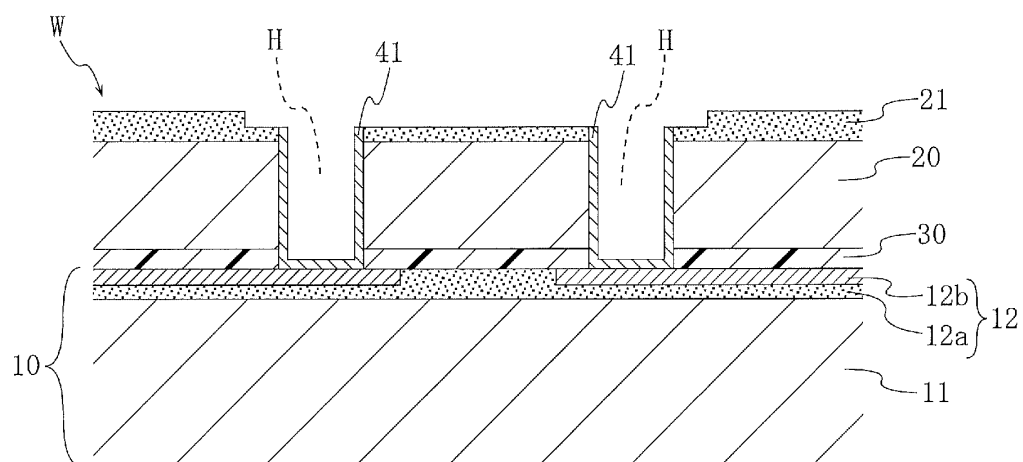


Figure 1 consists of three cross-sectional views of a semiconductor device, labeled (a), (b), and (c).

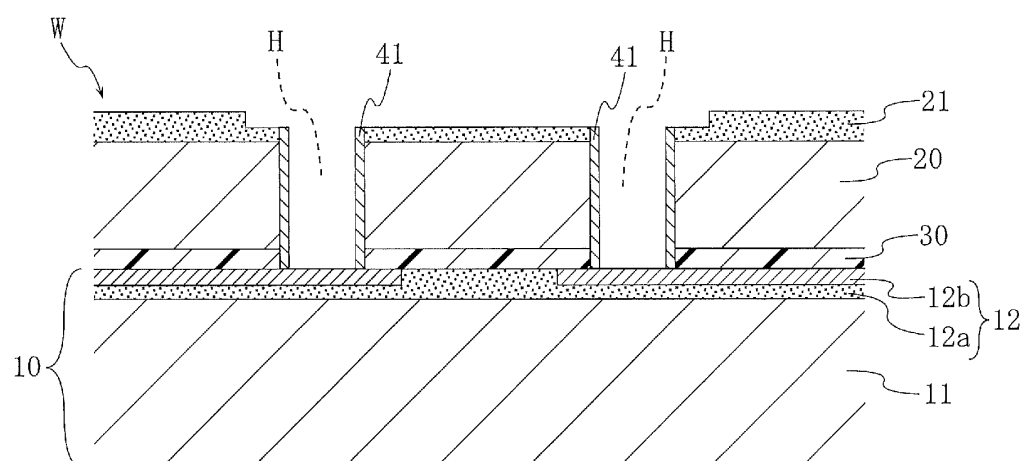
- (a)** Shows a substrate 11 with a layer 10 on top. Layer 10 is divided into regions 10a and 10b. A thin layer 20 is on top of 10a, with a sub-layer 20a. A layer 30 is on top of 10b. A layer 12 is on top of 10a, with sub-layers 12a and 12b. A layer 21 is on top of 10b.
- (b)** Shows the same structure as (a), but with a layer 20a on top of 10a, and a layer 21 on top of 10b. The layer 20a is shown with a dashed line, indicating it is a virtual layer.
- (c)** Shows the same structure as (b), but with a layer 20a on top of 10a, and a layer 21 on top of 10b. The layer 20a is shown with a dashed line, indicating it is a virtual layer. The layer 21 is shown with a dashed line, indicating it is a virtual layer.

[図2]

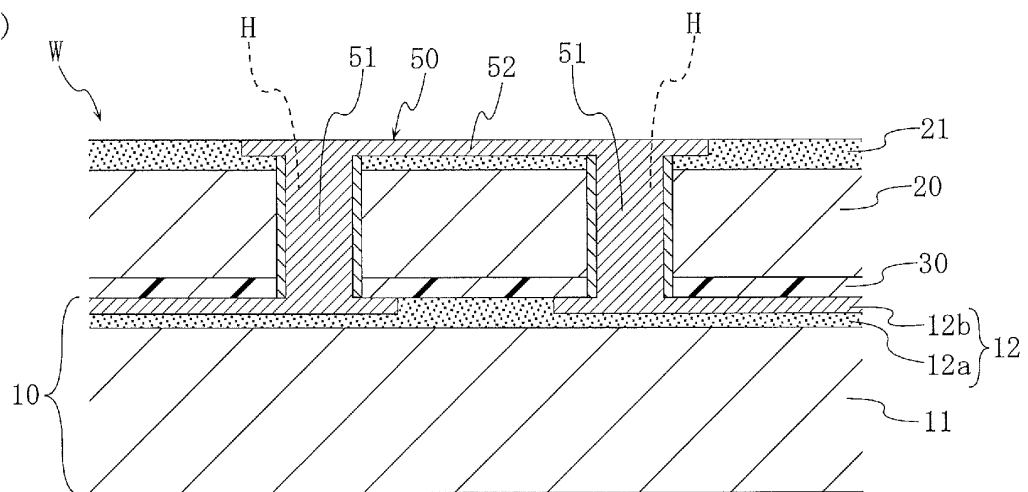
(a)



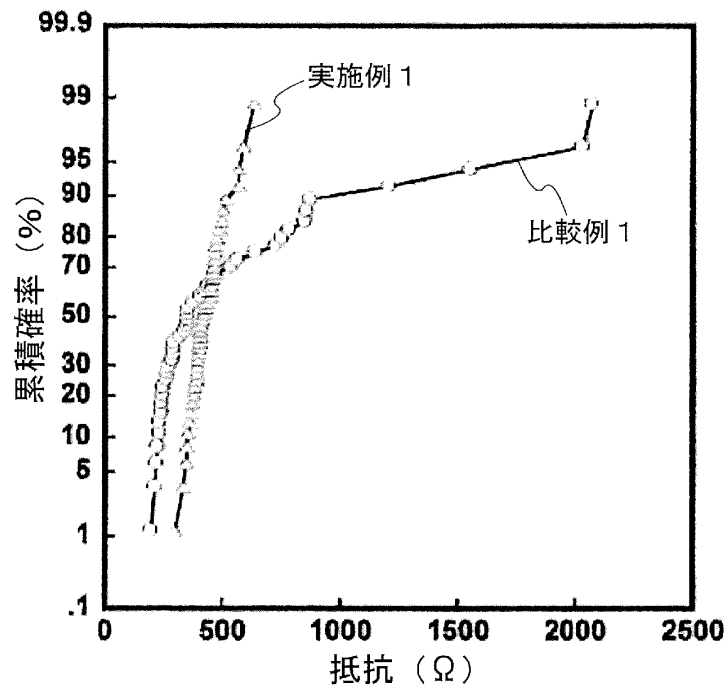
(b)



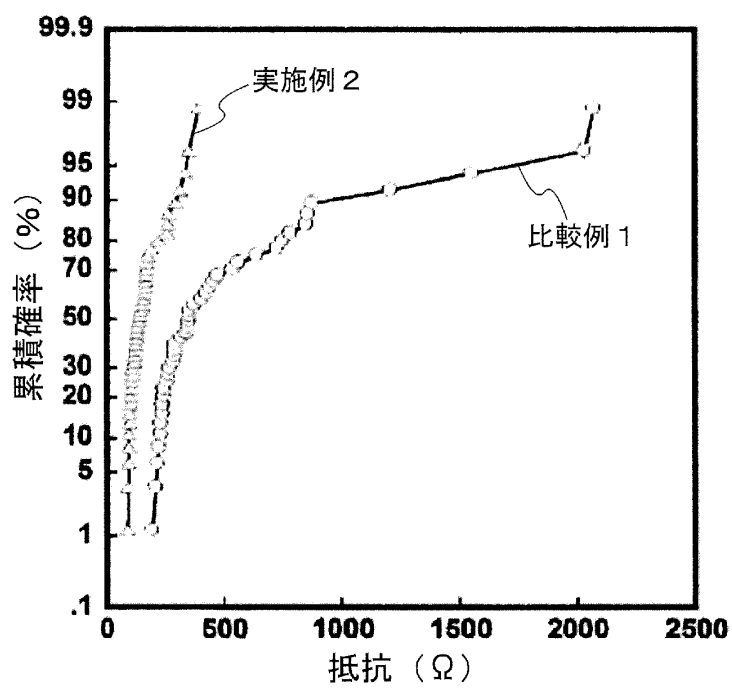
(a)



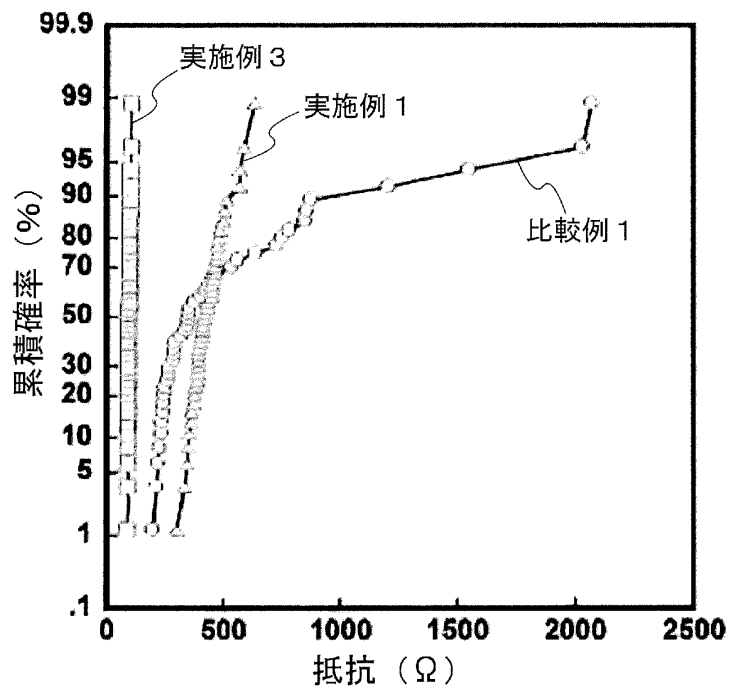
[図4]



[図5]



[図6]



[図7]

