WHAT IS CLAIMED IS:

1. A memory device, comprising:

a stack of alternating word line layers and insulating layers over a substrate, the stack including an array region and a first staircase region that are positioned adjacent to each other and arranged in a length direction of the substrate, the word line layers including a bottom select gate (BSG) over the substrate;

first dielectric trenches formed in only the BSG of the word line layers and extending in the length direction of the substrate through the array region and through the first staircase region to separate the BSG into a plurality of sub-BSGs; and

a first common source region (CSR) formed over the substrate and extending in the length direction of the substrate, the first CSR further extending through the word line layers, and the insulating layers in a height direction of the substrate.

2. The memory device of claim 1, wherein the first CSR is arranged between two adjacent first dielectric trenches of the first dielectric trenches.

3. The memory device of claim 1, wherein the word line layers further include a top select gate (TSG) positioned over the substrate and the BSG.

4. The memory device of claim 3, further comprising:

second dielectric trenches formed in the TSG of the word line layers and extending in the length direction of the substrate to separate the TSG into a plurality of sub-TSGs.

5. The memory device of claim 1, further comprising a second staircase region.

6. The memory device of claim 5, wherein the array region is positioned between the first staircase region and the second staircase region in the length direction of the substrate.

7. The memory device of claim 6, wherein:

the memory device further includes a second CSR and a third CSR that are formed over the substrate, extend in the length direction of the substrate, and further extend through the word line layers, and the insulating layers in the height direction of the substrate,

the second CSR, the first CSR, and the third CSR are arranged sequentially in a width direction of the substrate so that the two adjacent first dielectric trenches of the first dielectric trenches are arranged between the second CSR and the third CSR,

the second CSR, the first CSR, and the third CSR extend in parallel to each other in the length direction of the substrate, and

the second CSR, the first CSR, and the third CSR extend through the first staircase region, the array region, and the second staircase region sequentially in the length direction of the substrate.

8. The memory device of claim 1, wherein the first CSR has a discontinuous profile that includes a first portion and a second portion being aligned in the length direction of the substrate.

9. The memory device of claim 7, further comprising:

a plurality of channel structures that extend through the word line layers and the insulating layers in the height direction of the substrate, positioned in the array region, and arranged between the second CSR and the third CSR.

10. The memory device of claim 7, further comprising:

a plurality of dummy channel structures that extend through the word line layers and the insulating layers in the height direction of the substrate, positioned in the first staircase region and the second staircase region, and arranged between the second CSR and the third CSR.

11. The memory device of claim 4, wherein the first CSR is arranged between two adjacent second dielectric trenches of the second dielectric trenches.

12. The memory device of claim 3, wherein the TSG is an uppermost word line layer of the word line layers.

13. The memory device of claim 1, wherein the BSG is a lowermost word line layer of the word line layers.

14. The memory device of claim 6, wherein the first dielectric trenches extend through the first staircase region, the array region, and the second staircase region in the length direction of the substrate.

15. The memory device of claim 4, wherein the second dielectric trenches extend through the array region in the length direction of the substrate.