METHOD FOR PACKAGING CIRCUITS AND PACKAGED CIRCUITS

Abstract

A method for packaging integrated circuit chips (die) is described that includes providing a base substrate with package level contacts, coating a base substrate with adhesive, placing dies on the adhesive, electrically connecting the die to the package level contacts, and removing the backside of the base substrate to expose the backside of the package level contacts. Accordingly, an essentially true chip scale package is formed. Multi-chip modules are formed by filling gaps between the chips with an encapsulant. In an embodiment, chips are interconnected by electrical connections between package level contacts in the base substrate. In an embodiment, substrates each having chips are adhered back-to-back with through vias formed in aligned saw streets to interconnect the back-to-back chip assembly.



