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SEMICONDUCTOR DEVICE

Field of the Invention

The present invention relates to the field of semiconductor devices, and in particular, to conductive layers for semiconductor devices.

Background of the Invention

Aluminum is widely used for interconnects in semiconductor devices. However, aluminum has been found to be susceptible to a number of problems that may lead to device failure. Component densities (number of components per substrate area within an integrated circuit) typically are becoming higher as the size of components within a semiconductor device become smaller. The higher component density typically causes higher current densities in conductive layers when the device is operating. The higher current density generally results in an increase of device failure because of electromigration, which is a current-induced mass transport that is a function of current density and temperature of the device. Pure aluminum has problems with electromigration. In addition to electromigration, corrosion of the aluminum is a problem and is usually caused by chlorine exposure to the aluminum in an ambient including water, such as air exposure of an aluminum layer immediate following a dry etching step using chlorine-containing chemistry.

In an attempt to solve the problems discussed above, an element, such as silicon (Si), copper (Cu), nickel (Ni), or chromium (Cr) has been added to aluminum to form alloys. In reality, these alloys either do not solve all of the problems previously discussed or cause other problems. Electromigration is typically measured in terms of median-time-to-fail (MTTF) for a given current density and temperature. At a current density of about $4x10^6$ amperes per square centimeter and a temperature of about 175 degrees Celsius, the MTTF for Al-Cr is reported to be about 830 hours and that of Al-Ni is reported to be only about 300 hours.

In addition, many aluminum alloys do not etch similar to aluminum and require aggressive processing conditions that may attack other portions of the semiconductor device, such as silicon dioxide. Therefore, new process steps may need to be developed. Also, when the concentrations of some of the elements in the aluminum alloy become too high, the resistance of the conductive layer may be too high.

Summary of the Invention

The present invention includes a semiconductor device comprising a semiconductor substrate and a conductive layer overlying the substrate, wherein the conductive layer includes aluminum, nickel, and chromium.

Other features and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, and in which:

FIG. 1 includes a cross-sectional view of a portion of a semiconductor substrate including a transistor and field isolation regions.

FIG. 2 includes a cross-sectional view of the substrate of FIG. 1 after forming a first insulating layer and contact plugs.

FIG. 3 includes a cross-sectional view of the substrate of FIG. 2 after forming a first interconnecting member.

FIG. 4 includes a cross-sectional view of the substrate of FIG. 3 after forming a second insulating layer and via plugs.

FIG. 5 includes a cross-sectional view of the substrate of FIG. 4 after forming a second interconnecting member.

FIG. 6 includes a plot of cumulative failures versus time for aluminum-nickel-chromium, aluminum-silicon-copper, and aluminum-copper layers.

Detailed Description of Embodiments

An aluminum-nickel-copper (Al-Ni-Cr) alloy layer may be used as an interconnect or part of an interconnect. The Al-Ni-Cr alloy layer has a relatively low content of nickel and chromium. Therefore, the Al-Ni-Cr alloy layer may be deposited and etched similar to conventional aluminum-based layers that are also used for interconnects. The Al-Ni-Cr alloy layer has many benefits including resistance to electromigration and corrosion. The use and benefits of the Al-Ni-Cr alloy layer are better understood with the embodiments described below.

Device Including an Al-Ni-Cr Layer

FIG. 1 includes a cross-sectional view of a portion of a silicon substrate 10. Doped regions 11 act as source/drain regions and lie adjacent to the primary surface of the substrate 10. Adjacent to the doped regions 11 are field isolation regions 12. Between the doped regions is a channel region 16. A gate dielectric layer 13 overlies the channel region 16 and portions of the doped regions 11, and a gate electrode 14 overlies the gate dielectric layer 13. The gate electrode 14 typically includes a silicon containing material, such as amorphous silicon, polycrystalline silicon (polysilicon), and/or a refractory metal silicide. Spacers 15 overlie the doped regions 11 and lie adjacent to sides of the gate dielectric layer 13 and the gate electrode 14. Process steps used to form the device at this point in the process are conventional.

A first insulating layer 21 is formed over the substrate 10 as shown in FIG. 2. A first masking layer (not shown) is formed over the first insulating layer. The first insulating layer 21 is patterned to form contact openings to expose portions of one of the doped regions 11 and the gate electrode 14. The width of the openings are typically about 0.6 to 1.0 micron wide, although other widths may be used. Other contact openings (not shown) may be formed to other parts of the device. The first masking layer is removed after the contact openings are formed.

Contact plugs 22 are formed within the contact openings as shown in FIG. 2. A first barrier/glue layer 23 is deposited over the first insulating layer 21 and within the contact openings. The first barrier/glue layer 23 includes a titanium layer about 200 angstroms thick that acts as a glue layer and a titanium nitride (TiN) layer about 600 angstroms thick that acts as a barrier layer. A first tungsten layer 24 is blanket deposited to a thickness sufficient to fill the contact openings . Portions of the first barrier/glue and first tungsten layers 23 and 24 overlying the first insulating layer 21 are removed using a conventional etching step, thereby forming the contact plugs 22.

A first interconnecting member 31 is formed over the first insulating layer 21 as shown in FIG. 3. The first interconnecting member 31 is formed by sequentially sputter depositing four conductive layers and patterning those layers to form the first interconnecting member 31. The first two layers form a second barrier/glue layer 33 and is similar to the first barrier/glue layer 23 except that the TiN layer is about 400 angstroms thick. The third conductive layer 34 includes an aluminum-nickel-chromium (Al-Ni-Cr) alloy typically having about 0.1-0.5 weight percent nickel, about 0.02-0.1 weight percent chromium, and the balance aluminum. The third conductive layer 34 is about 6000 angstroms thick. In other embodiments, the TiN layer of the second barrier/glue layer 33 has a thickness between about 400-800 angstroms, and the third conductive layer 34 has a thickness typically between 1000-15,000 angstroms thick. The fourth conductive layer is a first antireflective coating 35 that is a TiN layer about 250 angstroms thick.

A second masking layer (not shown) is formed over the first antireflective coating 35. The layers 33-35 are etched during a single etch step to form the first interconnecting member 31. Other first interconnecting members (not shown) are also formed. The etching step is performed using at least one chlorine-containing gas, such as molecular chlorine (Cl_2), boron trichloride (BCl_3), and the like. Diluting gases, such as nitrogen, helium, and the like, may also be used. The width of the first

interconnecting members 31 may be about 0.9 micron wide. Typically, the width of the first interconnecting members 31 may be between about 0.5-1.5 micron wide. The length of the first interconnecting members 31 may be virtually any length, but is typically longer than the width. The second masking layer is then removed.

The first interconnecting member 31 is annealed at about 390 degrees Celsius for a time of about 30 minutes in an ambient including nitrogen and hydrogen. In other embodiments, the temperature may be between about 350-450 degrees Celsius, the time may be between 10-100 minutes, and the ambient may include only hydrogen, nitrogen, helium, or argon, or may include a combination those gases.

A second insulating layer 41, a via opening, and a via plug 42 are formed over the first insulating layer 21 and the first interconnecting member 31 as shown in FIG. 4. The via opening and via plug 42 are formed similar to the contact openings and contact plugs 22, respectively. The via plug 42 includes a third barrier/glue layer 43 and a second tungsten layer 44 that are similar to the first barrier/glue layer 23 and the first tungsten layer 24, respectively. Other via openings (not shown) and via plugs 42 (not shown) are also formed.

A second interconnecting member 51 is formed over the second insulating layer 41 and via plugs as shown in FIG. 5. The second interconnecting member 51 is formed similar to the first interconnecting member 31. The second interconnecting member includes four conductive layers. A fourth barrier/glue layer 53 includes a titanium and TiN layer similar to the second barrier/glue layer 33. The second interconnecting member 51 also includes an intermediate layer 54 of Al-Ni-Cr similar to the third conductive layer 34 and a second antireflective coating 55 made of a TiN layer similar to the first antireflective coating 35. The four conductive layers are etched to form the second interconnecting member 51 similar to the first interconnecting member 31. Other second interconnecting members (not shown) are also formed. The second interconnecting member 51 is

annealed similar to the first interconnecting member 31. A passivation layer 56 is formed over the second interconnecting member 51 as shown in FIG. 5 to form a substantially completed device. As used in this specification, the passivation layer is one or more layers formed over the uppermost interconnecting level. Therefore, no interconnecting layers are formed on the passivation layer.

In forming the semiconductor device, other electrical connections or additional layers may be required. One skilled in the art can determine whether other electrical connections or additional layers are needed.

Processing options are available in this embodiment. In one option, more than one etching step may be performed to form the first and second interconnecting members 31 and 51. In yet another option, the annealing step following the formation of the first interconnecting member 31 may be omitted if the annealing step following the formation of the second interconnecting member 51 is sufficient to anneal both the first and second interconnecting members 31 and 51. Also, the annealing step following the formation of the second interconnecting member 51 may be performed after the passivation layer 56 is formed rather that before the passivation layer 56 is formed. In another embodiment, the contact plugs 22 or the via plugs 42 do not have to be separately formed. For example, after forming the via openings, the four layers that form the second interconnecting member 51 are sputter deposited onto the second insulating layer 41 and within the via openings and etched to form the second interconnecting member 51. Therefore, the first and second interconnecting members 31 and 51 may contact each other.

Materials options also exist. Other semiconductor materials such as germanium and gallium arsenide may be used for the silicon substrate 10. Separate glue and barrier layers are not needed for the glue/barrier layers 23, 33, 43, and 53. A single layer may be used for one of the glue/barrier layers if the single layer adheres to insulating, silicon, and metal layers and helps to reduce adverse interactions between a metal-containing

layer and a silicon-containing layer. Refractory metals, such as tantalum, tungsten, cobalt, molybdenum, and the like and their silicides may be used as glue and/or barrier layers. The selection of proper materials for glue/barrier layers may be performed by those skilled in the art. The antireflective coatings may include silicon nitride, tungsten nitride, or the like.

Benefits of the Embodiments

Aluminum-silicon-copper (Al-Si-Cu), aluminum-copper (Al-Cu) and Al-Ni-Cr layers were compared to determine their times to failure. The Al-Si-Cu layer included about one weight percent silicon and one weight percent copper, the Al-Cu layer included about one weight percent copper, and the Al-Ni-Cr layer included about 0.2 weight percent nickel and about 0.04 weight percent chromium. The layers were patterned to with the same masking layer and tested with a current density of about $4x10^6$ amperes per square centimeter and an ambient temperature of about 200 degrees Celsius.

FIG. 6 includes a graph of the cumulative failures (%) versus time (hours) for the three layers. The MTTF for the Al-Si-Cu layer was about 295 hours, and the MTTF for the Al-Cu layer is about 990 hours. Unlike the Al-Si-Cu and Al-Cu layers, the Al-Ni-Cr layer did not have any failures even after 2200 hours. If the data obtained for Al-Ni-Cr layer is adjusted to 175 degrees Celsius, the MTTF would be no less than about 20,000 hours. Because no failures were seen with the Al-Ni-Cr layer after 2200 hours, the MTTF estimate of 20,000 hours may actually be low. In any event, the Al-Ni-Cr layer should have an MTTF of at least 2-20 times longer compared to the Al-Si-Cu, Al-Cu, Al-Ni, and Al-Cr layers. Although the MTTF measurement is pattern dependent, it is assumed that the pattern used for the Al-Ni and Al-Cr layers described in the background section have patterns similar to the Al-Ni-Cr layer.

The Al-Ni-Cr layer allows it to be used as an interconnect because of its resistivity is similar to other aluminum alloys. The Al-Ni-Cr layer resistivity of about 3.15 microohms·cm, the

Al-Cu layer has a resistivity of about 3.1 microohms·cm, and the Al-Si-Cu layer has a resistivity of about 3.35 microohms·cm. If the nickel or chromium concentrations are greater than 0.5 weight percent, the resistivity of the Al-Ni-Cr layer with that nickel and chromium content may be too high. If resistivity is less of a concern, even higher concentrations of nickel and chromium may be used. If the concentration of the nickel and chromium are too high, such as about 3 weight percent each, then the Al-Ni-Cr layer may not etch similar to aluminum. Therefore, each of the nickel and chromium concentration should not be higher than about 0.5 weight percent.

Al-Cu and Al-Ni-Cr layers were etched using a chlorine-containing plasma. Corrosion was evident with the Al-Cu layer while no evidence of corrosion was found on the Al-Ni-Cr layer. The Al-Ni-Cr layer is expected to be more corrosion resistant compared to Al-Si-Cu, Al-Cu, and Al-Ni. Copper should not be included in the Al-Ni-Cr layer because copper may enhance its corrosion.

Another benefit is the simplicity in which Al-Ni-Cr may be incorporated into an existing process sequence. Depositing and etching the Al-Ni-Cr is expected to be similar to depositing and etching the Al-Si or Al-Si-Cu layers previously described. Other than possibly the parameters previously described above, virtually all other parameters for depositing and etching are expected to be virtually the same for Al-Ni-Cr, Al-Si, and Al-Si-Cu. The reason why the Al-Ni-Cr layer is expected to deposit and etch similar to Al-Si and Al-Si-Cu is because the nickel and chromium concentrations are low (no greater than about 0.5 and 0.1 weight percent, respectively).

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. However, it will be evident that various modifications and changes can be made thereto without departing from the broader spirit or scope of the invention as set forth in the appended claims. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

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Claims

What is claimed is:

1. A semiconductor device comprising an interconnecting member (31, 51) overlying a semiconductor substrate (10) and a passivation layer (56) overlying the interconnecting member (31, 51), wherein the interconnecting member (31, 51) is characterized such that:
   the interconnecting member (31, 51) includes a conductive layer (34, 54);
   the conductive layer (34, 54) extends along all of the interconnecting member (31, 51) and includes an alloy; and
   the alloy includes aluminum, nickel, and chromium, but no silicon.

2. The semiconductor device of claim 1, characterized such that the conductive layer (34, 54) includes at least 99 weight percent aluminum, between about 0.2-0.5 weight percent nickel, and between about 0.02-0.1 weight percent chromium.

3. The semiconductor device of claim 1, further characterized by:
   a glue layer (33, 53) underlying the conductive layer
   a barrier layer (33, 53) lying between the glue (33, 53) and conductive layers (34, 54); and
   an antireflective coating (35, 55) overlying the conductive layer (34, 54).

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4. A semiconductor device comprising: a conductor (11, 14, 23, 24, 31, 43, 44) within or overlying a semiconductor substrate (10); an insulating layer (21, 41) overlying the conductor (11, 14, 23, 24, 31, 43, 44) and including an opening, wherein at least a portion of the conductor (11, 14, 23, 24, 31, 43, 44) underlies the opening; an interconnecting member (31, 51) overlying the insulating layer (21, 41) and electrically connected to the conductor (11, 14, 23, 24, 31, 43, 44); and a passivation layer (56) overlying the interconnecting member (31, 51), wherein the interconnect member (31, 51) is characterized such that:
the interconnecting member (31, 51) includes a conductive layer (34, 54) ;
the conductive layer (34, 54) extends along all of the interconnecting member (31, 51) and includes an alloy; and
the alloy includes at least 99 weight percent aluminum, about 0.1-0.5 weight percent nickel, and about 0.02-0.1 weight percent chromium, but no silicon; and
a portion of the conductive layer (34, 54) overlies the insulating layer (21, 41) and another portion of the conductive layer (34, 54) overlies the opening of the insulating layer (21, 41) or lies within the opening of the insulating layer (21, 41).

5. The semiconductor device of claim 4, further characterized by:
a glue layer (33, 53) underlying the conductive layer
a barrier layer (33, 53) lying between the glue (33, 53) and conductive layers (34, 54); and
an antireflective coating (35, 55) overlying the conductive layer (34, 54).

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6. A semiconductor device comprising a conductor that is a doped region lying within the semiconductor substrate (11), a gate electrode overlying the substrate (14), a silicon-containing electrode (14) overlying the substrate (11), or a metal-containing member (23, 24, 31, 43, 44) overlying the substrate (11); an insulating layer (21, 41) overlying the conductor (11, 14, 23, 24, 31, 43, 44) and including an opening, wherein at least a portion of the conductor (11, 14, 23, 24, 31, 43, 44) underlies the opening; a plug (23, 24, 43, 44) within the opening, wherein the plug is a contact plug (23, 24) or a via plug (43, 44); an interconnecting member (31, 51), wherein a portion of the interconnecting member (31, 51) overlies the insulating layer (21, 41) and another portion of the interconnecting member (31, 51) overlies the plug (23, 24, 43, 44); and a passivation layer (56) overlying the interconnecting member (31, 51), wherein the interconnecting member (31, 51) is characterized such that:

the interconnecting member (31, 51) includes a conductive layer (33, 53) that extends along all of the interconnecting member (31, 51); and

the conductive layer (33, 53) is an alloy that consists of aluminum, nickel, and chromium and has at least 99 weight percent aluminum, 0.1-0.5 weight percent nickel, and 0.02-0.1 weight percent chromium; and

the interconnecting member (31, 51) is electrically connected to the conductor (11, 14, 23, 24, 31, 43, 44).

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SEMICONDUCTOR DEVICE

Abstract of the Disclosure

An aluminum-nickel-chromium (Al-Ni-Cr) layer (34) is used as an interconnect (31) within a semiconductor device. The Al-Ni-Cr layer (34) has about 0.1-0.5 weight percent nickel and about 0.02-0.1 weight percent chromium. Usually, the nickel or chromium concentrations are no greater than 0.5 weight percent. The layer (34) is resistant to electromigration and corrosion. The low nickel and chromium concentrations allow the layer (34) to be deposited and patterned similar to most aluminum-based layers.

FIG. 3 accompanies this abstract.

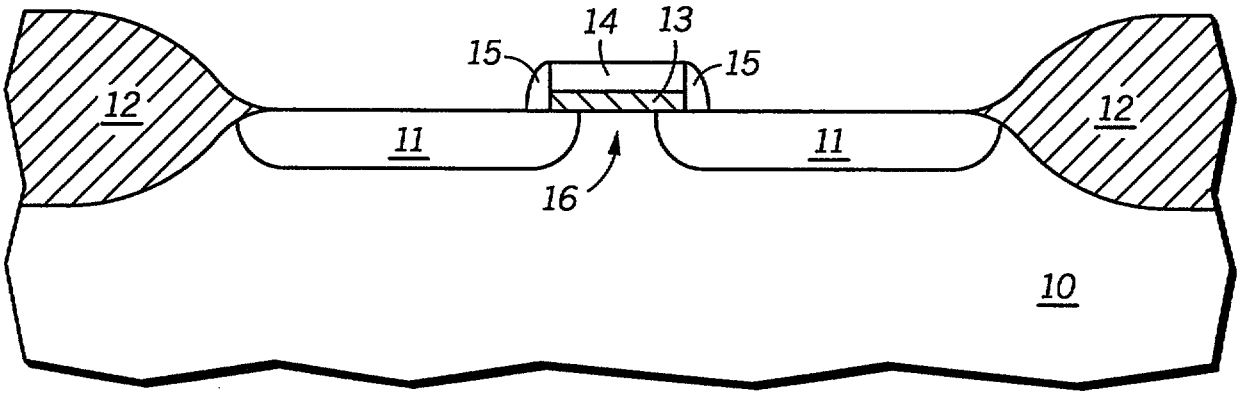


FIG.1

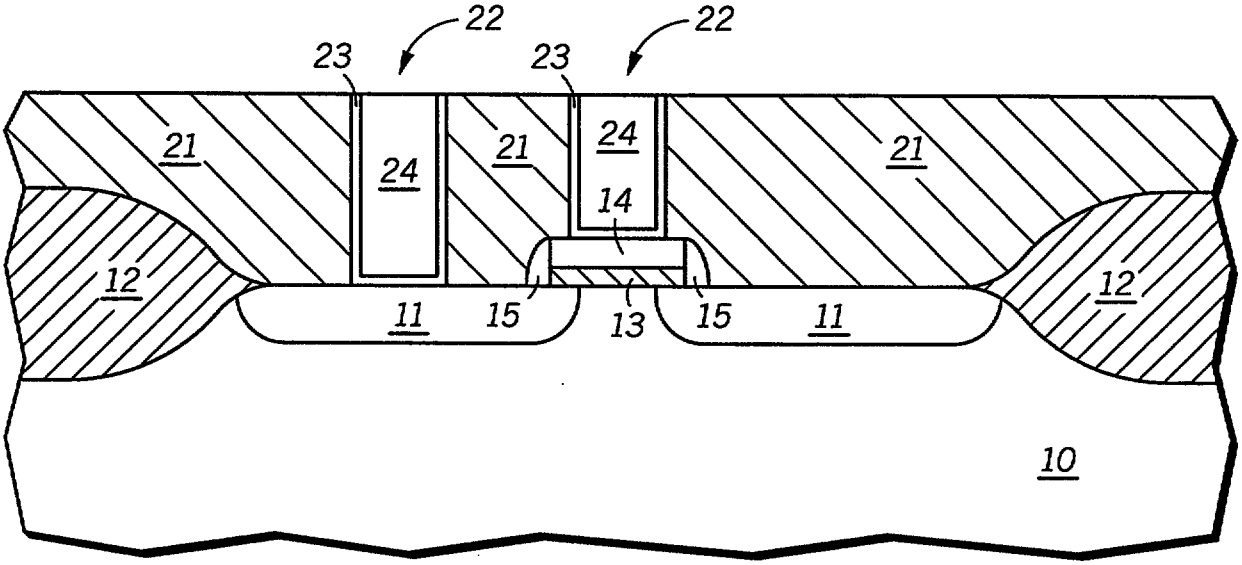


FIG.2

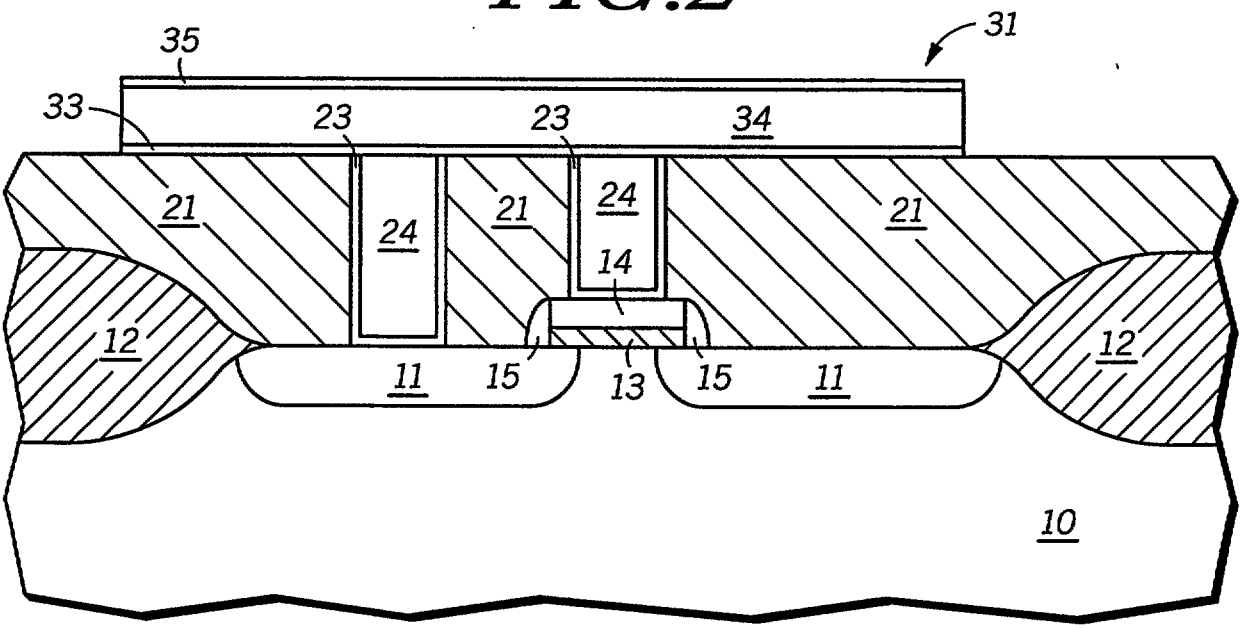


FIG.3

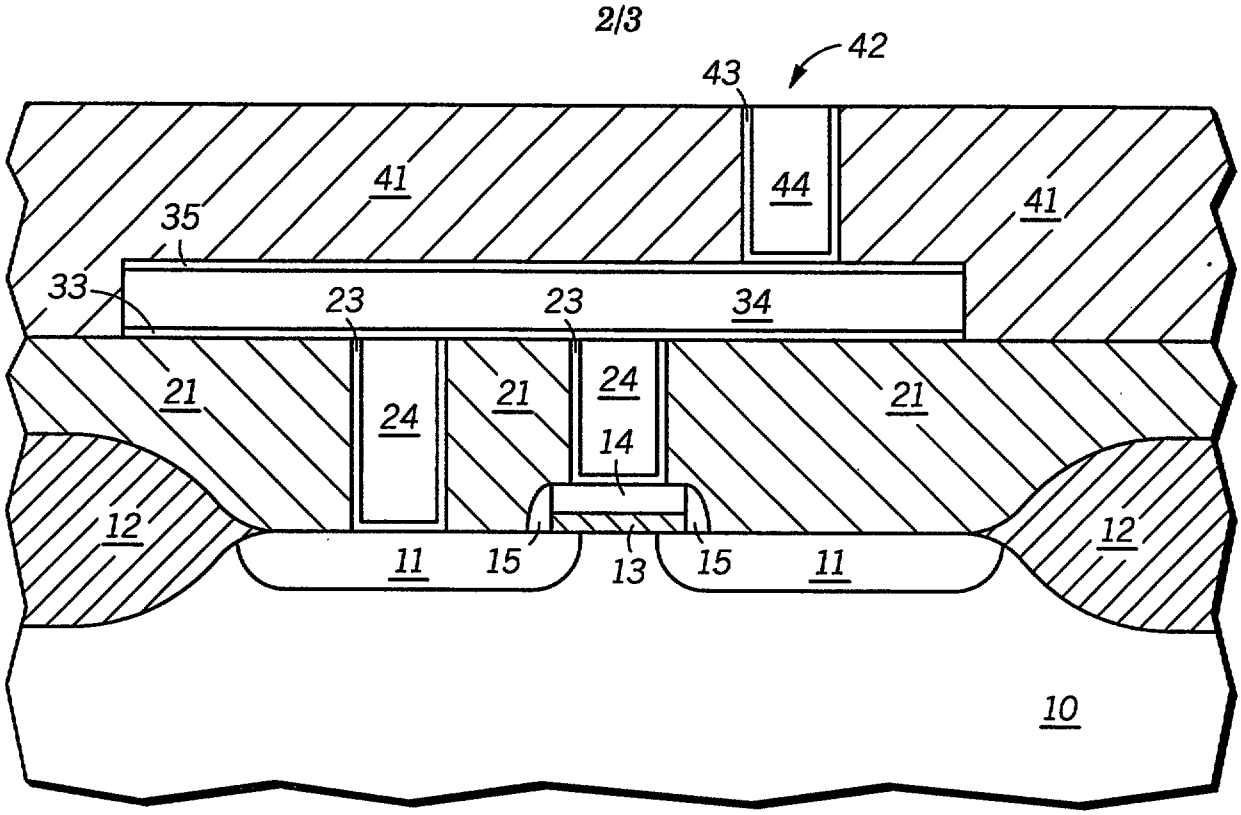

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FIG.4

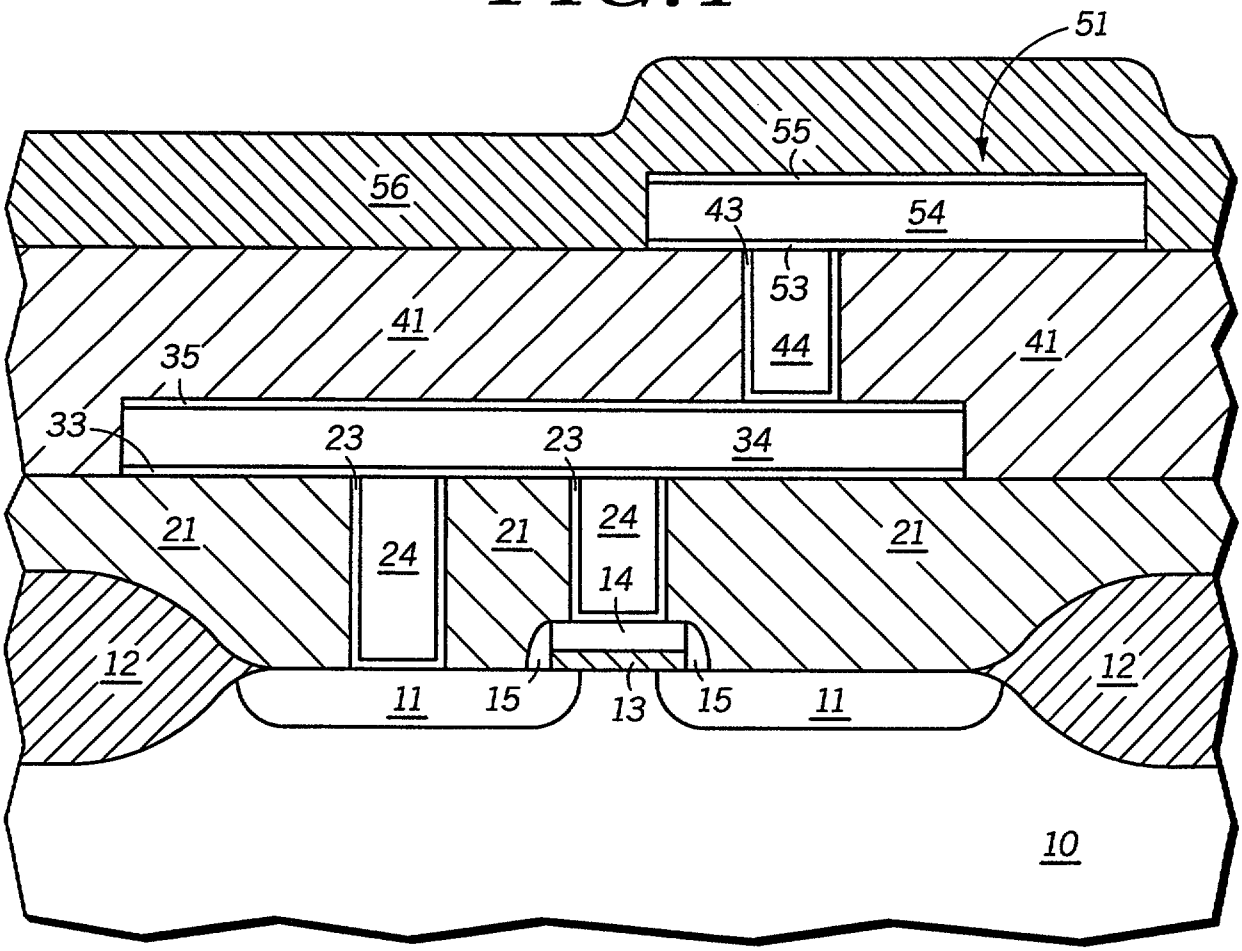

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FIG.5

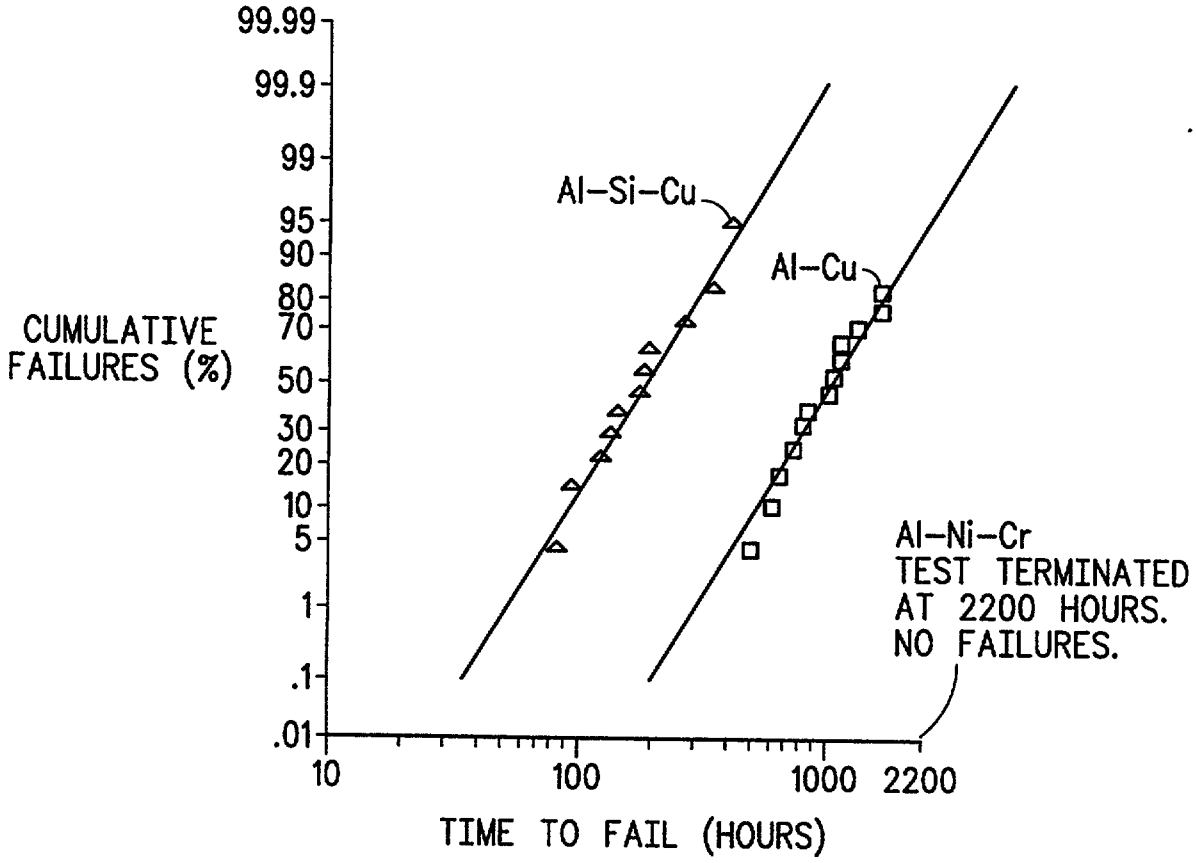

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10
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CUMULATIVE FAILURES (%)
Al–Si–Cu
Al–Cu
Al–Ni–Cr
TEST TERMINATED
AT 2200 HOURS.
NO FAILURES.
10
100
1000
2200
TIME TO FAIL (HOURS)

FIG.6

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Claims

1. A semiconductor device comprising:
   a substrate;
   an interconnecting member overlying the substrate, wherein:
      the interconnecting member includes a conductive layer;
      the conductive layer includes an alloy;
      the alloy includes aluminum, nickel, and chromium, but no silicon; and
      the conductive layer extends along all the interconnecting member; and
   a passivation layer overlying the interconnecting member.

2. A process for forming a semiconductor device comprising the steps of:
   depositing a conductive layer over a substrate, wherein:
      the conductive layer includes an alloy; and
      the alloy includes aluminum, nickel, and chromium, but no silicon; and
   patterning the conductive layer to form an interconnecting member,
      wherein the conductive layer extends along all the interconnecting member; and
   forming a passivation layer overlying the interconnecting member.

3. The semiconductor device of claim 1 or the process of claim 2, wherein the conductive layer includes at least 95 weight percent aluminum, no more than 0.5 weight percent nickel, and no more than 0.5 weight percent chromium.

4. The semiconductor device of claim 1 or the process of claim 2, wherein the conductive layer includes at least 99 weight percent aluminum, between about 0.1-0.5 weight percent nickel, and between about 0.02-0.1 weight percent chromium.

5. The semiconductor device of claim 1 or the process of claim 2, wherein the alloy consists of aluminum, nickel, and chromium.

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6. The semiconductor device of claim 1 or the process of claim 2, wherein the interconnecting member further comprises:
a barrier layer underlying at least a portion of the conductive layer; and
an antireflective coating overlying at least a portion of the conductive layer.

7. The semiconductor device or process of claim 6, wherein the interconnecting member further comprises a glue layer underlying the barrier layer.

8. The semiconductor device or process of claim 7, wherein:
the glue layer includes titanium;
the barrier layer includes titanium nitride; and
the antireflective coating includes titanium nitride.

9. The semiconductor device of claim 1, 3, 4, 5, 6, 7, or 8, further comprising:
a conductor selected from a group of a doped region lying within a semiconductor substrate, a gate electrode overlying the substrate, a silicon-containing electrode overlying the substrate, and a metal-containing member overlying the substrate;
an insulating layer overlying the conductor and including an opening, wherein at least a portion of the conductor is exposed beneath the opening;
a conductive plug within the opening, wherein the conductive plug electrically connects the conductor to the interconnecting member.

10. The process of claim 2, 3, 4, 5, 6, 7, or 8, further comprising steps of:
forming a conductor selected from a group of a doped region lying within a semiconductor substrate, a gate electrode overlying the substrate, a silicon-containing electrode overlying the substrate, and a metal-containing member overlying the substrate;
forming an insulating layer overlying the conductor;

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patterning the insulating layer to form an opening that exposes at least a portion of the conductor; and

forming a conductive plug within the opening before the step of depositing the conductive layer.

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Claims

1. A semiconductor device comprising:
   a substrate;
   an interconnecting member overlying the substrate, wherein:
      the interconnecting member includes a conductive layer;
      the conductive layer includes an alloy;
      the alloy includes aluminum, nickel, and chromium, but no silicon; and
      the conductive layer extends along all the interconnecting member; and
   a passivation layer overlying the interconnecting member.

2. The semiconductor device of claim 1, wherein the conductive layer includes at least 95 weight percent aluminum, no more than 0.5 weight percent nickel, and no more than 0.5 weight percent chromium.

3. The semiconductor device of claim 1, wherein the conductive layer includes at least 99 weight percent aluminum, between about 0.1-0.5 weight percent nickel, and between about 0.02-0.1 weight percent chromium.

4. The semiconductor device of claim 1, wherein the alloy consists of aluminium, nickel, and chromium.

5. The semiconductor device of claim 1, wherein the interconnecting member further comprises:
   a barrier layer underlying at least a portion of the conductive layer; and
   an antireflective coating overlying at least a portion of the conductive layer.

6. The semiconductor device of claim 5, wherein the interconnecting member further comprises a glue layer underlying the barrier layer.

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7. The semiconductor device of claim 6, wherein:
the glue layer includes titanium;
the barrier layer includes titanium nitride; and
the antireflective coating includes titanium nitride.

8. The semiconductor device of any preceding claim, further comprising:
a conductor selected from a group of a doped region lying within a semiconductor substrate, a gate electrode overlying the substrate, a silicon-containing electrode overlying the substrate, and a metal-containing member overlying the substrate;
an insulating layer overlying the conductor and including an opening, wherein at least a portion of the conductor is exposed beneath the opening;
a conductive plug within the opening, wherein the conductive plug electrically connects the conductor to the interconnecting member.

9. A process for forming a semiconductor device according to any preceding claim, the process comprising the steps of:
depositing the conductive layer over the substrate;
patterning the conductive layer to form the interconnecting member; and
forming the passivation layer overlying the interconnecting member.

10. The process of claim 9, further comprising steps of:
forming a conductor selected from a group of a doped region lying within a semiconductor substrate, a gate electrode overlying the substrate, a silicon-containing electrode overlying the substrate, and a metal-containing member overlying the substrate;
forming an insulating layer overlying the conductor;
patterning the insulating layer to form an opening that exposes at least a portion of the conductor; and

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forming a conductive plug within the opening before the step of depositing the conductive layer.