

ABSTRACT OF THE DISCLOSURE

The present disclosure relates to a semiconductor memory device. The semiconductor memory device includes memory cell array, error correction code (ECC) engine, refresh control circuit and control logic circuit. The memory cell array includes memory cell rows. The refresh control circuit performs a refresh operation on the memory cell rows. The control logic circuit controls the ECC engine such that the ECC engine generates an error generation signal by performing ECC decoding on sub-pages in at least one first memory cell row during a read operation. The control logic circuit compares an error occurrence count of the first memory cell row with a threshold value and provides the refresh control circuit with a first address of the first memory cell row as an error address based on the comparison. The refresh control circuit increases a number of refresh operations performed in the first memory cell row during a refresh period.

FIG. 2