

CLAIMS

1. A memory device, comprising:

a lower conductive line extending in a first direction, the lower conductive line comprising alternating layers of at least a first material and at least a second material;

an upper conductive line extending in a second direction and crossing the lower conductive line, the upper conductive line comprising alternating layers of at least a third material and at least a fourth material;

wherein at least one of the alternating layers of the upper and lower conductive lines comprises tungsten and carbon; and

a memory cell stack interposed at an intersection between the upper and lower conductive lines, the memory cell stack including:

a first active element over the lower conductive line and a second active element over the first active element, wherein one of the first and second active elements comprises a storage element and the other of the first and second active elements comprises a selector element;

a first electrode interposed between the first active element and the lower conductive line; and

a second electrode interposed between the second active element and the upper conductive line.

2. The memory device of Claim 1, wherein the memory device is a phase change memory device, and wherein the first active element is a storage element comprising a first chalcogenide composition and the second active element is a selector element comprising a second chalcogenide composition.

3. The memory device of Claim 1, wherein the at least one of the upper and lower conductive lines is at least partially amorphous.

4. The memory device of Claim 1, wherein the at least one of the upper and lower conductive lines comprises between about 0.5% and about 20% of carbon by atomic percentage.

5. The memory device of Claim 1, wherein the at least one of the upper and lower conductive

lines has a surface roughness having a root mean square value less than about 2.5% of a thickness of the at least one of upper and lower conductive lines.

6. The memory device of Claim 5, wherein the thickness of the at least one of the upper and lower conductive lines is less than or equal to about 100 nm, and wherein a width of the at least one of the upper and lower conductive lines is less than or equal to about 50 nm.

7. The memory device of Claim 1, wherein the at least one of the upper and lower conductive lines comprises a stack of alternating layers comprising at least one metal line and at least one alloy line comprising tungsten and carbon.

8. The memory device of Claim 7, wherein the at least one alloy line is at least partially amorphous.

9. A memory device, comprising:

a lower conductive line extending in a first direction, the lower conductive line comprising alternating layers of at least a first material and at least a second material;

an upper conductive line extending in a second direction and crossing the lower conductive line, the upper conductive line comprising alternating layers of at least a third material and at least a fourth material; and

a phase change memory cell formed at an intersection between the upper and lower conductive lines, the phase change memory cell including an active element comprising a chalcogenide material,

wherein at least one of the first material, the second material, the third material, or the fourth material comprises a metallic conductive line; and

wherein at least one of the first material, the second material, the third material, or the fourth material comprises a conductive carbon-containing line, and wherein the conductive carbon-containing line has an electrical resistivity in a direction of line extension that is lower than an electrical resistivity of amorphous carbon.

10. The memory device of Claim 9, wherein a layer comprising the conductive carbon-containing line comprises graphene.

11. The memory device of Claim 10, wherein the layer comprising the conductive carbon-containing line comprises less than 20 monolayers of graphene.
12. The memory device of Claim 10, wherein the layer comprising the conductive carbon-containing line has a thickness between about 1 nm and about 10 nm, and wherein a width of the at least one of the upper and lower conductive lines is less than or equal to about 50 nm.
13. The memory device of Claim 9, wherein a layer comprising the metallic conductive line comprises tungsten.
14. The memory device of Claim 9, wherein thicknesses of the carbon-containing lines are between about 0.5 nm and about 3 nm, and wherein a width of the at least one of the upper and lower conductive lines is less than or equal to about 50 nm.
15. The memory device of Claim 9, wherein an aspect ratio of the at least one of upper and lower conductive lines is less than about one.
16. The memory device of Claim 9, wherein the phase change memory cell comprises an electrode contacting the at least one of the upper and lower conductive lines.
17. A memory device, comprising:
 a lower conductive line extending in a first direction;
 an upper conductive line extending in a second direction and crossing the lower conductive line; and
 a variable resistance memory cell formed at an intersection between the upper and lower conductive lines,
 wherein at least one of the upper and lower conductive lines comprises:
 grains comprising at least one of alpha or beta phase tungsten; and
 a matrix having a carbon content greater than a carbon content of the grains.
18. The memory device of Claim 17, wherein the at least one of the upper and lower conductive lines is at least partially amorphous.

19. The memory device of Claim 18, wherein the matrix is at least partially amorphous.

20. A method of fabricating a memory device, comprising:

providing a substrate;

forming a lower conductive line extending in a first direction by forming and patterning a lower conductive material over the substrate, the lower conductive line comprising alternating layers of at least a first material and at least a second material;

forming a memory cell stack on the lower conductive line by forming and patterning a memory cell material stack, wherein the memory cell material stack includes a first active material and a second active material over the first active material, wherein one of the first and second active materials comprises a storage material and the other of the first and second active materials comprises a selector material; and

forming an upper conductive line extending in a second direction by forming and patterning an upper conductive material over the lower conductive line, the upper conductive line comprising alternating layers of at least a third material and at least a fourth material;

wherein at least one of the alternating layers of the upper and lower conductive lines comprises tungsten and carbon, and

wherein forming the memory cell stack includes forming a first electrode interposed between the first active element and the lower conductive line and forming a second electrode interposed between the second active element and the upper conductive line.

21. The method of Claim 20, wherein forming the memory cell material stack comprises forming the first active material comprising a first chalcogenide composition and forming the second active material comprising a second chalcogenide composition.

22. The method of Claim 20, wherein at least one of forming the lower conductive line and forming the upper conductive line comprises forming a conductive material that is at least partially amorphous.

23. The method of Claim 20, wherein the at least one of the upper and lower conductive lines comprises between about 1% and about 20% of carbon by atomic percentage.

24. The method of Claim 22, wherein forming the conductive material that is at least partially

amorphous comprises:

- precipitating grains comprising at least one of alpha or beta phase tungsten; and
- forming a matrix having a carbon content greater than a carbon content of the grains.

25. The method of Claim 20, wherein forming the lower conductive material comprises forming the lower conductive material having surface roughness having a root mean square value between about 2.5% and about 7.5% of a thickness of the lower conductive material.

26. The method of Claim 20, wherein at least one of forming the lower conductive line or forming the upper conductive line comprises forming a stack comprising at least one metal line and at least one alloy line comprising tungsten and carbon.

27. The method of Claim 20, wherein forming the memory cell stack comprises patterning a memory cell line stack and the lower conductive line extending in the first direction using a single mask.

28. The method of Claim 27, wherein forming the memory cell stack further comprises, after patterning the memory cell line stack, separating the first and second active materials of the memory cell line stack in the second direction, wherein separating the memory cell line stack and forming the upper conductive line are performed using a single mask.

29. The method of Claim 22, wherein forming the at least one of upper and lower conductive lines comprises depositing using physical vapor deposition.

30. The method of Claim 31, wherein depositing using physical vapor deposition comprises co-sputtering a first target comprising tungsten and a second target comprising carbon.

31. A method of fabricating a memory device, comprising;

- providing a substrate;

- forming a lower conductive line extending in a first direction by forming and patterning a lower conductive material over the substrate, the lower conductive line comprising alternating layers of at least a first material and at least a second material;

- forming an upper conductive line extending in a second direction by forming and

patterning an upper conductive material over the lower conductive line, the upper conductive line comprising alternating layers of at least a third material and at least a fourth material; and

forming a phase change memory cell, between and at an intersection of the lower conductive line and the upper conductive line, the phase change memory cell comprising a selector element and a storage element, wherein the lower conductive line and at least one of the selector element and the storage element is patterned in the first direction using a single mask process, and the upper conductive line and the at least one of the selector element and the storage element is patterned in the second direction using a single mask process, such that the at least one of the selector material and the storage material is isolated, in both first and second directions after forming the phase change memory cell,

wherein at least one of the first material, the second material, the third material, or the fourth material comprises a metallic conductive line; and

wherein at least one of the first material, the second material, the third material, or the fourth material comprises a conductive carbon containing line, and wherein the conductive carbon-containing line has an electrical resistivity in a direction of line extension that is lower than an electrical resistivity of amorphous carbon.

32. The method of Claim 31, wherein forming the at least one of lower and upper conductive lines comprising depositing graphene.

33. A method of fabricating a memory device, comprising:

providing a substrate;

forming a lower conductive line extending in a first direction by forming and patterning a lower conductive material over the substrate;

forming a variable resistance memory cell comprising a storage element and a selector element; and

forming an upper conductive line extending in a second direction by forming and patterning an upper conductive material over the lower conductive line,

wherein at least one of forming the upper conductive line and forming the lower conductive line comprises:

forming grains comprising at least one of alpha or beta phase tungsten; and

forming a matrix having a carbon content greater than a carbon content of the grains.

34. The method of Claim 33, wherein at least one of forming the upper conductive line and forming the lower conductive line comprises forming a conductive material that is at least partially amorphous.