

## [ABSTRACT]

An information processing device (1) includes: a decoding circuit (12b),  
provided on a data bus (DB) for connecting a main memory (101) and an external storage  
device (11), which is capable of switching between enabling and disabling a process for  
5 decoding information that is transmitted through the data bus (DB); and a CPU (100) that  
is configured to read out information written in the external storage device (11) into the  
main memory (101). The CPU (100) is configured to enable the decoding process of  
the decoding circuit 12b in a case where a snapshot image of the main memory 101 is  
read out as the information written in the external storage device (11).