

Abstract

To propose a non-volatile semiconductor memory device capable of suppressing occurrence of disturbance more greatly than in a conventional technique while achieving miniaturization. A plurality of word lines are formed in a matrix in the non-volatile semiconductor memory device, power supply units are respectively provided for word line columns (memory wells), a different unit voltage is applied for each of power supply units depending on whether or not a selected memory cell exists in the word line column, a switching mechanism in each of the power supply units is switched by the word line depending on a value of a voltage on a control line, a charge storage gate voltage or a charge storage inhibition gate voltage is individually applied for each of the word lines so that the charge storage inhibition gate voltage value and a bit line voltage value can be freely set for each of the word line columns to values at which occurrence of disturbance can be suppressed. A plurality of power supply units are connected to the control line in a common row direction, and a row-direction address decoder, which is independent for each of the word line columns is not required so that the non-volatile semiconductor memory device can be miniaturized.