WHAT IS CLAIMED:

1. A method of operating a memory device that comprises a memory block operatively connected to a common source line and a plurality of bit lines, wherein the memory block includes first and second sub-blocks each having a respective position in the memory block relative to the common source line and the plurality of bit lines, the method comprising:

receiving a command and an address from outside the memory device, and

performing a precharge operation on the memory block in response to the command, using a first precharge path through the memory block or a second precharge path through the memory block based on the respective position of the first or second sub-block that includes a word line that is configured to activate responsive to the address,

wherein the first precharge path is through the plurality of bit lines and the second precharge path is through the common source line.

2. The method of claim 1, wherein the first and second sub-blocks are each configured to perform a respective partial erase operation.

3. The method of claim 1, wherein the memory block further comprises:

a plurality of string select transistors configured to control connection of the plurality of bit lines to a plurality of strings of memory cells in the memory block responsive to a plurality of string select lines; and

a plurality of ground select transistors configured to control connection of the common source line to the plurality of strings of memory cells responsive to a plurality of ground select lines, wherein the first sub-block is adjacent to the plurality of string select lines and the second sub-block is adjacent to the plurality of ground select lines;

performing the precharge operation via the first precharge path when the word line that is configured to activate responsive to the address is in the first sub-block.

4. The method of claim 3, wherein performing of the precharge operation includes:

disabling the plurality of ground select transistors;

enabling the plurality of string select transistors; and

applying a precharge voltage to the plurality of bit lines.

5. The method of claim 3, wherein performing of the precharge operation includes:

performing the precharge operation via the second precharge path when the word line that is configured to activate responsive to the address is in the second sub-block.

6. The method of claim 5, wherein performing of the precharge operation further includes:

disabling the plurality of string select transistors;

enabling the plurality of ground select transistors; and

applying a precharge voltage to the common source line.

7. The method of claim 1, wherein performing the precharge operation further comprises:

identifying whether the first sub-block or the second sub-block that includes the word line configured to activate responsive to the address is included in a first block group that is adjacent to a plurality of string select transistors configured to control connection of the plurality of bit lines to the memory block or is included in a second block group that is adjacent to a plurality of ground select transistors configured to control connection of the common source line to the memory block to provide an identification result; and

performing the precharge operation via the first precharge path or via the second precharge path based on the identification result.

8. The method of claim 7, wherein performing the precharge operation further comprises:

performing the precharge operation via the first precharge path when the identification result indicates that the word line configured to activate responsive to the address is in the first block group; and

performing the precharge operation via the second precharge path when the identification result indicates that the word line configured to activate responsive to the address is in the second block group.

9. The method of claim 1, wherein performing the precharge operation further comprises:

defining a reference word line included in the memory block to provide a reference sub-block to indicate which sub-blocks included in the memory block are adjacent to a plurality of string select transistors;

determining whether the word line configured to activate responsive to the address is included in a sub-block that is adjacent to the plurality of string select transistors that are configured to connect the plurality of bit lines to the memory block or is adjacent to a plurality of ground select transistors that are configured to connect a plurality of ground select lines to the memory block to provide an identification result; and

performing the precharge operation via the first precharge path or via the second precharge path based on the identification result.

10. The method of claim 9, wherein the memory block further comprises:

a plurality of dummy memory cells connected to the reference word line.

11. A method of operating a memory device including a memory block having at least two sub-blocks, the memory block connected to a plurality of ground select lines configured to control coupling to a common source line and connected to a plurality of string select lines configured to control coupling to a plurality of bit lines, the method comprising:

receiving a program command from outside the memory device;

determining if a plurality of selected word lines configured to activate memory cells responsive to the program command are included a first sub-block or are included in a second sub-block to provide a selected program sub-block;

performing a program operation using a first sequence of a plurality of first selected word lines extending in a first direction from the plurality of ground select lines toward the plurality of string select lines responsive to determining that the plurality of selected word lines are included in the first sub-block; and

performing the program operation using a second sequence of a plurality of second selected word lines extending in a second direction from the plurality of string select lines toward the plurality of ground select lines responsive to determining that the plurality of selected word lines are included in the second sub-block, and

performing a precharge operation associated with the program operation using a first

precharge path or a second precharge path determined based on a position of a selected precharge sub-block connected to the plurality of selected word lines, wherein the first precharge path is through the plurality of bit lines and the second precharge path is through the common source line.

12. The method of claim 11, wherein the selected program sub-block is adjacent to the plurality of string select lines, wherein performing the program operation comprises performing the program operation using the first sequence of the plurality of first selected word lines in the first direction.

13. The method of claim 11, wherein the selected program sub-block is adjacent to the plurality of ground select lines, wherein performing the program operation comprises performing the program operation using the second sequence of the plurality of second selected word lines in the second direction.

14. The method of claim 11, further comprising:

performing the precharge operation via the first precharge path when the selected precharge sub-block connected to the plurality of selected word lines is adjacent to the plurality of string select lines; and

performing the precharge operation via the second precharge path when the selected precharge sub-block connected to the plurality of selected word lines is adjacent to the plurality of ground select lines.

15. The method of claim 11, wherein a number of data bits programmed in a memory cell included in the first sub-block is identical to or different from a number of data bits in a memory cell included in the second sub-block.

16. A memory system including:

a memory device including a memory block having at least two sub-blocks, each of the at least two sub-blocks including a plurality of memory cells, and the at least two sub-blocks connected to a plurality of ground select lines configured to control connection to a common source line and the at least two sub-blocks connected to a plurality of string select lines configured to control connection to a plurality of bit lines; and

a memory controller configured to select one of a first precharge operation through the plurality of bit lines and a second precharge operation through the common source line based on a position of a sub-block connected to at least one select word line subject to a program operation or a read operation performed on the memory block to control the selected precharge operation.

17. The memory system of claim 16, wherein the memory controller is configured to control a partial erase operation on the memory block at a sub-block level.

18. The memory system of claim 16, wherein

the memory controller is configured to control the program operation on a plurality of selected word lines in an order of selected word lines in a first direction extending from the plurality of ground select lines toward the plurality of string select lines and in a second direction extending from the plurality of string select lines toward the plurality of ground select lines.

19. The memory system of claim 18, wherein when the first precharge operation is performed the memory controller is configured to carry out the program operation on selected word lines in an order in the first direction, and

when the second precharge operation is performed the memory controller is configure to carry out the program operation selected word lines in an order the second direction.