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(54) Title: APPARATUS AND METHOD FOR MEMORY STORAGE CELL LEAKAGE CANCELLATION SCHEME

(57) Abstract: An apparatus is described having a plurality of storage cells coupled between a first bit line and a second bit line. The apparatus also has a first transistor that pre-charges the first bit line and provides a first supply of current for one or more leakage currents drawn from the first bit line by any of the plurality of storage cells. The apparatus also has a second transistor that pre-charges the second bit line and provides a second supply of current for one or more leakage currents drawn from the second bit line by any of the plurality of storage cells.



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