

Description

Method for forming metallic conductor patterns on electrically insulating substrates.

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US-A-4 804 615 discloses a method for forming metallic conductor patterns with solderable connection regions, in which the starting point is an electrically insulating, flat substrate laminated with copper on both sides. After through-contact holes have been drilled, a copper layer, which also extends over the walls of the hole, is deposited in a chemical deposition bath. An electrolytic resist is then applied to this copper layer and covers everything except the subsequent connection regions, so that copper and a tin/lead alloy can be deposited here electrolytically one after another. The tin/lead alloy forms a final surface of the connection regions which can be soldered. After the complete removal of the electrolytic resist, an etch resist is applied and, with the exception of the connection regions, covers all the regions of the subsequent conductor pattern. After this, all those regions of the chemically deposited copper layer which do not correspond to the conductor pattern, and of the copper lamination, are etched away down to the surface of the substrate. During this etching process, it is not only the actual etch resist but also the etch-resistant final surface of the connection regions which protect the copper located beneath them from etching attack. After the complete removal of the etch resist, a solder-stop lacquer is then applied, which covers everything except those connection regions of the conductor pattern which can be soldered.

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US-A-4 608 274 discloses a further method for forming metallic conductor patterns with connection regions which can be soldered, in which the starting point is a pre-drilled, electrically insulating, flat

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substrate. After the non-electrolytic deposition of copper to both sides of the substrate and in the holes, an etch resist is applied to the copper layer,

and, with the exception of the subsequent connection regions, covers all the regions of the subsequent conductor pattern. An electrolytic resist is then applied, and covers everything except the subsequent
5 connection regions, so that copper and a tin/lead alloy can be deposited electrolytically here one after another. Following the complete removal of the electrolytic resist, all the regions of the exposed copper layer are etched away, down to the surface of
10 the substrate; in the region of the conductor pattern, the etch resist and the etch-resistant final surface of the connection regions protect the copper layer located beneath them from etching attack. Following the complete removal of the etch resist, a solder-stop
15 lacquer is also applied again, and covers everything except the connection regions of the conductor pattern which can be soldered.

WO 95/29573 discloses a further method for forming metallic conductor patterns having connection
20 regions that can be soldered and/or bonded on electrically insulating substrates. This method comprises the following method steps:

- a.) Applying a metalization to the substrate;
- b.) Applying an organic, electrolysis-resistant and
25 etch-resistant protective layer to the metalization in an electrolytic dip-coating bath;
- c.) Removing the protective layer in the subsequent connection regions by means of laser radiation;
- d.) Electrolytically depositing an etch-resistant
30 final surface which can be soldered and/or bonded onto those regions of the metalization exposed in method step c);
- e.) Removing the protective layer, at least in the regions directly adjacent to the subsequent
35 conductor pattern, by means of laser radiation;

f.) Etching those regions of the metalization exposed in method step e) down to the surface of the substrate.

The advantages of the method outlined above
5 reside in particular in the fact that only a single organic protective layer has to be applied in an electrolytic dip-coating bath and, following first structuring by means of laser radiation, serves as an electrolytic resist and, after second structuring by
10 means of laser radiation, serves as an etch resist, and also does not have to be removed following the formation of the conductor pattern. The protective layer previously already used as a electrolytic resist and etch resist can, if appropriate, additionally be
15 used further as a solder-stop mask.

In WO 96/09646, a so-called Polymer Stud Grid Array (PSGA) is described which combines the advantages of a Ball Grid Array (BGA) with the advantages of MID technology. The description of the new design type as a
20 polymer stud Grid Array (PSGA) was carried out in this case following the model of the Ball Grid Array (BGA), the term "Polymer Stud" being intended to refer to the polymer studs formed at the same time during the injection molding of the substrate. The new design
25 type, suitable for single-chip, few-chip or multi-chip modules, comprises

- an injection-molded, three-dimensional substrate made of an electrically insulating polymer,
- polymer studs arranged over the area of the
30 underside of the substrate and formed at the same time during the injection molding,
- external connections formed on the polymer studs by a final surface that can be soldered,

- conductor trains, formed at least on the underside of the substrate, which connect the external connections to internal connections, and
 - at least one chip arranged on the substrate,
- 5 whose connections are electrically conductively connected to the internal connections. .

The invention specified in claim 1 is based on the problem of providing a simple and economical method for forming metallic conductor patterns having
10 connection regions that can be soldered and/or bonded on electrically insulating substrates which, in particular, is also suitable for the production of flexible circuits and Polymer Stud Grid Arrays (PSGA). With regard to the requirements placed on modern chip
15 packages, it should be possible for conductor patterns having extremely fine structures to be formed on the substrates.

The basis for the solution according to the invention is fine laser structuring, which makes it
20 possible to implement, on a processing area of, for example, $5 \times 5 \text{ cm}^2$, structures of about $40 \text{ }\mu\text{m}$ conductor width and $30 \text{ }\mu\text{m}$ insulation spacing, without clean-room conditions. Very dense, one-layer wiring between single-row or multi-row chip connections, and multi-row
25 printed circuit board connections can be implemented in this way.

Preferred refinements of the invention emerge from the subclaims.

Exemplary embodiments of the invention are
30 illustrated in the drawing and will be described in more detail below. In the drawing:

Figure 1 to Figure 8 show, in a very simplified schematic illustration, various method stages in the formation of metallic conductor patterns having connection regions which can be soldered on an electrically insulating substrate,

Figure 9 shows a section through a substrate, designed as a sheet, having connection regions on opposite sides of the sheet,

Figure 10 shows a section through a Polymer Stud Grid Array with connection regions formed on integral polymer studs,

Figure 11 shows an exemplary embodiment of an electrically conductive connection between the individual conductors of a conductor pattern,

Figure 12 shows a first exemplary embodiment of a flexible circuit with chip connections arranged on one side, and

Figure 13 shows a second exemplary embodiment of a flexible circuit with chip connections arranged in two rows.

According to Figure 1, the starting point is an electrically insulating substrate U1, which in the exemplary embodiment outlined is a thin flexible sheet.

The substrate U1 illustrated in Figure 1 is first slightly etched to increase the adhesion of the conductor pattern which is subsequently to be applied, and is then cleaned. After cleaning, seeding (not visible in detail from the drawing) of the substrate U1 is carried out, for example by dipping in a $\text{Pd-Cl}_2\text{-SnCl}_2$ bath.

After the seeding has been activated, a metalization M1, which can be seen from Figure 2, is applied over the whole area to the substrate

U1, this metalization being formed by a copper layer which is deposited chemically without externally applied current. If appropriate, the metalization M1 can also be further reinforced by subsequent
5 electrolytic copper deposition.

According to Figure 3, the metalization M1 is removed, by means of laser radiation LS, in the regions which directly adjoin the desired conductor pattern, in such a way that the individual conductors L1 of the
10 conductor pattern remain electrically connected to one another. The electrically conductive connection (not visible in Figure 3) of the individual conductors L1 will be explained in more detail at a later point using Figure 11.

According to Figure 4, an organic, electrolysis-resistant protective layer S is then applied to the conductor pattern in an electrolytic dip-coating bath, the electrically interconnected
15 conductors L1 of the conductor pattern having anodic or cathodic contact made with them, depending on the type of electrolytic dip-coating bath.
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According to Figure 5, the protective layer S can also be used as an etch resist, all those regions of the metalization M1 which do not correspond to the
25 conductor pattern being removed in a corresponding etching bath. Those regions of the metalization M1 which do not correspond to the conductor pattern can also remain on the substrate U1, however, and can be used later, for example as electromagnetic shielding.
30 In the latter case, the remaining regions of the metalization M1 likewise have an anodic or cathodic contact made with them, and are covered with the protective layer S.

Figure 6 shows the longitudinal extent of a
35 conductor L1 and the protective layer S applied to it in a section through the substrate U1 rotated through 90° by comparison with Figure 5.

According to Figure 7, the protective layer S is then removed again by means of laser radiation LS in the subsequent connection regions of the conductor pattern. In Figure 7, it is possible to see a connection region CA1, to be used later as a chip connection, and a connection region LA1, to be used later as a printed circuit board connection.

Subsequently, according to Figure 8, a final surface E which can be soldered is applied, by means of electrolytic metal deposition, to those regions of the conductor pattern exposed by means of laser radiation LS. In the exemplary embodiment illustrated, this final surface E is a tin/lead alloy.

Figure 9 shows a variant in which the substrate U1, formed by a flexible sheet, is provided with through-contact holes DL in the region of the connection regions CA1 serving later as chip connections. As a result, connection regions LA1 designed as printed circuit board connections, and conductors L1 leading away from these, can be arranged on the underside of the substrate U1, while the connection regions CA1 designed as chip connections can be arranged on the upper side of the substrate U1. In this case, the connection regions CA1 designed as chip connections are built up by means of the electrolytic deposition of the final surface E (which can be soldered) in the region of the through-contact holes DL.

Figure 10 shows a further exemplary embodiment, in which the method steps outlined using Figures 1 to 8 are applied during the production of a Polymer Stud Grid Array. Here, use is made of a three-dimensional substrate U2 produced by injection-molding a thermoplastic molding compound, on the underside of which polymer studs PS arranged over the area are formed at the same time during the injection molding. Furthermore, it is possible to see that a trough M for

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accommodating a chip is also formed on the underside of the substrate U2 during the injection molding, and that, in the region of this trough M,

polymer studs PH are likewise formed at the same time during the injection molding. The connection regions CA2 designed as chip connections are then produced on these polymer studs PH. The connection of the connection regions LA2 designed as printed circuit board connections and the connection regions CA2 designed as chip connections is carried out by means of conductors L2. The protective layer S covers all the regions of the conductor pattern which do not correspond to the connection regions LA2 and CA2.

Figure 11 shows an example of the electrically conductive connection of the conductors L1 of the conductor pattern. The connection is made here by means of a transverse web QS, which interconnects all the connection regions CA1 designed as chip connections. This transverse web QS then has anodic or cathodic contact made with it, depending on the type of bath, during the application of the protective layer S in an electrolytic dip-coating bath. Following the electrolytic deposition of the final surface, the transverse web can be severed, for example by means of stamping. A further simple and economic possibility is to sever the transverse web QS from the associated connection regions by means of laser radiation.

Figure 12 shows a first exemplary embodiment of a flexible circuit, in which the connection regions CA1 designed as chip connections and the conductors L1 are formed on one side of the substrate U1. The connection regions CA1 designed as chip connections are in this case arranged in a row in the edge region of the substrate U1. The connection regions LA1 designed as printed circuit board connections are arranged in two rows on the opposite side of the substrate U1. The production of these printed circuit board connections is carried out following the model of the procedure described in conjunction with Figure 9 in the region of through-contact holes, but these are not specifically illustrated in Figure 12.

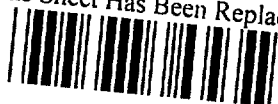
Figure 13 shows a second exemplary embodiment of a flexible circuit in which, as distinct from the embodiment according to Figure 12, two rows of connection regions CA1 designed as chip connections are provided, arranged so as to be offset from one another. This offset arrangement of the connection regions in two rows means that particularly low insulation spacings can be implemented between the individual conductors L1.



Patent claims

1. A method for forming metallic conductor patterns having connection regions (CA, LA1; CA, LA2)
5 that can be soldered and/or bonded on electrically insulating substrates (U1; U2), having the following method steps:
- a.) Applying a metalization (M1; M2) to the substrate (U1; U2)
- 10 b.) Removing the metalization (M1; M2), at least in those regions directly adjacent to the desired conductor pattern, in such a way that the individual conductors (L1; L2) of the conductor pattern remain electrically connected to one another;
- 15 c.) Applying an organic, electrolysis-resistant protective layer (S) to the conductor pattern in an electrolytic dip-coating bath;
- d.) Removing the protective layer (S) in the subsequent connection regions (CA, LA1; CA2, LA2);
- 20 e.) electrolytically depositing a final surface (E) which can be soldered and/or bonded to those regions of the metalization (M1; M2) exposed in method step d).
2. The method as claimed in claim 1, characterized in that a flexible sheet is used as the substrate (U1).
- 25 3. The method as claimed in claim 2, characterized in that connection regions (LA1) designed as printed circuit board connections and connector trains (LZ1) leading away from these are arranged on the underside of the substrate (U1), and in that connection regions
30 (CA1) designed as chip connections are arranged on the upper side of the substrate (U1), the connection regions (CA1) designed as

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chip connections being built up by means of the electrolytic deposition of the final surface (E) which can be soldered and/or bonded in the region of through-contact holes (DL).

5 4. The method as claimed in claim 1, characterized in that use is made of a three-dimensional substrate (U2) produced by injection-molding a thermoplastic molding compound.

10 5. The method as claimed in claim 4, characterized in that polymer studs (PS) arranged over the area are formed on the underside of the substrate (U2) at the same time during the injection molding, and in that connecting regions (LA2) designed as printed circuit board connections are produced on the polymer studs
15 (PS).

6. The method as claimed in claim 5, characterized in that a trough (M) for accommodating a chip is formed on the underside of the substrate (U2) during the injection molding, and in that the polymer studs (PS)
20 are arranged outside the trough region.

7. The method as claimed in claim 6, characterized in that polymer studs (PH) are formed at the same time in the region of the trough (M) during the injection molding, and in that connection regions (CA2) designed
25 as chip connections are produced on these polymer studs (PH).

8. The method as claimed in one of the preceding claims, characterized in that the metalization (M1; M2) is applied to the substrate (U1; U2) by chemical metal
30 deposition.





9. The method as claimed in claim 8, characterized in that the metalization (M1; M2) is produced by the chemical deposition of copper.

10. The method as claimed in claim 8 or 9,
5 characterized in that the metalization (M1; M2), before or after its structuring in method step b), is reinforced by electrolytic metal deposition.

11. The method as claimed in claim 10,
10 characterized in that the metalization (M1; M2) is reinforced by the electrolytic deposition of copper.

12. The method as claimed in one of the preceding claims, characterized in that the partial removal of the metalization (M1; M2) in method step b) is performed by means of fine laser structuring.

15 13. The method as claimed in claim 12, characterized in that, during the fine laser structuring, conductor tracks with a width (b) of about 35 to 45 μm and an insulation spacing (a) of about 25 to 35 μm are produced.

20 14. The method as claimed in one of the preceding claims, characterized in that the metalization (M1; M2) is applied to the entire surface of the substrate (U1; U2).

15. The method as claimed in claim 1,





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characterized in that, in process step c) in the electrolytic dip-coating bath, a temperature-resistant lacquer suitable as a solder-stop lacquer is applied as a protective layer (S) to the conductor pattern.

5 16. The method as claimed in claim 15, characterized in that the protective layer (S) is dried after being applied to the conductor pattern.

17. The method as claimed in claim 15 or 16, characterized in that the protective layer (S)
10 remaining after the structuring in method step d) is cured.

18. The method as claimed in one of the preceding claims, characterized in that the structuring of the protective layer (S) in method step d) is carried out
15 by laser structuring.

19. The method as claimed in one of the preceding claims, characterized in that in method step c) of claim 1 or in method step e) of claim 2, tin or a tin/lead alloy is deposited as the final surface (E).

20 20. The method as claimed in one of claims 1 to 18, characterized in that in method step c) of claim 1 or in method step e) of claim 2, nickel and gold are deposited as the final surface (E).

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