Conversion of a sequence of m-bit information words into a modulated signal.

The invention relates to an apparatus for converting a sequence of m-bit information words into a modulated digital signal, where m is an integer, the apparatus comprising

- input means for receiving the sequence of m-bit information words,
- m-to-n bit converter means for converting the sequence of m-bit information words into a sequence of n-bit codewords, where n is an integer larger than m, the sequence of codewords forming the modulated signal, which signal comprises bit cells having a first signal value and bit cells having a second signal value,
- determining means for determining a coding state related to a digital sum value at the end of a modulated signal portion, which digital sum value denotes for said modulated signal portion a running value of a difference between the number of bit cells having the first signal value and the number of bit cells having the second signal value, the m-to-n bit converter means comprising selection means for selecting for the conversion a code word from a set of codewords that depends on the coding state, at least one of the digital sum values determining a first and a second coding state, the first and second coding state being determined in response to the information word that corresponds to the previous codeword and to a method for converting a sequence of m-bit information words into a modulated digital signal.

The invention further relates to a recording apparatus in which such a conversion apparatus is used.

The invention further relates to the modulated signal obtained and to a record carrier on which the modulated signal is recorded.

The invention furthermore relates to an apparatus for reconverting the modulated signal into a sequence of m-bit information words.

Finally, the invention relates to a reading apparatus in which a record carrier of this type is used.

A conversion apparatus as defined in the opening paragraph is known from WO 95/27,284, document D1 in the list of related documents that can be found at the end of the description.

Said document describes a modulation system in which a sequence of 8-bit information words is converted to a sequence of 9-bit code words. The sequence of 9-bit code words forms a modulated signal, which signal comprises bit cells having a first or a second signal value, such as a 'high' and a 'low' signal value representing the logical bit values '1' and '0' respectively in the codewords. Each bit cell represents a bit from the 9-bit codeword sequence, whilst the logical value of the bit is denoted by the signal value of the bit cell. On conversion, each time a 9-bit code word is delivered, together with a coding state, said coding state having a relation with a digital sum value for the delivered part of the modulated signal. This digital sum value denotes the difference between the number of 'high' bit cells and the number of 'low' bit cells for the delivered part of the modulated signal.

The next code word to be delivered is selected from a set of code words in dependence of the coding state derived with the previous codeword. The code words in the set are selected in such a way that the digital sum value of the modulated signal remains within a small range, which leads to the fact that the frequency spectrum of the signal has reduced frequency components in the low-frequency area. Such a signal is also referenced a DC-free signal or DC-balanced signal. The lack of low-frequency components in the signal generally has great advantages for information transfer *via* a record carrier or other transmission channels, such as eg. an optical fibre.

The conversion apparatus known from WO 95/27,284 provides for an increased information density on the record carrier.

The known apparatus, however, has the disadvantage that sometimes errors occur upon reconversion, resulting in a distorted reconverted sequence of information words.

It is an object of the invention to provide a conversion apparatus capable of generating a modulated signal such that the conversion-reconversion chain is less prone to errors.

In accordance with the invention, this object is achieved with the apparatus as claimed in claim 1.

The invention is based on the recognition that the errors that occur in the conversion and subsequent reconversion chain, result from an incorrect clock recovery in the reconversion apparatus, which clock frequency is recovered from the incoming modulated signal. In the known apparatus, the maximum runlength of the modulated signal is 9. The longer the maximum runlength is, the larger is the probability of occurrence of errors in the recovered clock frequency, resulting in more errors in the reconverted sequence of information words.

In accordance with the invention, the conversion apparatus is adapted to generate a modulated signal having a maximum runlength that does not exceed 7. This is a significant decrease compared to a maximum runlength of 9, as per the prior art conversion apparatus. Thus, the reliability of the clock recovery process in the reconversion apparatus is largely improved, resulting in a significant decrease in the occurrence of errors in the regenerated sequence of information words.

Preferably, apparatus as claimed in claim 1, wherein n is odd and equals m+1. This results in maintaining the advantage of a high information density, when recording the modulated signal on a record carrier

The requirement of a smaller maximum runlength leads to another conversion table. Surprisingly, it was possible to generate such conversion table for the available number of 2^m information words, although the maximum runlength was decreased to 7.

In addition, other sync words are required in order to satisfy the same requirement for the maximum runlength. More specifically, the apparatus further comprises

- sync word generator means for generating a sync word for a block of p consecutive code words in the modulated signal, the sync word generator means being adapted to generate said sync word from the following set of available sync words:

11100011111110, 10100011111110, 01100011111110 and 11000100000001,

the sync word generator means being adapted to select one of the sync words in dependence of the coding state. The apparatus further comprises

- sync word generator means for generating a sync word for a block of p consecutive code words in the modulated signal, the sync word generator means being adapted to generate said sync word from the following set of available sync words:

11100011111110, 10100011111110, 01100011111110, 11000100000001, 01011100000001,

10011100000001, and 00011100000001
the sync word generator means being adapted to select one of the sync words in dependence of the coding state.

These and other aspects of the invention will be apparent from and further elucidated with reference to the embodiments described in the following figure description, in which:

Figure 1 shows a sequence of information words and the corresponding sequence of code words, resulting in the modulated signal;

Figure 2 shows tables in which the relation between the information words and code words, in dependence of the coding state, is laid down;

Figure 3 shows an embodiment for the conversion apparatus according to the invention;

Figure 4 shows a modification of the conversion apparatus of Fig. 3 for inserting sync signals;

Figure 5 shows a reconversion apparatus;

Figure 6 shows portions of a modulated signal and the corresponding information words derived therefrom;

Figure 7 shows a record carrier;

Figure 8 shows a recording apparatus, and

Figure 9 shows a reading apparatus.

Figure 1 shows four successive m-bit information words, in this case 8-bit information words referenced 1. The four information words 1 have the respective decimal word values "1", "61", "58" and "49". This sequence of four information words 1 is converted to four successive n-bit code words, in this case 9-bit code words referenced 4. The code words 4 form a bit string of bits having a logical '0' value and bits having a logical '1' value. The conversion of the information words into codewords is such that, in the bit string of codewords, the number of consecutive bits having the same logical value is equal to 7 at the most. The individual bits of the code words will be referenced x1, ..., x9 in the following, where x1 indicates the first bit (from the left) of the code word and x9 the last bit of the code word.

The bit string of the code words 4 form the modulated signal 7. This modulated signal 7 contains four information signal portions 8 each representing one of the code words 4. The information signal portions 8 contain bit cells 11 which have a high signal value H and bit cells 12 which have a low signal value L. The number of bit cells for each information signal portion 8 is equal to the number of bits of the corresponding code word 4. Each codeword bit having a logical '1' value is indicated in the modulated signal 7 by one of the bit cells 11 having the high signal value H. Each codeword bit having the logical '0' value is indicated in the modulated signal 7 by one of the bit cells 12 having the low signal value L.

Furthermore, the requirement is made on the modulated signal 7 that the running digital sum value vary only within a limited range B2, which means that the frequency spectrum of the modulated signal 7 comprises substantially no low-frequency components. Worded differently, the modulated signal 7 is DC-free.

The digital sum value is in this respect meant to be understood as the difference between the number of preceding bit cells having a high signal value and the number of preceding bit cells having a low signal value. Worded differently, the digital sum value corresponds to the integrated value of the modulated signal.

Figure 1 shows the variation of the digital sum value in curve 20. In Fig. 1 said range B2 in which the digital sum value varies, lies between -4 and +5.

In the embodiment described, the number of different values the digital sum value can assume at the ends of the signal portions 8 is equal to 8. These values lie in a range B1 bounded by the values -3 and +4. The number of consecutive bit cells having the same signal value, defined as the maximum runlength, is lower than given in the prior art coding device, namely 7. In spite of this restriction of the maximum runlength, it appeared to be possible to generate a conversion table, to be described later with reference to figure 2, for the conversion of all 256 8-bit information words.

The number of bits of the code words is odd, which means that the digital sum value at the ends of the signal portions 8 will be alternately odd and even. The code words in which the digital sum value at the beginning is even will be referenced even code words in the following. The code words in which the digital sum value at the beginning is odd will be referenced odd code words in the following. Periods of time in which an even code word is delivered will be referenced even periods II and periods of time in which an odd code word is delivered will be referenced odd periods I.

Hereafter there will be a detailed description of an embodiment for the

method according to the invention by which the modulated signal 7 can be obtained.

Either one of the two digital sum values '-3' and '+4' at the end of each information portion determines a coding state of the second type. In the embodiment described the digital sum value '-3' determines the coding state S1 and the digital sum value '+4' the coding state S14. Each of the digital sum values '-2', '-1', '0', '1', '2', '3' refer to coding states of the first type.

More specifically, the coding states S8 and S9 both correspond to the digital sum value '-2'. After having converted an information word into a codeword, which resulted in the digital sum value of '-2', the coding state reached (S8 or S9, in this example) is determined by this digital sum value, as well as by the specific information word that has been converted last. The coding states S2 and S3 correspond to the digital sum value '-1'. After having converted an information word into a codeword, which resulted in the digital sum value of '-1', the coding state reached (S2 or S3, in this example) is determined by this digital sum value, as well as by the specific information word that has been converted last.

In the same way, the coding states S10 and S11 correspond to the digital sum value '0', the coding states S4 and S5 correspond to the digital sum value '1', the coding states S12 and S13 correspond to the digital sum value '2', and the coding states S6 and S7 correspond to the digital sum value '3'.

In the matrix T below, each element t_{ij} denotes the number of different code words with which it is possible to abandon state i and enter state j.

0	0	0	0	0	0	0	90	90	69	69	27	27	3
0	0	0	0	0	0	0	54	54	55	55	40	40	18
0	0	0	0	0	0	0	63	63	65	65	36	36	9
0	0	0	0	0	0	0	41	41	56	56	55	55	37
0	0	0	0	0	0	0	38	38	68	68	65	65	32
0	0	0	0	0	0	0	20	20	41	41	54	54	42
0	0	0	0	0	0	0	10	10	38	38	63	63	48
48	63	63	38	38	10	10	0	0	0	0	0	0	0
42	54	54	41	41	20	20	0	0	0	0	0	0	0
32	65	65	68	68	38	38	0	0	0	0	0	0	0

37	55	55	56	56	41	41	0	0	0	0	0	0	0
9	36	36	65	65	63	63	0	0	0	0	0	0	0
18	40	40	55	55	54	54	0	0	0	0	0	0	0
3	27	27	69	69	90	90	0	0	0	0	0	0	0

This table has been obtained using the requirement that the maximum runlength is 7. Further some additional boundary conditions for the various codewords have been adopted, such as

- the codewords in states S1, S8 and S9 have at maximum 2 leading 'zeroes' and at maximum 5 leading 'ones',
- the codewords in states S2, S3, S10 and S11 have at maximum 3 leading 'zeroes' and at maximum 4 leading 'ones',
- the codewords in states S4, S5, S12 and S13 have at maximum 4 leading 'zeroes' and at maximum 3 leading 'ones', and
- the codewords in states S6, S7 and S14 have at maximum 5 leading 'zeroes' and at maximum 2 leading 'ones'.

Further,

- when the next state is S1, S8 or S9, the codewords have at maximum 2 trailing 'ones' and at maximum 5 trailing 'zeroes',
- when the next state is S2, S3, S10 or S11, the codewords have at maximum 3 trailing 'ones' and at maximum 4 trailing 'zeroes',
- when the next state is S4, S5, S12 or S13, the codewords have at maximum 4 trailing 'ones' and at maximum 3 trailing 'zeroes', and
- when the next state is S6, S7 or S14, the codewords have at maximum 5 trailing 'ones' and at maximum 2 trailing 'zeroes'.

Starting from an even digital sum value, always an odd sum value is reached and *vice versa*. The elements in the matrix denoting transitions from an even digital sum value to another even sum value and transitions from an odd sum value to another odd sum value are therefore all equal to "0". The matrix is also symmetrical. This is due to the case where a code word changes a computed first digital sum value into a computed second digital sum value, said second digital sum value is changed into the first digital sum value by the inverse of the code word concerned.

To each of the coding states S1, ... S14 is assigned a set V1, ..., V14 of

code words, which contains a code word for each possible information word. In the case where the number of bits for each information word is equal to 8, each set thus contains 256 code words.

Furthermore, the sets of code words are selected such that the sets of code words established by the second coding states of the first type which belong to the same digital sum value, are disjunct, in other words, these sets have no code words whatsoever in common. In the embodiment shown, V2 and V3, V4 and V5, V6 and V7, V8 and V9, V10 and V11, V12 and V13 are pairs of disjunct sets.

The digital sum value '-1' always causes a code word from the set V2 or a code word from the set V3 to be assigned to the next information word to be converted. This means that during the information word conversion each of the code words leading to a digital sum value '-1' can be used twice. This code word (leading to the digital sum value '-1'), together with a random code word from the set V2, forms a bit combination that can be distinguished from the bit combination formed by the same code word and the random code word from the set V3. In similar fashion, each of the code words resulting in one of the digital sum values '+1', '+3', '-2', '0' and '+2' can be used twice for forming uniquely, together with the next word, two different information words.

All this means that the number of unique bit combinations is increased considerably, compared to coding systems in which each code word *per se* is to define an information word in a unique manner.

Since for a code word that changes the digital sum value from a first value to a second value always the inverse codeword value changes the digital sum value back from the second value to the first value, a set of code words can be assigned to one-half of the number of coding states, for example, the coding states belonging to a set of coding states determined by an odd digital sum value. The code words for the coding states determined by the even digital sum values may then be obtained by inverting the code words from the sets that belong to the coding states determined by the odd digital sum values. In the embodiment described here, the code words belonging to the coding state S_i are the inverse of the code words belonging to the state S_{15-i}, where i is an integer greater than or equal to 1 and smaller than or equal to 14.

By way of illustration Fig. 2 shows in the first column the word values WW of all the 256 different 8-bit information words. The dedicated sets V1, V2, V3, V4, V5, V6 and V7 are shown in the respective second, fourth, sixth, eighth, tenth, twelfth and fourteenth columns.

The relations between the information words and code words in Fig. 2 are selected such that in the case where the same code word occurs in two or more of the sets V1, V2, V3, V4, V5, V6 and V7, this code word, combined with the next code word, as required, always establishes the same information word. This is advantageous in that on the recovery of the information words the corresponding coding states need not be determined, which results in little error propagation on the recovery of the information words. The disjunct sets belonging to the digital sum value can be distinguished in Figure 2 on the basis of the bits x1 and x8 of the code words. In the code words in the sets belonging to the coding states S3, S5, S7, the logical values of bit x1 and bit x8 are not the same, whereas in the disjunct sets established by the corresponding coding states S2, S4 and S6, the bits x1 and x8 have the same logical value.

The digital sum value at the beginning of the code word uniquely determines, together with the codeword, the digital sum value at the end of the code word. This digital sum value at the end of this code word, combined with the converted information word, determines the coding state which is established at the end of the code word concerned. These coding states Sx which are determined at the end of each of the code words from the sets V1, V2, V3, V4, V5, V6 and V7 are shown in the respective third, fifth, seventh, ninth, eleventh, thirteenth and fifteenth columns, respectively.

The sets V14, V13, V12, V11, V10, V9 and V8 can be derived by a codeword inversion from the code words of the sets V1, V2, V3, V4, V5, V6 and V7, respectively. The coding states S_i corresponding to the DSV value at the end of the code words, for i larger than 7, can be converted in accordance with the relation $S_{in} = S_{15-i}$, so as to obtain the coding state S_{in} shown in the third, fifth, seventh, ninth, eleventh, thirteenth and fifteenth columns.

The conversion of the sequence of information words 1 to the sequence of code words 4 as shown in Figure 1 can be explained by means of the Tables shown in Figure 2. At the instant at which the first information word (word value '1') is to be converted, the digital sum value is equal to '0'. This means that the code word is to be selected from the set V10 or V11, depending on the information word that was encoded directly prior to the information word '1'. Assuming that this information word, together with the digital sum value '0', determines the coding state S11, the code word corresponding to the information word '1' is to be selected from set V11. Based upon the conversion rule given above, the desired code word may be obtained by inversion of the code word '110101010' which is assigned to the information word having the word value '1' in the set V4 (S_{in}) = S_{15-11}) =

S_4). The code word thus obtained is then equal to '001010101'. The coding state at the end of the code word corresponding to the information word '1' is then S3. This follows directly from column 9 in table 2. This also follows more or less directly from figure 1, in the sense that at the end of the codeword corresponding to the encoded information word '1', the DSV equals -1, which corresponds to a state of either S2 or S3, as per figure 1. It is the state S3, as encoding the information word '0', instead of the information word '1', which results in the same codeword, would have led to the state S2, see also the table of figure 2.

Being in the coding state S3, this means that the next code word is to be selected from set V3. The next information word to be converted has the word value '61', which means that the next code word is equal to '011010111'. In accordance with column 7 in the table of figure 2, the next coding state is equal to S3. This again corresponds with figure 1, which shows that the DSV equals 2 at the end of the codeword corresponding to the information word '61'. This DSV value corresponds to either state S12 or S13. It is state S12, as encoding the information word '60', instead of the information word '61', which results in the same codeword, would have led to the state S13, see also the table of figure 2.

Being in the coding state S12, this means that the next code word is the inverse of the code word assigned to the next information word in the set V3, as $S_{in}=S_{15-12}$. In this case the word value of the next information word is '58'. The dedicated code word in the set V3 is '010111110'. The information word is converted to the inverse of this code word and thus to '101000001'. The next coding state then becomes equal to S2, see column 7 in the tables of figure 2. The code word for the next information word to be converted is thus to be selected from the set V2. This information word to be converted has the word value "49", so that the dedicated code word is equal to '011001100'.

Figure 3 shows an embodiment for a conversion apparatus 140 according to the invention by which the method described above can be implemented. The conversion apparatus is arranged for converting the m-bit information words 1 to the m-bit code words 4, whilst the number of different coding states can be denoted by s bits. The conversion apparatus comprises a converter 60 for converting (m+s) binary input signals to (n+s) binary output signals. From the inputs of the converter m inputs are connected to a bus 61 for receiving m-bit information words. From the outputs of the converter n outputs are connected to a bus 62 for supplying n-bit code words. Furthermore, s inputs are connected to an s-bit bus 63 for receiving a state word denoting the current coding state. The state word is

produced by a buffer memory 64, for example, in the form of s-flip flops. The buffer memory 64 has s inputs connected to a bus 58 for receiving a state word to be loaded in the buffer memory. For transporting the state word to be loaded in the buffer memory, s outputs of the converter 60 are used which are connected to the bus 58.

The bus 62 is connected to a controllable inverter circuit 75 of a customary type which, in response to a control signal on its input, inverts or not the n-bit code words received over bus 62 and conveys them to a bus 76. The bus 76 is connected to parallel inputs of a parallel/serial converter 66. The parallel/serial converter 66 converts the n-bit code words received over bus 76 into a serial datastream, which is the modulated signal 7 supplied over a signal line 70.

The converter 60 may comprise a ROM memory which stores the code word sets shown in Figure 2 in the form of a so-termed look-up tables at addresses established by the combination of state word and information word applied to the inputs of converter.

The converter 60 may comprise, *in lieu of* a ROM memory, a combinatorial logical circuit formed by gate circuits.

The synchronization of the operations performed in the device may be obtained in customary fashion with synchronized clock signals which may be generated by a clock generation circuit 77. The clock generation circuit 77 causes, by applying the control signal to the inverter circuit 75, the code words delivered by the converter for the even periods II to be inverted by the inverter circuit 75 and the code words delivered by the converter 60 for the odd periods I to be delivered unchanged by the converter 60.

In the embodiment shown the new coding state is directly delivered by the converter. In principle, however, it is alternatively possible that the new coding state is derived by computing the digital sum value at the end of each delivered code word and to derive the new coding state based upon the digital sum value thus computed. In that case the device is to comprise a unit for computing the digital sum values as well as a unit which applies a corresponding state word to the buffer memory 64 based upon the computed digital sum value.

Sync words are added to blocks of codewords of the modulated signal 7. The sync words preferably have a signal pattern that cannot occur in a random sequence of information signal portions. Equally preferably, parts of the sync words together with a part of an adjacent information signal portion, cannot form a signal pattern that corresponds to the pattern of the sync words. The sync words are inserted into the sequence of n-bit code

words. The table below shows seven 14-bit sync words which are pre-eminently suitable for use in combination with the code words shown in Fig. 2.

1	11100011111110	6
2	10100011111110	6
3	01100011111110	6
4	01011100000001	1
5	10011100000001	1
6	00011100000001	1
7	11000100000001	1

The first column of the table shows coding states. The second column in the Table shows the sync words dedicated to this coding state. The third column shows the coding state adopted after the sync word has been delivered.

The sync words delivered at the coding states S2, S4, S6 can be distinguished on the basis of the bits x1 and x8 from the sync words delivered at the coding states S3, S5 and S7 in the same way as the code words coming after these coding states can be distinguished. At the coding states S2, S4 and S6 a sync word is delivered for which the logical value of the bits x1 and x8 is the same. In the sync words delivered at the coding states S3, S5 and S7, the logical value of the bits x1 and x8 is not the same.

From the sync words listed above, it is clear that some of them are the inverse of others. A sync word generator may thus be required that generates the sync words

11100011111110, 10100011111110, 01100011111110, and
11000100000001.

With the addition of sync words to the sequence of codewords, the matrix T given above will change.

In the matrix T below, each element t_{ij} denotes the number of different code words with which it is possible to abandon state i and enter state j, when also having sync words in the sequence of codewords.

0 0 0 0 0 0 0 87 87 68 68 25 25 2

0 0 0 0

0	0	0	0	0	0	0	61	61	64	64	36	36	8
0	0	0	0	0	0	0	40	40	56	56	55	55	36
0	0	0	0	0	0	0	38	38	67	67	64	64	32
0	0	0	0	0	0	0	20	20	40	40	53	53	42
0	0	0	0	0	0	0	9	9	38	38	62	62	48
48	62	62	38	38	9	9	0	0	0	0	0	0	0
42	53	53	40	40	20	20	0	0	0	0	0	0	0
32	64	64	67	67	38	38	0	0	0	0	0	0	0
36	55	55	56	56	40	40	0	0	0	0	0	0	0
8	36	36	64	64	61	61	0	0	0	0	0	0	0
18	39	39	54	54	54	54	0	0	0	0	0	0	0
2	25	25	68	68	87	87	0	0	0	0	0	0	0

The next table shows the runlength distribution of the new coding method compared to the runlength distribution of the coding method described in WO 95/27,284.

runlength (in # bits)	runlength distribution of new method	runlength distribution of known method
1	0.5104302	0.5150166
2	0.2770573	0.2772678
3	0.1348177	0.1306489
4	0.0552561	0.0519760
5	0.0182932	0.0191180
6	0.0037600	0.0049965
7	0.0003854	0.0008885
8	0.0000000	0.0000833
9	0.0000000	0.0000044

It should be noted here, that the results given in the above table are from modulated signals without any sync words in them.

The table shows that runlengths larger than 7 do not occur in the new coding method and that further, runlengths of 5, 6 and 7 bits occur less frequently in the new coding method than in the prior art coding method. This results in a better clock recovery property for the new coding method.

Figure 4 shows a modification of the conversion apparatus shown in Fig. 3, by which sync words can be inserted in the manner described above. In Fig. 4 the components identical with the components shown in Figure 3 have like reference characters. The modification relates to a memory 103 having seven memory locations which each accommodate one of the seven sync words from the table. The memory 103 comprises an addressing circuit for addressing one of the seven memory locations in response to the state word received over bus 63 on address inputs of the memory 103. The sync word in the addressed memory location is applied to a parallel/serial converter 105 over a bus 104. The

serial output of the converter 105 is applied to a first input of an electronically operable switch unit 106. The serial output of the parallel/serial converter 66 is connected to a second input of the switch unit 106. The conversion apparatus is controlled by the control circuit 77 adapted for this purpose to alternately bring the conversion apparatus into a first and a second mode. In the first mode, a predefined number of information words is converted to code words which are serially applied to the signal line 70 *via* the switch unit 106. At the transition from the first to the second mode, the conversion of information words is interrupted and the sync word established by the state word is delivered by the memory 103 and applied to the signal line 70 *via* the parallel/serial converter 105 and switch unit 106. In addition, at the transition from the second to the first mode, the buffer memory 64 is loaded, under the control of the control circuit 77, with the new coding state determined by the delivered sync word, after which the conversion from information words to code words is resumed until the conversion apparatus is again brought to the second mode by the control circuit 77.

Figure 5 shows an embodiment for a reconversion apparatus 150 according to the invention, for reconverting the modulated signal obtained by the implementation of the methods described above to a sequence of information words. The reconversion apparatus comprises two series-arranged shift registers to which the modulated signal 7 is applied. Each of the shift registers 111 and 112 has a length corresponding to the length of an n-bit code word. The contents of the shift registers 111 and 112 are fed to respective buses 113 and 114 through parallel outputs. The reconversion apparatus comprises an (n+p)-to-m-bit converter 115. All the n bits available in the shift register 112 are applied to inputs of the converter 115 *via* the bus 114 and a controllable inverter circuit 110. From the n bits available in the shift register 111, the p bits that together with the n bits in the shift register 114 uniquely establish an information word are applied to the converter 115. In this example they are the bits x1 and x8. The converter 115 may comprise a memory with a look-up table that contains an m-bit information word for each permitted bit combination formed by the n bits of an n-bit code word and the predefined p bits of a bit string portion following this code word. The converter 115 may also be formed by gate circuits, however. As the controllable inverter circuit 110 is inserted between the outputs of register 112 and the inputs of the converter 115. the converter 115 only needs to be capable of processing code words from the sets V1 to V7. For that matter, the code words in the odd periods I are inverse to the code words in the even periods II. The reconversion apparatus is then to comprise means for alternately activating (in the even periods) and deactivating (in the odd

periods) the inverter circuit 110. The inverter circuit 110 is of a customary type which, in deactivated state, transfers the code words received on its input unmodified to the converter 115. In active state the inverter circuit 110 transfers the received code words in inverse form to the converter 115.

The control of the inverter circuit 110 and the conversions carried out by the converter 115 may be synchronized in a customary manner by a synchronizing circuit 117, so that each time a code word as a whole is loaded in the shift register 112, the information word corresponding to the bit combination applied to the inputs of the converter 115 is available on the outputs of the converter.

Preferably, a sync word detector 116 connected to the buses 113 and 114 and detecting the bit patterns corresponding to the sync words is used during the synchronization process.

In order for the sync word detector 116 to function properly, a clock signal which has a relation to the bitfrequency may be applied to the sync word detector 116. This clock signal is supplied by a clock signal recovery circuit 118, which clock recovery circuit generates the clock signal from the incoming modulated signal 7. In general, it can be said that for all other functions in the apparatus, such as the bit detection itself, the clock recovery by the recovery circuit 118 should be very accurate.

By way of illustration, Figure 6 shows a signal which can be obtained with the invented method described above. The signal comprises a sequence of q successive information signal portions 160, where q is an integer, which portions represent q information words. Sync words, of which Figure 6 shows one, referenced 161, are inserted between blocks of codewords. A plurality of information signal portions 160 are shown in detail. Each of the information signal portions 160 contains n bit cells, in this case 9, which have a first (low) signal value L or a second (high) signal value H. The number of successive bit cells having the same signal value is equal to 1 at the least and equal to 7 at the most. Due to the digital sum value-dependent selection of the code words the running value of the difference between the number of bit cells having the first signal value and the bit cells having the second signal value at a random point in the signal is substantially constant in the signal portion preceding this point. Each information signal portion 160 resulting in either of the digital sum values '-3' or '4', uniquely establishes an information word. Each information signal portion representing a code word which results in one of the digital sum values from '-2' to '3', together with an adjacent signal portion, uniquely establishes an information word.

In Figure 6 they are, for example, the information signal portions 160a and 160b. These information signal portions, together with the bit cells on the first and eighth positions of a next signal portion, establish the information words having the word values '61' and '58'.

Figure 7 shows, by way of example, a portion of a record carrier 120 according to the invention. The record carrier shown is one of the magnetically detectable type. The record carrier may, however, also be of a different type, for example, a optically detectable type. The record carrier shown is tape-like shaped. However, the invention may also be applied to disk-like record carriers. The record carrier 120 contains tracks T1, T2, T3, ... running parallel to each other in the longitudinal direction of the record carrier, in which tracks the modulated signal can be recorded.

Figure 8 shows a recording apparatus for information recording, in which the conversion apparatus according to the invention is used, for example, the conversion apparatus 140 shown in Figure 3. In the recording apparatus the signal line for delivering the modulated signal is connected to a control circuit 141 for a write head 142, along which a record carrier 143 of an inscribable type is moved in a direction indicated by the arrow. The write head 142 is a magnetic write head which is capable of writing the modulated signal in a track on the record carrier 143. The control circuit 141 may likewise be of a customary type generating a write signal for the write head in response to the modulated signal applied to the control circuit 140, so that the write head 142 realises a magnetic pattern in the track corresponding to the modulated signal.

Figure 9 shows a reproducing apparatus in which a reconversion apparatus according to the invention is used, for example, the reconversion apparatus 150 shown in Figure 5. The reproducing apparatus comprises a read head 152 of a customary type for reading a record carrier according to the invention on which an information pattern corresponding to the modulated signal is written. With it the read head 152 produces an analog read signal which is converted to a binary signal in the circuit 153, which binary signal is subsequently fed to the reconversion apparatus 150. The circuit 153 may comprise, for example, a so-termed partial response detector.

Whilst the present invention has been described with respect to preferred embodiments thereof, it is to be understood that these are not limitative examples. Thus, various modifications may become apparent to those skilled in the art, without departing from the scope of the invention, as defined in the appended claims.

Further, the invention lies in each and every novel feature and

combination of features.

The conversion/reconversion apparatuses described are very well suitable in multitrack recording/reproduction apparatuses, as described in EP pat. appln. no. 95202926.2, document D2, EP pat. appln. no. 95203028.6, document D3, EP pat. appln. no. 95203029.4, document D4, EP pat. appln. no. 95203192.0, document D5 and EP pat. appln. no. 95203380.1, document D6, in the list of related documents. Further, the invention is equally well applicable in transmission systems for transmitting the modulated signal via a transmission medium, such as an optical fibre, see EP-A 97,763, document D7 in the list of related documents.

Related documents

(D1)	WO 95/27,284 (PHN 14.789)
(D2)	EP pat. appln. no. 95202926.2 (PHN 15.520), filing date 30.10.95
(D3)	EP pat. appln. no. 95203028.6 (PHN 15.543), filing date 08.11.95
(D4)	EP pat. appln. no. 95203029.4 (PHN 15.545), filing date 08.11.95
(D5)	EP pat. appln. no. 95203192.0 (PHN 15.563), filing date 21.11.95
(D6)	EP pat. appln. no. 95203380.1 (PHN 15.594), filing date 07.12.95
(D7)	EP-A 97,763

CLAIMS:

1. Apparatus for converting a sequence of m-bit information words into a modulated digital signal, where m is an integer, the apparatus comprising

- input means for receiving the sequence of m-bit information words,
- m-to-n bit converter means for converting the sequence of m-bit information words into a sequence of n-bit codewords, where n is an integer larger than m, the sequence of codewords forming the modulated signal, which signal comprises bit cells having a first signal value and bit cells having a second signal value,
- determining means for determining a coding state related to a digital sum value at the end of a modulated signal portion, which digital sum value denotes for said modulated signal portion a running value of a difference between the number of bit cells having the first signal value and the number of bit cells having the second signal value, the m-to-n bit converter means comprising selection means for selecting for the conversion a code word from a set of codewords that depends on the coding state, at least one of the digital sum values determining a first and a second coding state, the first and second coding state being determined in response to the information word that corresponds to the previous codeword,

wherein the apparatus is adapted to form a modulated signal satisfying the requirement that the number of consecutive bit cells in the modulated signal having the same signal value does not exceed 7.

2. Apparatus as claimed in claim 1, wherein n is odd and equals m+1.

3. Apparatus as claimed in claim 2, wherein m is equal to 8 and n is equal to 9.

4. Apparatus as claimed in claim 1, 2 or 3, the apparatus further comprising

- sync word generator means for generating a sync word for a block of p consecutive code words in the modulated signal, the sync word generator means being adapted to generate said sync word from the following set of available sync words:

11100011111110. 10100011111110, 01100011111110 and 11000100000001,
the sync word generator means being adapted to select one of the sync words in dependence of the coding state.

5. Apparatus as claimed in claim 1, 2 or 3, the apparatus further comprising sync word generator means for generating a sync word for a block of p consecutive code words in the modulated signal, the sync word generator means being adapted to generate said sync word from the following set of available sync words:

11100011111110, 10100011111110, 01100011111110, 11000100000001, 01011100000001, 10011100000001, and 00011100000001
the sync word generator means being adapted to select one of the sync words in dependence of the coding state.

6. Apparatus as claimed in claim 5, the sync word generator means being adapted to generate the following sync words:

1	11100011111110	6
2	10100011111110	6
3	01100011111110	6
4	01011100000001	1
5	10011100000001	1
6	00011100000001	1
7	11000100000001	1

where the value in the first column indicates the coding state after having converted the information word directly preceding the sync word to be added, the bit sequence in the second column indicates the sync word generated in response to said coding state and the value in the third column indicates the coding state required to obtain the codeword directly following the sync word.

7. Apparatus as claimed in claim 4, 5 or 6, wherein the sync words generated present bit patterns that cannot occur in the bit sequence of the codewords.

8. Apparatus as claimed in anyone of the preceding claims, wherein the sets of code words belonging to each pair of coding states of the first type are disjunct.

9. Apparatus as claimed in claim 8, wherein the sets of code words belonging to the pairs of coding states of the first type are mutually distinguishable based

upon the logical values of bits on p predefined positions in the code words, where p is an integer smaller than or equal to n.

10. Apparatus as claimed in claim 1, wherein the m-to-n bit converter means are adapted to convert m-bits information words into n-bit codewords in accordance with the conversion tables given in figure 2.

11. Recording apparatus for recording a modulated signal in a track on a record carrier, comprising the conversion apparatus as claimed in anyone of the preceding claims, further comprising writing means for writing the modulated signal in said track on the record carrier.

12. Method for converting a sequence of m-bit information words into a modulated digital signal, where m is an integer, the method comprising the steps of

- receiving the sequence of m-bit information words,
- converting the sequence of m-bit information words into a sequence of n-bit codewords, where n is an integer larger than m, the sequence of codewords forming the modulated signal, which signal comprises bit cells having a first signal value and bit cells having a second signal value,
- determining a coding state related to a digital sum value at the end of a modulated signal portion, which digital sum value denotes for said modulated signal portion a running value of a difference between the number of bit cells having the first signal value and the number of bit cells having the second signal value, the converter step comprising the substep of selecting for the conversion a code word from a set of codewords that depends on the coding state (63), at least one of the digital sum values determining a first and a second coding state, the first and second coding state being determined in response to the information word that corresponds to the previous codeword,

wherein the modulated signal satisfies the requirement that the number of consecutive bit cells in the modulated signal having the same signal value does not exceed 7.

13. Modulated signal obtained with the method as claimed in claim 12.

14. Record carrier obtained with the recording apparatus as claimed in claim 11.

15. Apparatus for reconverting a modulated signal into a sequence of m-bit information words, where m is an integer, the apparatus comprising

- input means for receiving the modulated signal comprising a sequence of n bit codewords,

n-to-m bit converter means for converting the sequence of n-bit codewords into a sequence of m-bit information words by assigning an information word to a codeword to be converted in dependence of said codeword to be converted, where n is an integer larger than m,

the converter means being adapted to assign the information word to a codeword in dependence of the logical values of the bits in the bitstring which are situated at p predefined positions with respect to the corresponding codeword, and where the modulated signal satisfies the requirement that the number of consecutive bit cells in the modulated signal having the same signal value does not exceed 7.

16. Apparatus as claimed in claim 15, wherein the apparatus comprises sync word detector means for detecting sync words present in the modulated signal having the following bit patterns:
11100011111110, 10100011111110, 01100011111110, and
11000100000001.

17. Apparatus as claimed in claim 15, wherein the apparatus comprises sync word detector means for detecting sync words present in the modulated signal having the following bit patterns:
11100011111110, 10100011111110, 01100011111110, 11000100000001, 01011100000001, 10011100000001, and 00011100000001

18. Apparatus for reading a modulated signal from the record carrier as claimed in claim 14, provided with the reconversion apparatus as claimed in claim 15, 16 or 17, further comprising reading means for reading the modulated signal from a track on the record carrier.

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