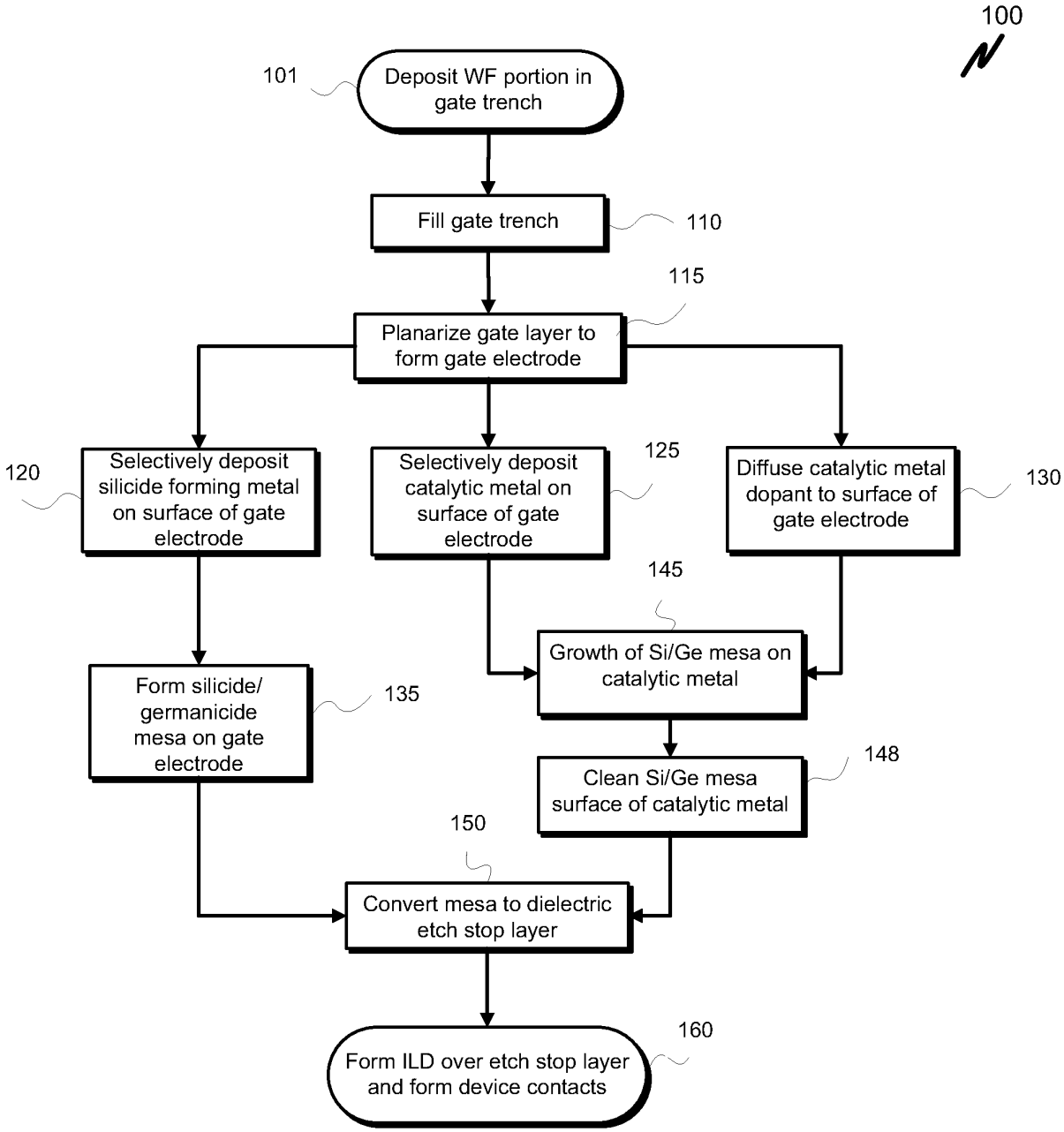

100
101
Deposit WF portion in gate trench
Fill gate trench
110
115
Planarize gate layer to form gate electrode
120
Selectively deposit silicide forming metal on surface of gate electrode
125
Selectively deposit catalytic metal on surface of gate electrode
130
Diffuse catalytic metal dopant to surface of gate electrode
145
Growth of Si/Ge mesa on catalytic metal
135
Form silicide/ germanicide mesa on gate electrode
148
Clean Si/Ge mesa surface of catalytic metal
150
Convert mesa to dielectric etch stop layer
160
Form ILD over etch stop layer and form device contacts

FIG. 1

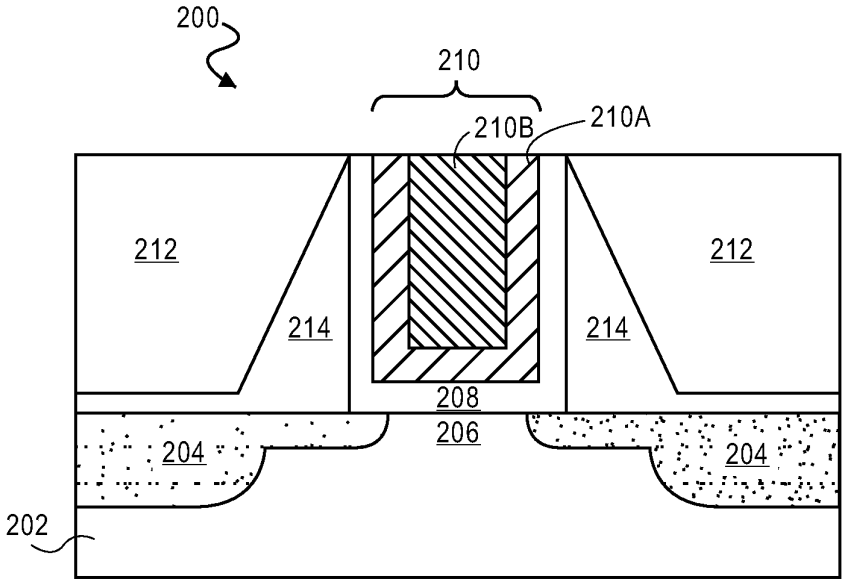


FIG. 2

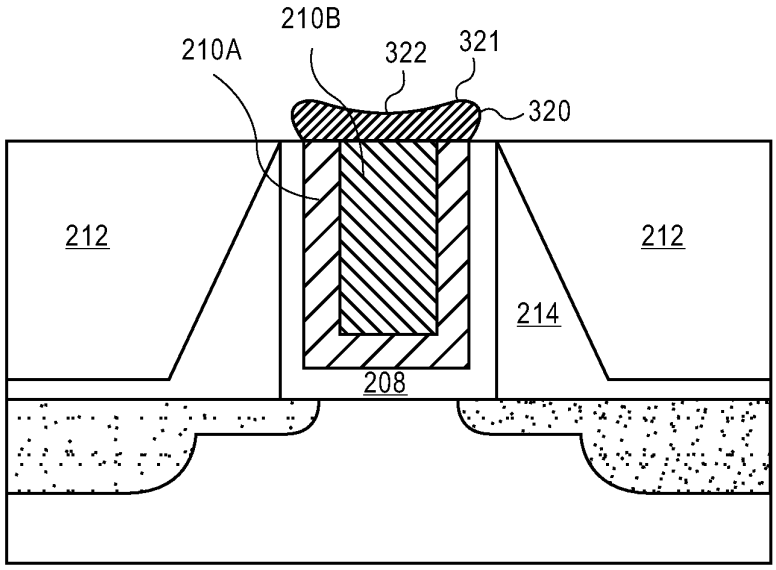


FIG. 3A

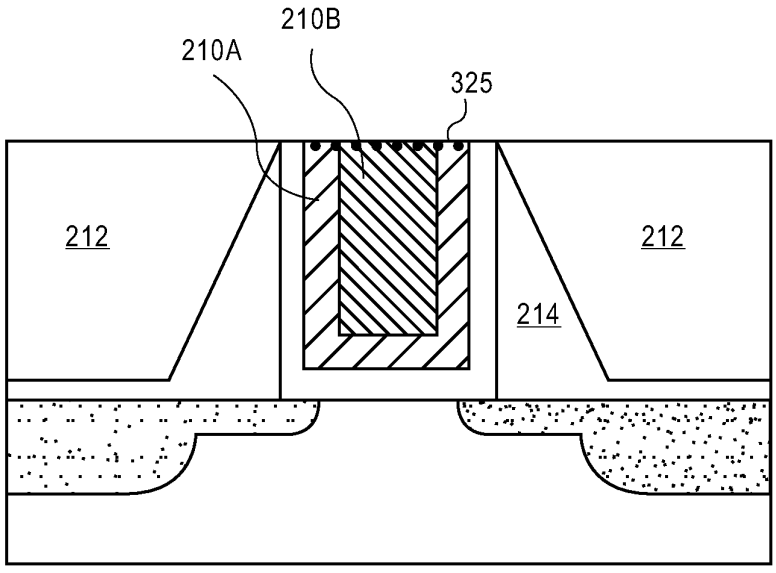


FIG. 3B

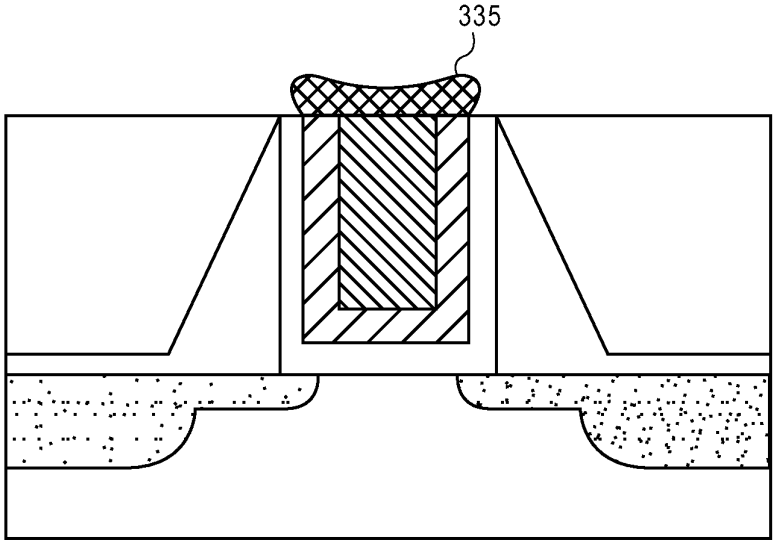


FIG. 4A

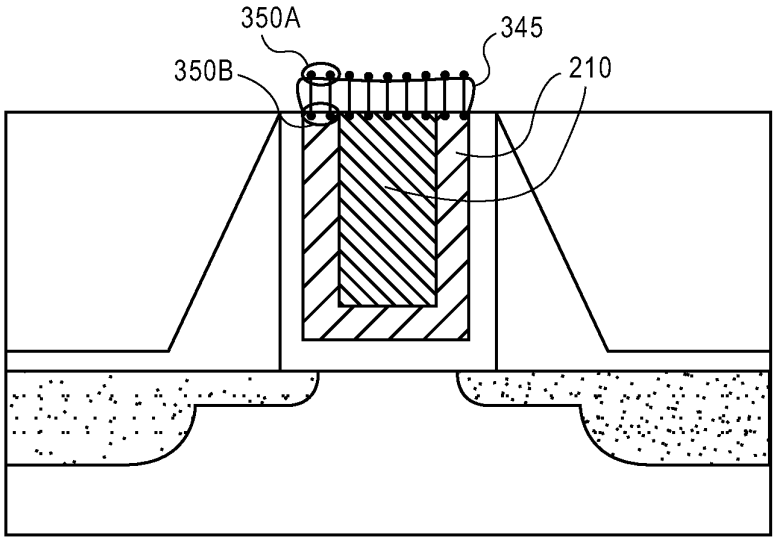


FIG. 4B

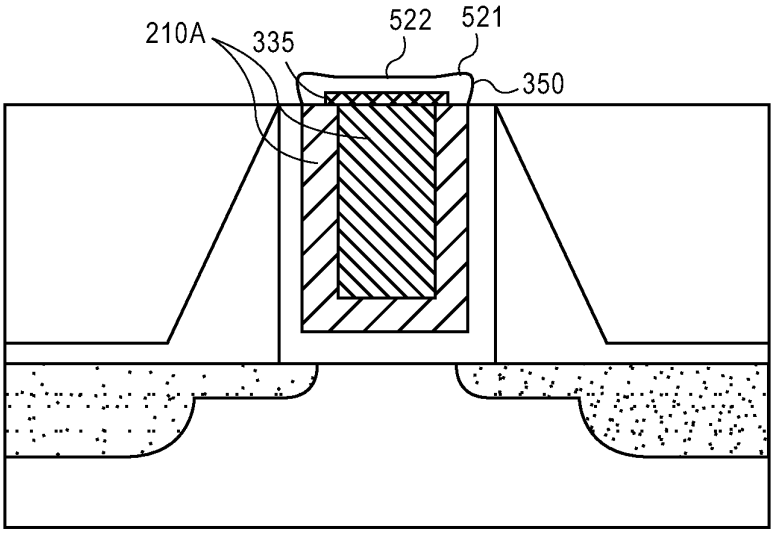


FIG. 5A

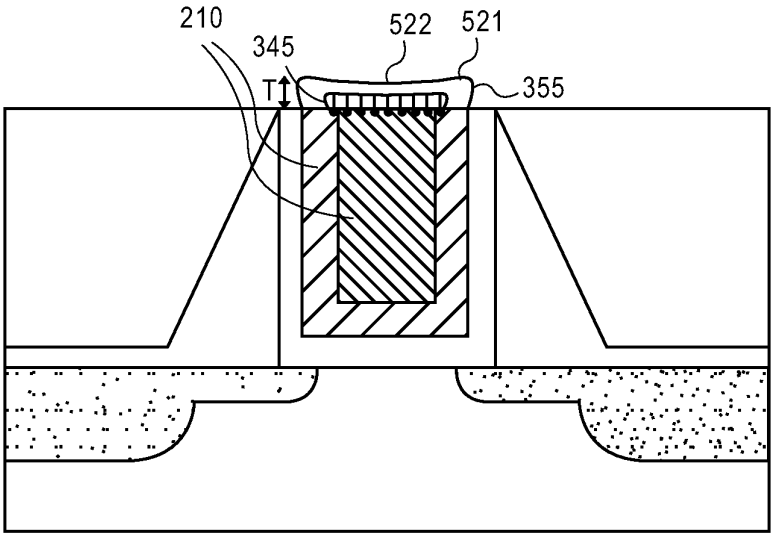


FIG. 5B

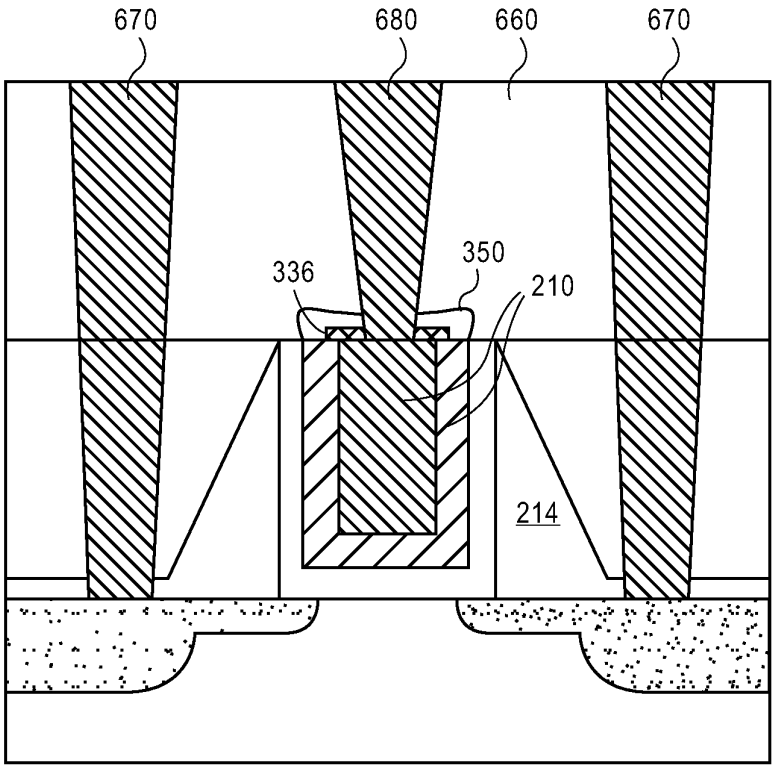


FIG. 6A

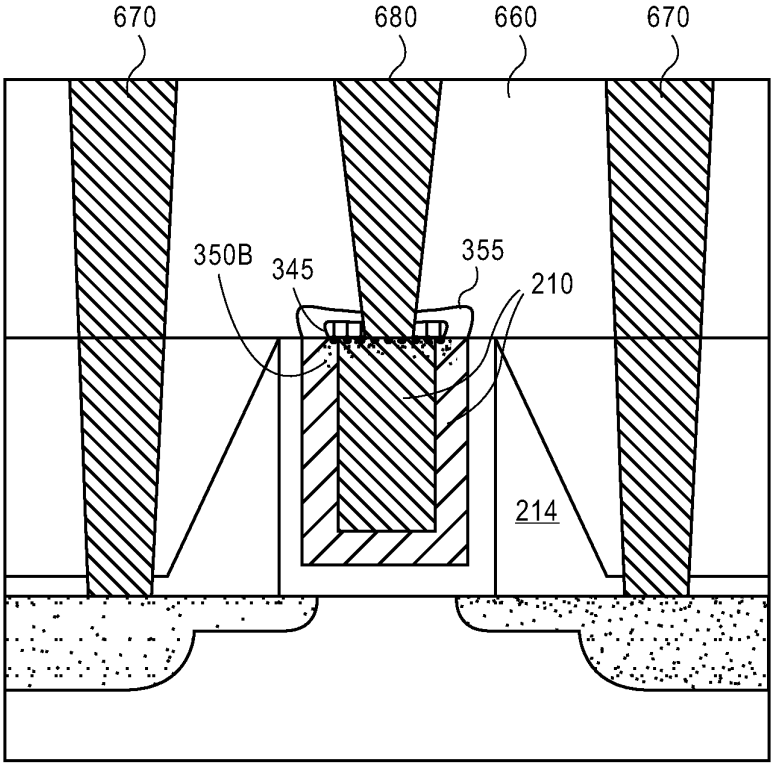


FIG. 6B